EVM User's Guide: SK-AM62-LP

AM62x-Low Power SK Evaluation Module

Description

The AM62x-Low Power (LP) starter kit (SK) evaluation module (EVM) is a low-cost starter kit built around the AM62x system-on-chip (SoC). The AM62x processor comprises of a quad-core 64-bit Arm®-Cortex® A53 microprocessor, single-core Arm Cortex-R5F MCU and an Arm Cortex-M4F MCU. The SK EVM allows the user to experience a great dual display feature through HDMI (over DPI) and LVDS, up to 2K resolution, and industrial communication applications using serial, Ethernet, USB and other interfaces.

Applications

- Automotive HMI
- Driver monitoring system
- Industrial applications
  - PLC
  - Automation control
  - Monitor and supervisor system

Features

- 2x Gigabit Ethernet RJ45 connectors
- 2GB LPDDR4 memory
- 1Gb OSPI Flash memory
- 16GB eMMC Flash memory
- MicroSD card slot
- 1x USB 2.0 Type-C®
- 1x USB 2.0 Type-A
- 1x 3.5mm TRRS audio jack
- M.2 connector for Wi-Fi/BT module
- HDMI® connector for external display
- 3x GPIO expansion connector
- CSI Camera Header
- 1x LVDS Display connector

This design incorporates HDMI® technology.

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1 Evaluation Module Overview

1.1 Introduction

This technical user's guide describes the hardware architecture of the SK-AM62-LP EVM, a low-power starter kit evaluation module designed to accelerate development with the AM62x system-on-chip (SoC) from Texas Instruments (TI™). This versatile platform features a powerful quad-core ARM® Cortex®-A53 processor and two integrated microcontrollers capable of running Embedded Linux and RTOS operating systems, making this platform good choice for a wide range of industrial automation and monitoring applications. Users can explore rich interface options, including dual-display capabilities (HDMI and LVDS) and robust industrial communication designs using Ethernet™, USB, and serial interfaces. The SK EVM can communicate with other processors or systems and act as a communication gateway. The SK EVM can also directly operate as a standard remote I/O system or simple sensor connected to an industrial communication network. The embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ IDE from Texas Instruments.

Note

This evaluation board is a pre-production release and has several known issues that should not be copied into a production system

1.2 Kit Contents

- EVM
- Quick Start Guide

Note

The maximum length of the IO cables shall not exceed 3 meters.

1.3 Device Information

The SK-AM62-LP EVM is centered around the AM62x System-on-Chip (SoC) featuring a quad-core ARM Cortex-A53 processor and integrated microcontrollers. Key components include 2GB of LPDDR4 RAM, 512 Mbit OSPI flash, a TPS65219 Power Management IC (PMIC), and a SiI9022A HDMI transmitter. The board integrates an onboard XDS110 JTAG emulator. Furthermore, the SK-AM62-LP supports Linux® and Android development with a feature-rich software development kit (SDK). On-chip emulation logic allows for emulation and debugging using standard development tools such as the Code Composer Studio integrated development environment (IDE) (CCSTUDIO) as well as an intuitive out-of-box user's guide to quickly start design evaluation

1.4 EVM Revisions and Assembly Variants

The various SK-AM62-LP EVM PCB design revisions, and assembly variants are listed in Table 1-1. The specific PCB revision is indicated in silkscreen on the PCB and the specific assembly variant is indicated with an additional sticker label

Table 1-1. SK EVM PCB Design Revisions and Assembly Variants

OPN	PCB Revision	Assembly Variant	Revision and Assembly Variant Description
SK-AM62-LP	PROC124E1	N/A	First prototype, early release revision of the AM62X Low-Power SK EVM. Implements the Sitara AM62X MPU with a PMIC power design.
SK-AM62-LP	PROC124E2	N/A	Second prototype, early release revision of the AM62X Low-Power SK EVM. Implements many changes and bug fixes.
SK-AM62-LP	PROC124E2	PROC124E2A	Few components updated in assembly

1.5 Specification

The functional block diagram of the AM62x-Low Power SK EVM is shown in Figure 1-1.

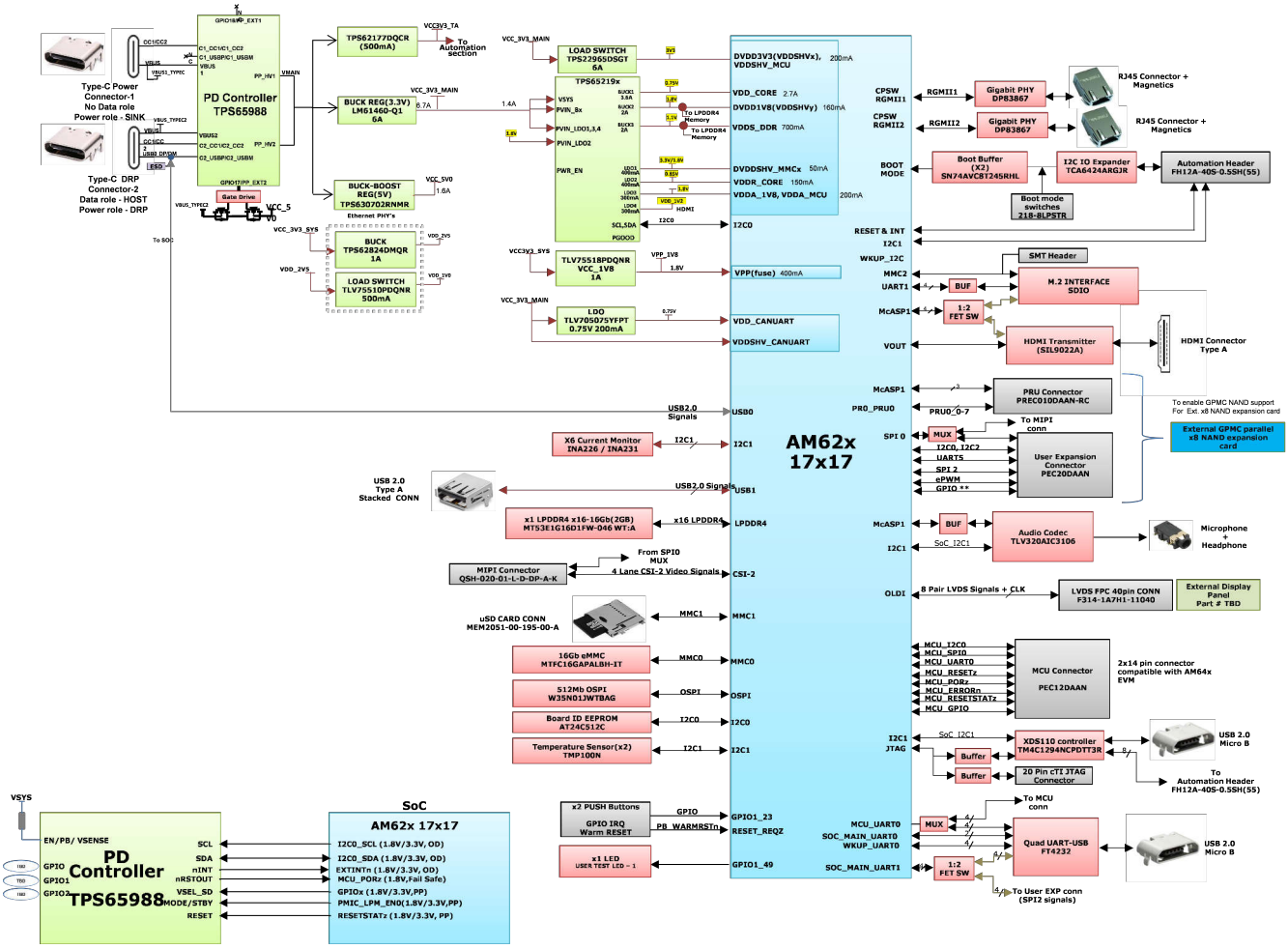


Figure 1-1. Functional Block Diagram

2 Hardware

2.1 Additional Images

This section shows the EVM pictures and location of various blocks on the board.

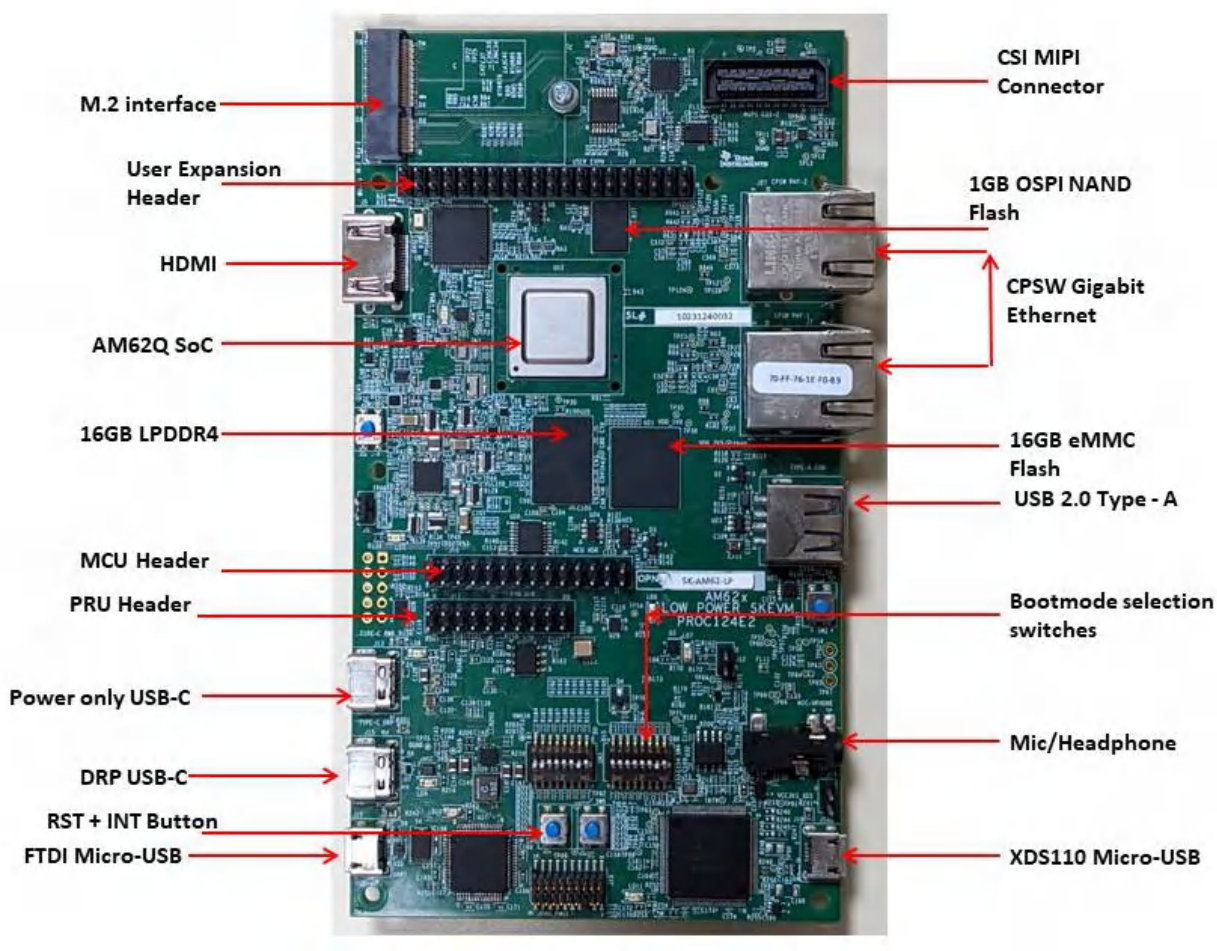


Figure 2-1. SK EVM Top

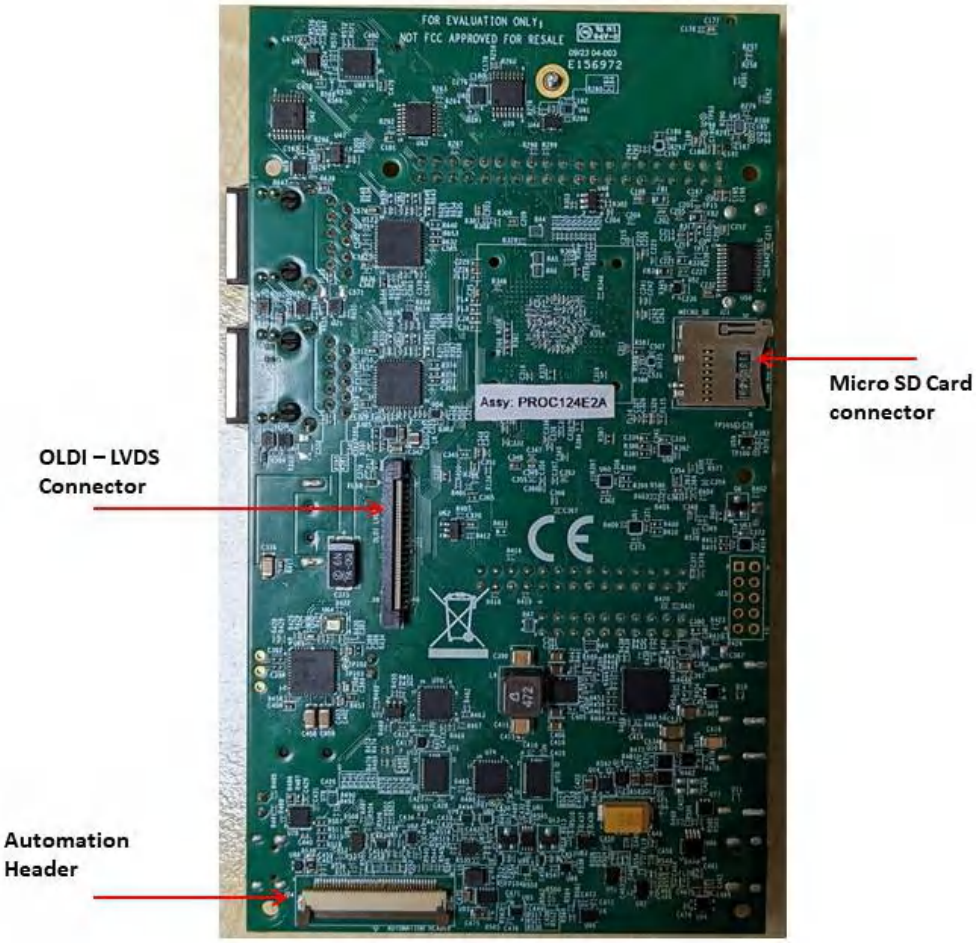


Figure 2-2. SK EVM Bottom

2.2 Key Features

The AM62x-Low Power SK EVM is a high performance, standalone development platform that enables users to evaluate and develop industrial applications for the Texas Instrument's AM62x System-on-Chip (SoC).

The following sections discuss the SK EVM's key features.

2.2.1 Processor

- AM62x SoC, 17.2mm x 17.2mm, 0.8mm pitch, 441-pin FCBGA.

2.2.2 Memory

- 2GB LPDDR4 supporting data rate up to 1600MT/s.
- Micro SD Card slot with UHS-1 support
- 1Gbit Octal SPI Flash memory
- 512 Kbit Inter-Integrated Circuit (I2C) board ID EEPROM
- 16GB eMMC Flash

2.2.3 JTAG Emulator

- XDS110 On-Board Emulator
- Supports 20-pin JTAG connection from external emulator

2.2.4 Supported Interfaces and Peripherals

- 1x USB 2.0 Type-C® Interface supporting DFP and UFP modes (Data) and DRP™ mode (Power)
- 1x USB2.0 Host Interface - Type A
- 1x HDMI Interface

- Audio line in and Mic + Headphone out
- M.2 Key E interface support for both Wi-Fi® and Bluetooth® modules
- 2x Gigabit Ethernet™ ports supporting 10/100/1000Mbps data rate on two connectors (RJ45, Un-populated Automotive).
- Quad port UART to USB circuit over microB USB connector
- INA devices for current monitoring
- 2x temperature sensors near SoC and LPDDR4 for thermal monitoring

2.2.5 Expansion Connectors Headers to Support Application Specific Add On Boards

- CSI Camera Header
- 1x LVDS Display connector
- User Expansion connector
- PRU Header
- MCU Header
- Test Automation Header

2.3 Power

2.3.1 Power Requirements

Power the AM62x-Low Power SK EVM through either of the two USB Type-C Connectors.

Table 2-1. USB Type-C Connectors

Connector	Power Role	Data Role
Connector 1 (J13)	SINK	None
Connector 2 (J15)	DRP	USB2.0 DFP or UFP

The AM62x-Low Power SK EVM supports voltage input from 5V to 15V and 3A of current. A USB PD controller (manufacturer part number: TPS65988DHRSHR) is used for PD negotiation upon cable detection to get necessary power required for the board. Connector 1 is configured as an UFP Port and has no Data role. Connector 2 is configured as a DRP port and can act as DFP only when Connector 1 powers the board. When both the connectors are connected to external power supply, the port with highest PD power contract powers the board.

Table 2-2. Type-C port Power roles

J13 (UFP)	J15 (DRP)	Board Power	Remarks
Plugged in	NC	ON - J13	J13 acts as the UFP and only sinks power and J15 can act as DFP if a peripheral is connected
NC	Plugged in	ON - J15	J15 acts as the UFP and can only sink power
Plugged in	Plugged in	ON- J13 or J15	The port with highest PD power contract powers the board

The PD IC uses a SPI EEPROM to load the necessary configuration on power up so that the PD IC can negotiate a power contract with a compatible power source.

The configuration file is loaded to the EEPROM using header J23. Once the EEPROM is programmed the PD obtains the configuration files via SPI communication. Upon loading the configuration files the PD negotiates with the source to obtain the necessary power requirement.

Power indication LEDs are provided for both the Type-C connectors for the user to identify which connector is powering the SKEVM Board. An external power supply (Type-C output) can be used to power the EVM but is not included as part of the SKEVM kit.

Table 2-3. Recommended External Power Supplies

DigiKey Part Number	Manufacturer	Manufacturer Part Number
1939-1794-ND	GlobTek®, Inc.	TR9CZ3000USBCG2R6BF21
Q1251-ND	Qualtek®	QADC-65-20-08CB

1. This is the adapter part number used for compliance testing.

Note

- Minimum Voltage: 5VDC
- Recommended Minimum Current: 3000mA
- Maximum Voltage: 15VDC
- Maximum current: 5000mA

Because SK-AM62-LP implements USB PD for power, the device can negotiate to the highest voltage and current combination supported by both the Device and power adapter. The power supply can exceed the maximum voltage and current requirements listed above if the power adapter is compliant with the USB-C® PD specification.

Note

TI recommends using an external power supply or power accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, or PSE.

2.3.2 Power Input

Both Type-C Connectors (VBUS and CC lines) are connected to a Dual PD controller manufacturer part number TPS65988. The TPS65988is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for two USB Type-C Connectors. Upon cable detection, the TPS65988 communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65988 enables the appropriate power path. The two internal power paths of TPS65988 are configured as sink paths for the two Type-C ports and an external FET path is provided for Type-C CONN 2 to source 5V when acting as DFP. The external FET path is controlled by GPIO17/PP_EXT2 of the PD controller. TPS65988 PD controller can provide an output of 3A (15V max) through CC negotiation. The VBUS pins from both the Type C connectors are connected to the VBUS pins of the PD controller. The output of the PD is VMAIN which is given to on board Buck-Boost and Buck regulators to generate fixed 5V and 3.3V supply for the SKEVM board.

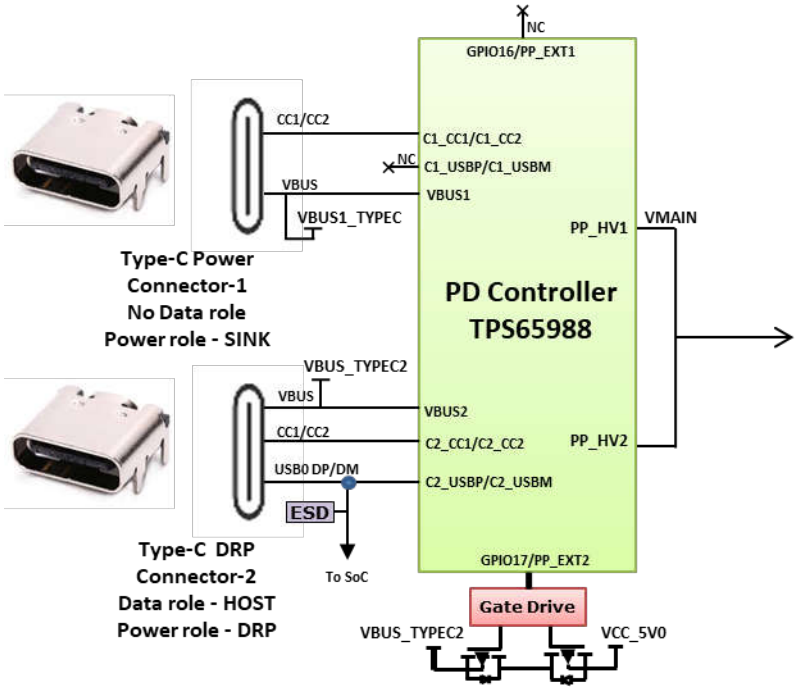


Figure 2-3. Power Input Block Diagarm

2.3.3 Power Supply

AM62x-Low Power SK EVM uses an array of DC-DC converters to supply the various memories, clocks, SoC and other components on the board with the necessary voltage and the power required.

Figure 2-4 shows the various discrete regulators and LDOs used to generate power rails and the current consumption of each peripheral on AM62x-Low Power SK EVM board.

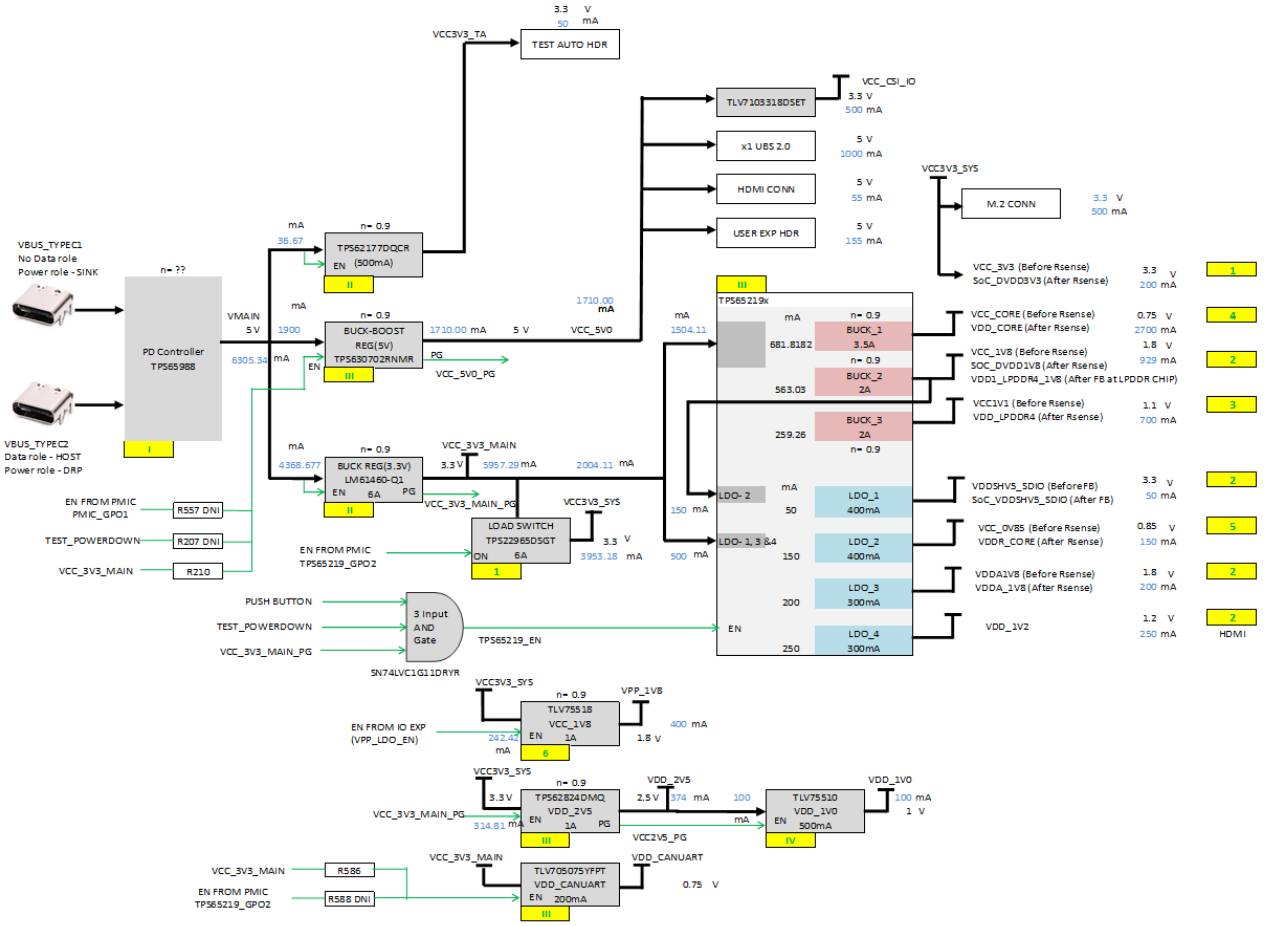


Figure 2-4. Power Architecture

The following sections describe the power distribution network topology that supplies the SK EVM board, supporting components and reference voltages.

The AM62x-Low Power SK EVM board includes a power design based on a PMIC as well as discrete power supply components. The initial stage of the power supply is VBUS voltage from either of the two USB Type C connectors J13 and J15. A USB™ Type-C Dual PD controller (manufacturer part number: TPS65988DHRSHR) is used for negotiation of the required power to the system.

Buck-Boost controller TPS630702RNMR and Buck converter LM61460-Q1 are used for the generation of 5V and 3.3V respectively and the input to the regulators is the PD output. These 3.3V and 5V are the primary voltages for the AM62x-Low Power SK EVM Board power resources. The 3.3V supply generated from the Buck regulator LM61460-Q1 is the input supply to the Various SOC regulators and LDOs. The 5V supply generated from the Buck Boost regulator TPS630702RNMR is used for powering the onboard peripherals. Table 2-4 lists the onboard discrete regulators and LDOs that are used.

Table 2-4. On-board Discrete Regulators and LDOs

On-board Discrete Regulators and LDOs	Description
TPS62824DMQR	To generate VDD_2V5 rail for PHY and DDR peripherals
TLV75510PDQNR	To generate VDD_1V0 for Ethernet™ PHYs
TPS65219	To generate various SoC and peripheral supply
TPS62177DQCR	Powering the always
TLV75518LDO	e-Fuse programming of SoC

Table 2-4. On-board Discrete Regulators and LDOs (continued)

On-board Discrete Regulators and LDOs	Description
TPS79601LDO	XDS110 On board emulator
TPS73533LDO	FT4232 UART to USB Bridge
TLV705075YFPT	To generate VDD_CANUART rail

Additionally, GPIO from the test automation header is also connected to the TPS630702RNMR Enable pin to control ON and OFF of the SKEVM using the test automation board. The GPIO only disables the VCC_5V0 output of TPS630702RNMR from which all other power supplies are derived. SoC has different IO groups.

2.3.4 Power ON OFF Procedures

Power to the EVM is provided through an external power supply providing PD voltage and current to the either of the two USB Type-C Ports.

2.3.4.1 Power-On Procedure

1. Place the SK EVM boot switch selectors (SW3, SW4) into selected boot mode. Figure 2-5 shows example boot-modes for the SD card.
2. Connect your boot media (if applicable).
3. Attach the PD capable USB Type-C cable to the SKEVM Type-C (J13 or J15) Connector.
4. Connect the other end of the Type-C cable to the source, either AC Power Adapter, or Type C source device (such as a Laptop computer).
5. Visually inspect that either LD8 or LD9 LED is illuminated.
6. XDS110 JTAG and UART debug console output are routed to micro-USB ports J18 and J17, respectively.

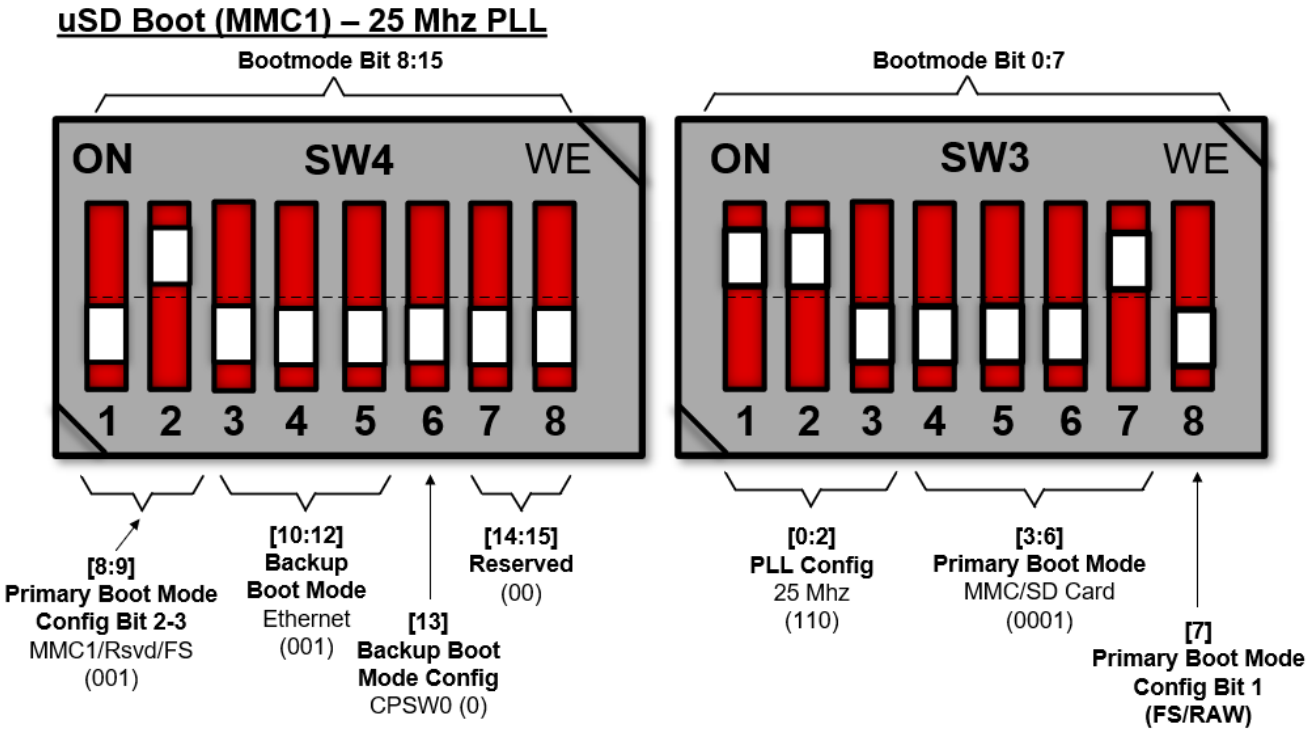


Figure 2-5. Example SD Boot Mode

2.3.4.2 Power-Off Procedure

1. Disconnect AC power from AC/DC converter.
2. Remove the USB Type-C cable from the SK EVM.

2.3.4.3 Power Test Points

Table 2-5 lists the test points for each power output on the board.

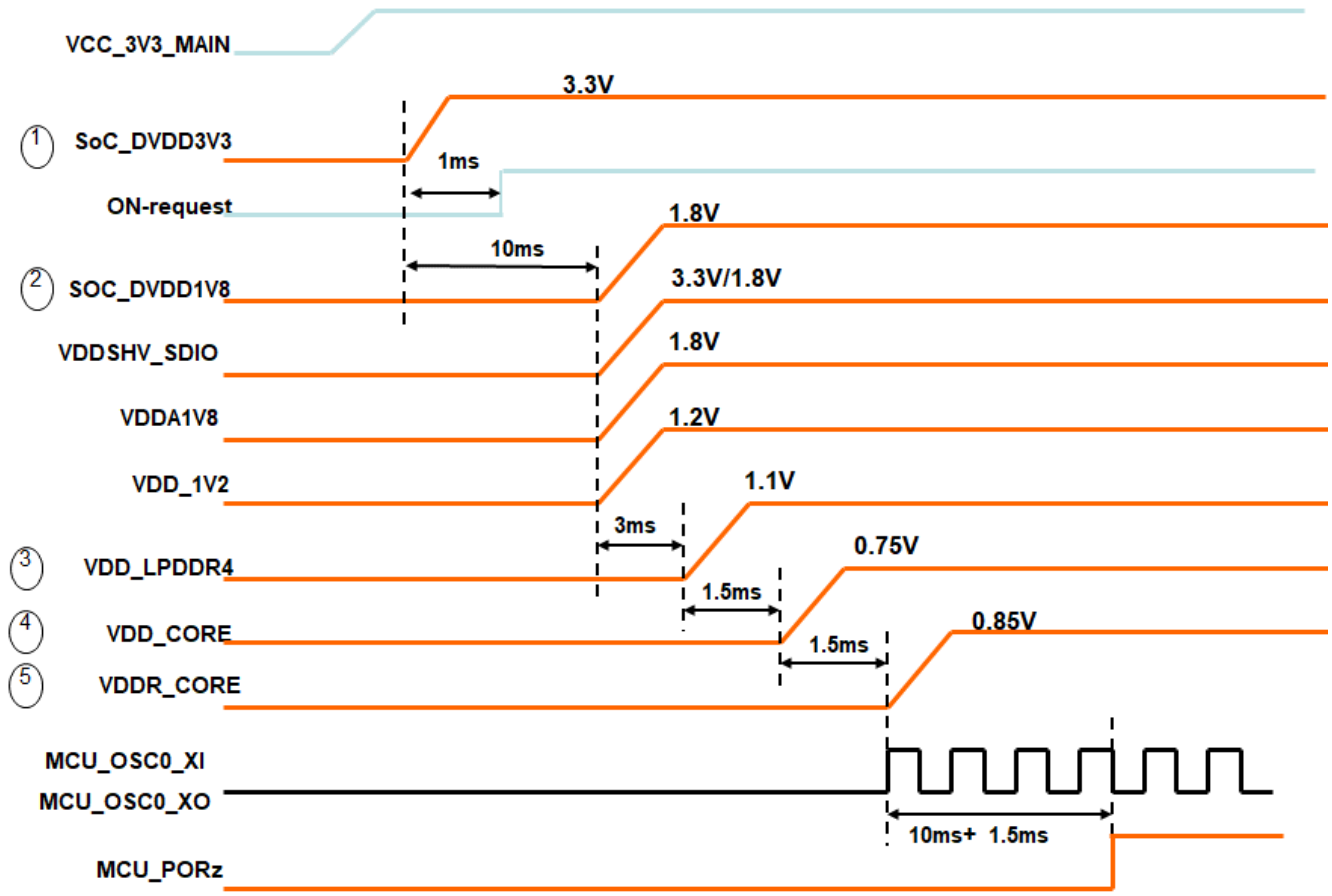
Table 2-5. Power Test Points

SI Number	Power Supply	Test Point	Voltage
1	VBUS_TYPEC1	R165.1	5V-15V
2	VBUS_TYPEC2	R214.1	5V-15V
3	VMAIN	TP73	5V-15V
4	VCC_5V0	TP76	5V
5	VCC_3V3_MAIN	TP56	3.3V
6	VCC3V3_TA	TP91	3.3V
7	VCC_3V3_SYS	TP54	3.3V
8	VCC_CORE	TP39	0.75V
9	VCC1V8_SYS	TP44	1.8V
10	VCC1V1	TP49	1.1V
11	VDDSHV_SDIO	TP41	1.8V/3.3V
12	VCC_0V85	TP51	0.85V
13	VDDA1V8	TP52	1.8V
14	VDD_1V2	TP53	1.2V
15	VDD_2V5	TP40	2.5V
16	VPP_1V8	TP33	1.8V
17	VDD_1V0	TP35	1.0V
18	VCC_CSI_IO	C12.1	1.8V/3.3V
19	VCC3V3_EXP	C192.1/J3.1	3.3V
20	VCC5V0_EXP	C185.1/J3.2	5.0V
21	VCC3V3_PRU	C384.1/J11.1	3.3V
22	VDD_MMC1	C39.1/FL8.1	3.3V
23	VBUS_5V0_TYPEA1	C375.1/C110.1	5.0V
24	XDS_USB_VBUS(1)	TP90	5.0V
25	VCC3V3_XDS(1)	TP81	3.3V
26	FT4232_USB_VBUS(2)	J17.1	5.0V
27	VCC_3V3_FT4232(2)	LD10.2	3.3V
28	VCC_1V8_FT4232(2)	C166.2	1.8V

(1) This voltage is available only when micro B to type A USB cable is connected between J18 and host PC.
(2) This voltage is available only when micro B to type A USB cable is connected between J17 and host PC.

2.3.5 Power Sequencing

The power sequencing of AM62x-Low Power EVM is given below.



2.3.6 AM62x 17x17 SoC Power

The core voltage of the AM62x 17x17 SoC can be 0.75V or 0.85V based on the PMIC configuration and on the power optimization requirement. By default, the PMIC, configured as VDD_CORE = 0.75V, can be changed to 0.85V by changing the PMIC configuration register. Current monitors are provided on all the SoC power rails.

The SoC has different IO groups. Each IO group is powered by specific power supplies as shown in the table below.

Table 2-6. SoC Power Rails

Sl. No	Power Supply	SoC Supply Rails	IO Power Group	Voltage
1	VDD_CORE	VDDA_CORE_USB		0.75
		VDDA_CORE_CSI		
		VDD_CANUART	CANUART	
		VDD_CORE	CORE	
2	VDDR_CORE	VDDR_CORE	CORE	0.85
3	VDDA_1V8	VDDA_1V8_CSIRX.	CSI	1.8
		VDDA_1V8_USB	USB	
		VDDA_1V8_MCU		
		VDDA_1V8_OLDI	OLDI	
		VDDA_1V8_OSCO	OSCO	
		VDDA_PLL0, VDDA_PLL1,VDDA_PLL2		
4	VDD_LPDDR4	VDDS_DDR	DDR0	1.1
		VDDS_DDR_C		
5	VPP_1V8	VPP_1V8		1.8

Table 2-6. SoC Power Rails (continued)

Sl. No	Power Supply	SoC Supply Rails	IO Power Group	Voltage
6	SoC_VDDSHV5_SDIO	VDDSHV5	MMC1	3.3
7	SOC_DVDD1V8	VDDSHV0	General	3.3
		VDDSHV1	OSPI	1.8
		VDDSHV4	MMC0	
		VDDSHV6	MMC2	
		VMON_1P8_SOC		
8	SOC_DVDD3V3	VDDSHV0	General	3.3
		VDDSHV2	RGMII	
		VDDSHV3	GPMC	
		VDDSHV_MCU	MCU General	
		VMON_3P3_SOC		
		VDDA_3P3_USB	USB	

2.3.7 Current Monitoring

INA231 power monitor devices are used to monitor current and voltage of various power rails of AM62x 17x17 SoC. The INA231 interfaces to the AM62x 17x17 SoC through I2C interface (SoC_I2C1). Four terminal, high precision shunt resistors are provided to measure load current.

Table 2-7. INA I2C Device Address

Source	Supply net	Device Address	Value of the Shunt Connected to the Supply Rail
VCC_CORE	VDD_CORE	0x40	10mΩ± 1%
VCC_0V85	VDDR_CORE	0x41	10mΩ± 1%
VCC_3V3_SYS	SoC_DVDD3V3	0x4C	10mΩ± 1%
VCC_1V8	SoC_DVDD1V8	0x45	10mΩ± 1%
VDDA1V8	VDDA_1V8	0x4E	10mΩ± 1%
VCC1V1	VDD_LPDDR4	0x46	10mΩ± 1%

2.4 AM62x-Low Power SK EVM Interface Mapping

Table 2-8. Interface Mapping

Interface Name	Port on SoC	DevicePart Number
Memory – LPDDR4	DDR0	MT53E1G16D1FW-046 WT:A
Memory –OSPI	OSPI0	W35N01JWTBAG
Memory –Micro SD Socket	MMC1	MEM2051-00-195-00-A
Memory –eMMC	MMC0	MTFC16GAPALBH-IT
Memory –Board ID EEPROM	SoC_I2C0	M24512-DFMC6TG
Ethernet 1– RGMII	SoC_RGMII1	DP83867IRRGZ
Ethernet 2– RGMII	SoC_RGMII2	DP83867IRRGZ
GPIO Port Expander1	SoC_I2C1	TCA6424ARGJR
PRU Header – 2x10 HDR	PR0_PRU0_GPOand SoC_I2C0	PREC010DAAN-RC
User Expansion Connector – 2x20 HDR	SPI0, SPI2, UART5, SoC_I2C0, SoC_I2C2 andGPIOs	PEC20DAAN
MCU Header – 2x14 HDR	MCU MCU_UART0, MCU_MCAN0, MCU_SPI0, MCU_I2C0 and MCU GPIOs	PREC014DAAN-RC
USB2.0 Type C	USB0	2012670005
USB2.0 Type A	USB1	629104151021
LVDS Display Connector	OLDI0	FFC2A32-40-T
CSI Interface	CSI0	QSH-020-01-L-D-DP-A-K

Table 2-8. Interface Mapping (continued)

Interface Name	Port on SoC	DevicePart Number
HDMI	VOUT0	Sil9022ACNU+ TPD12S016PWR + 10029449-001RLF
Audio Codec	McASP1 and SoC_I2C1	TLV320AIC3106IRGZT+ SJ-43514-SM
GPIO Port Expander 2	SoC_I2C1	TCA6424ARGJR
UART Terminal (UART-to-USB)	SoC_UART SoC_UART[1:0], WKUP_UART0 and MCU_UART0	FT4232HL + 629105150521
Test Automation Header	SoC_I2C1	FH12A-40S-0.5SH
Temperature Sensors	SoC_I2C1	TMP100NA/3K
Current Monitors	SoC_I2C1	INA231AIYFDR
Connectivity– M.2 Key E	MMC2, McASP1 and SoC_UART1	2199119-4

2.5 Clocking

Figure 2-6 shows the clocking architecture of the AM62x Low-Power SK EVM.

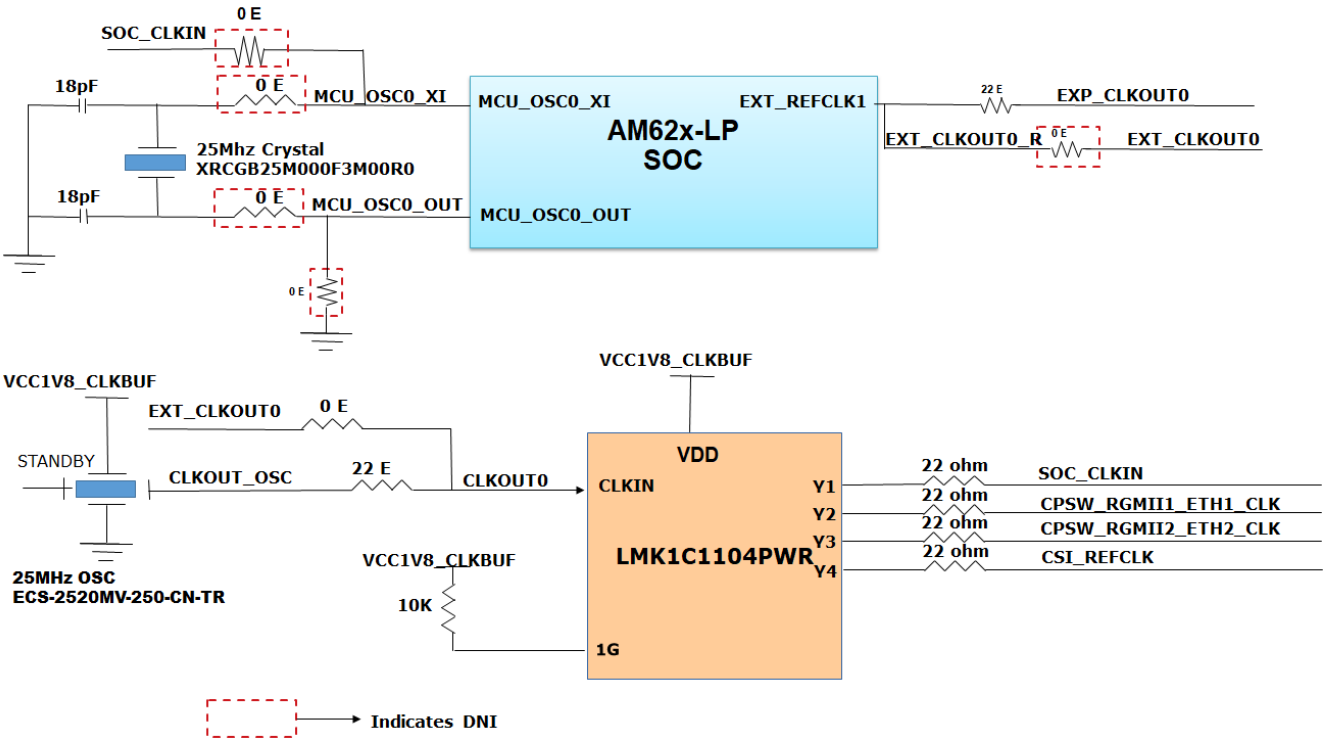


Figure 2-6. Clock Architecture

A clock generator of part number LMK1C1104PWR is used to drive the 25MHz clock to the SOC and two Ethernet PHYs. LMK1C1104PWR is a 1:4 LVCMOS clock buffer, which takes the 25MHz crystal/LVCMOS reference input and provides four 25MHz LVCMOS clock outputs. The source for the clock buffer shall be either the CLKOUT0 pin from the SOC or a 25MHz oscillator, the selection is made using a set of resistors. By default, an oscillator is used as input to the clock buffer on the AM62x Low Power SK EVM. Output Y2 and Y3 of the clock buffer are used as reference clock inputs for two Gigabit Ethernet PHYs. Output Y4 of the clock buffer are used as reference clock inputs for CSI Camera interface.

There is one external crystal attached to the AM62x SoC to provide clock to the WKUP domain of the SoC (32.768KHz).

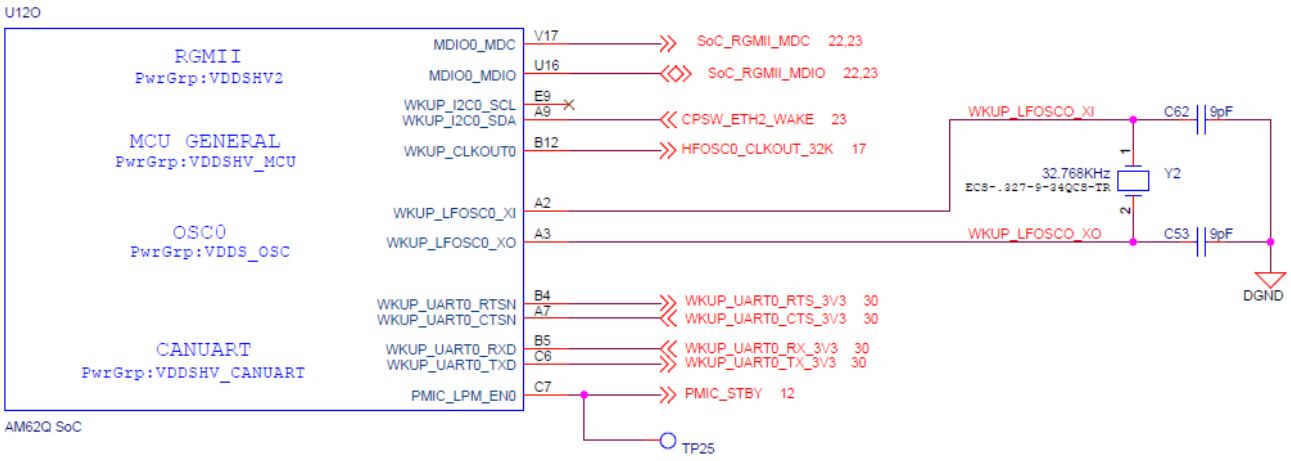


Figure 2-7. SoC Wakeup Domain Clock

Clock inputs required for peripherals such as XDS110, FT4232, HDMI transmitter and audio codec are generated locally using separate crystals or oscillators. Table 2-9 shows the crystals or oscillators used to provide the reference clocks to the EVM peripherals.

Table 2-9. Peripheral Clocking Table

Peripheral	Manufacturer Part Number	Description	Frequency
XDS110 emulator(Y3)	XRCGB16M000FXN01R0	CRY 16.000MHz 8pF SMD	16.000MHz
FT4232 Bridge(Y4)	445I23D12M00000	CRY 12.000MHz 18pF SMD	12.000MHz
Audio Codec(U64)	KC3225Z12.2880C1KX00	OSC 12.288MHz CMOS SMD	12.288MHz
HDMITransmitter(U9)	KC3225Z12.2880C1KX00	OSC 12.288MHz CMOS SMD	12.288MHz

The clock required by the HDMI transmitter can be provided by either the onboard oscillator or the SoC's AUDIO_EXT_REFCLK1, which can be selected through a resistor mux. SoC's EXT_REFCLK1 is used to provide clock to the User Expansion Connector on the SK EVM. The 32KHz clock to the M.2 module is provided by WKUP_CLKOUT0 of AM62x SoC through a voltage translational buffer.

2.6 Reset

The Reset Architecture of AM62x-Low Power SK EVM is shown below. The SoC has the following resets:

- RESETSTATz is the Main domain warm reset status output
- PORz_OUT is the Main domain power ON reset status output
- RESET_REQz is the Main domain warm reset input
- MCU_PORz is the MCU domain power ON/ Cold Reset input
- MCU_RESETSTATz is the MCU domain warm reset status output

Upon Power on Reset, all peripheral devices connected to the main domain get reset by RESETSTATz.

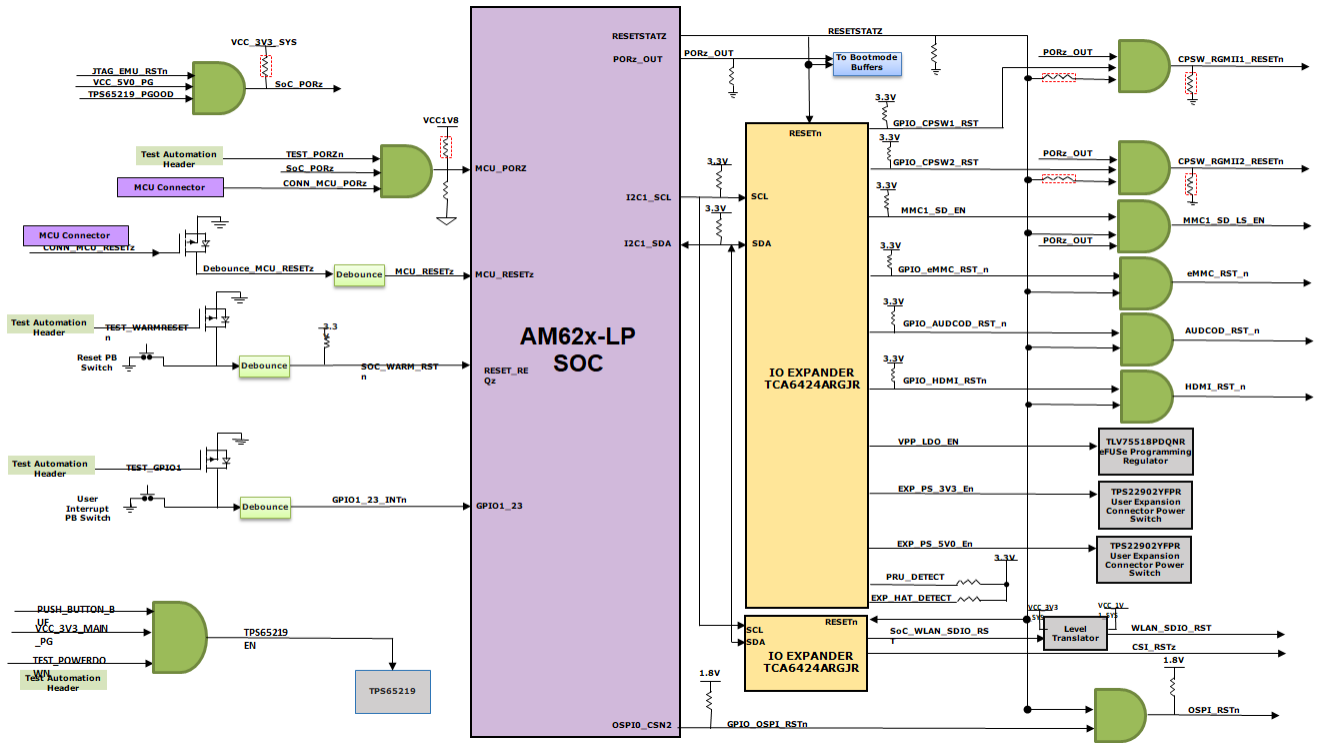


Figure 2-8. Reset Block Diagarm

2.7 OLDI Display Interface

The OLDI0 Display interface of the AM62x 17x17 SoC is connected to 40-pin LVDS display connector (J22) (manufacturer part number FFC2A32-40-T) from GCT. The OLDI Interface supports dual channel 8-bit LVDS output. Table 2-10 shows the Pin-out details of the display connector.

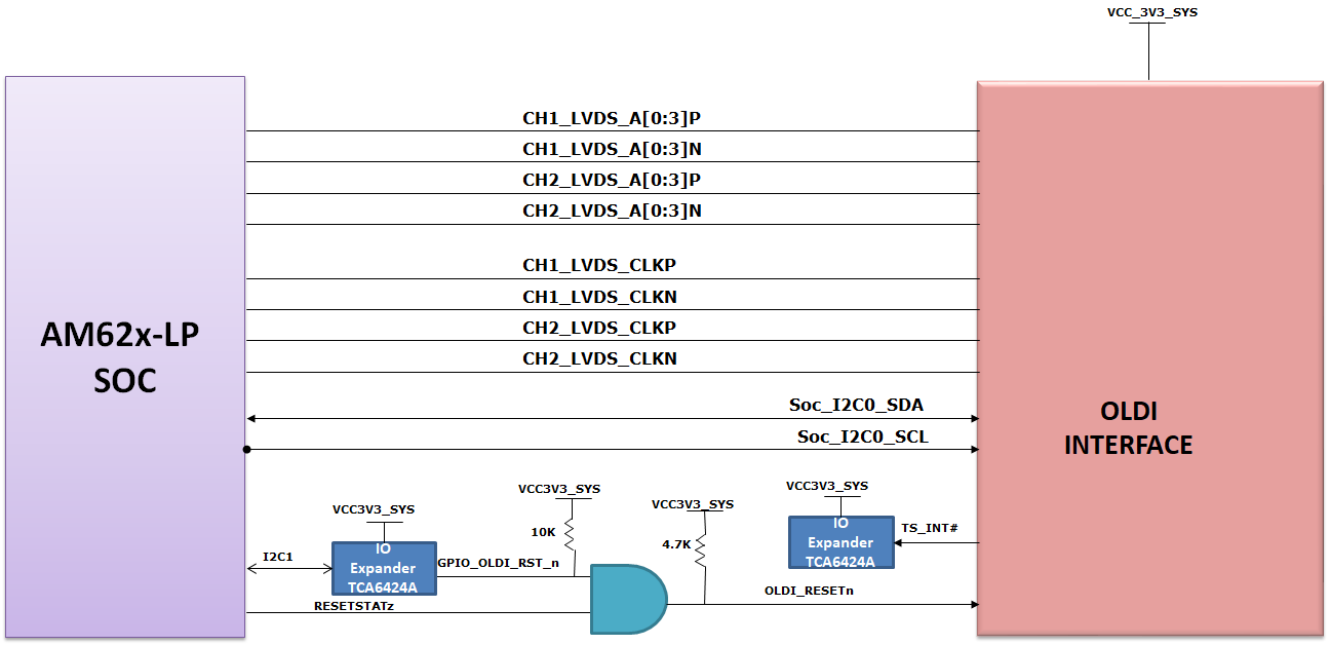


Figure 2-9. OLDI Interface Block Diagram

Table 2-10. Display Connector Pinout

Pin Number	Signal	Pin Number	Signal
1	VCC_3V3_SYS(EEPROM_VDD)	21	CH1_LVDS_A2P
2	SoC_I2C0_SCL	22	GND
3	SoC_I2C0_SDA	23	CH1_LVDS_A3N
4	NC	24	CH1_LVDS_A3P
5	NC	25	GND
6	GND	26	CH2_LVDS_A0N
7	GND	27	CH2_LVDS_A0P
8	OLDI_RESETn	28	GND
9	GPIO_OLDI_INT	29	CH2_LVDS_A1N
10	GND	30	CH2_LVDS_A1P
11	CH1_LVDS_A0N	31	GND
12	CH1_LVDS_A0P	32	CH2_LVDS_CLKN
13	GND	33	CH2_LVDS_CLKP
14	CH1_LVDS_A1N	34	GND
15	CH1_LVDS_A1P	35	CH2_LVDS_A2N
16	GND	36	CH2_LVDS_A2P
17	CH1_LVDS_CLKN	37	GND
18	CH1_LVDS_CLKP	38	CH2_LVDS_A3N
19	GND	39	CH2_LVDS_A3P
20	CH1_LVDS_A2N	40	GND

2.8 CSI Interface

The CSI-2 interface from the AM62x 17x17 SoC is terminated to a 40-pin camera MIPI connector QSH-020-01-L-D-DP-A-K. The SoC supports four CSI RX Lanes. Four are pinned out on the SKEVM. Table 2-11 lists the 40-pin camera MIPI connector pinout. SoC I2C2 signals are also connected to the CSI Header. IO Expander GPIO signals are connected to the camera GPIOs.

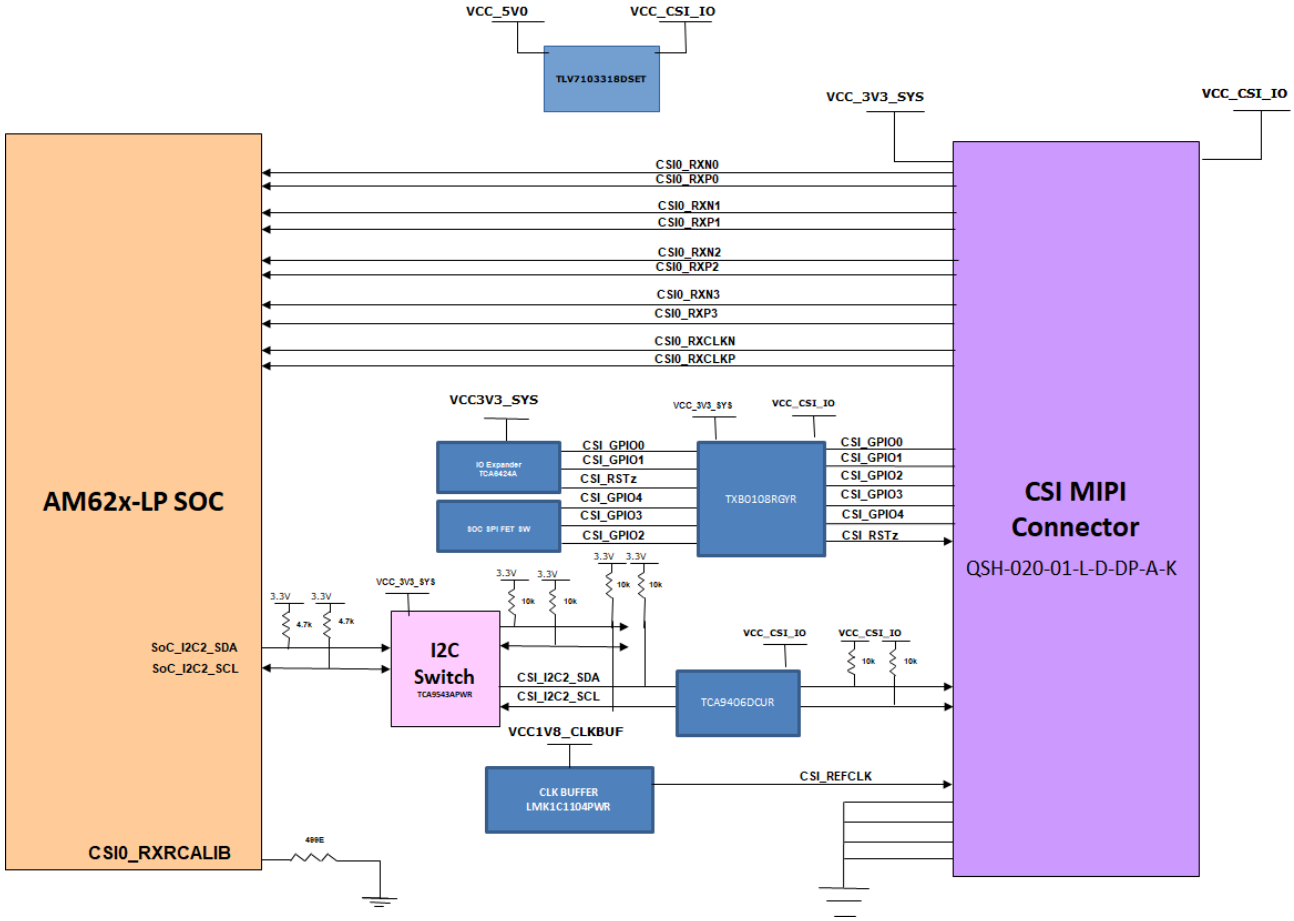


Figure 2-10. CSI Interface Block Diagram

Table 2-11. CSI Camera Connector J19 Pinout

Pin Number	Pin Description	Pin Number	Pin Description
1	NC	21	CSI0_RXP3
2	CSI_I2C2_SCL_BUFF	22	CSI_GPIO4_buff
3	NC	23	CSI0_RXN3
4	CSI_I2C2_SDA_BUFF	24	Ground
5	CSI0_RXCLKP	25	NC
6	CSI_GPIO0_buff	26	NC
7	CSI0_RXCLKN	27	NC
8	CSI_GPIO1_buff	28	NC
9	CSI0_RXP0	29	NC
10	CSI_REFCLK	30	VCC_3V3_SYS
11	CSI0_RXN0	31	NC
12	Ground	32	VCC_3V3_SYS
13	CSI0_RXP1	33	NC
14	CSI_RSTz_buff	34	VCC_3V3_SYS
15	CSI0_RXN1	35	NC
16	Ground	36	VCC_3V3_SYS
17	CSI0_RXP2	37	NC
18	CSI_GPIO2_buff	38	VCC_CSI_IO
19	CSI0_RXN2	39	NC

Table 2-11. CSI Camera Connector J19 Pinout (continued)

Pin Number	Pin Description	Pin Number	Pin Description
20	CSI_GPIO3_buff	40	VCC_CSI_IO

2.9 Audio Codec Interface

AM62x-Low Power SK EVM uses TI‘s Low-Power TLV320AIC3106 Stereo Audio Codec to interface with AM62x using McASP. TLV320AIC3106 is a low-power stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single ended or fully differential configurations. The record path of the TLV320AIC3106 contains integrated microphone bias, digitally controlled stereo microphone preamplifier and Automatic gain control (AGC) with mix and Mux capability among the multiple analog inputs. The stereo audio DAC supports sampling rates from 8kHz to 96kHz. One Standard 3.5mm TRRS Audio Jack connector (manufacturer part number: SJ-43514) is provided for MIC and Headphone output. Audio Codec’s Line inputs are terminated to Test points. SELECT pin is held LOW to select I2C as control interface. Codec can be configured over I2C interface, where I2C address can be set by driving pins MFP0 and MFP1 pin high or low. Both these pins are set to high, so the device address is set to 0x1B. Unused inputs and outputs of the Audio Codec are connected to ground. The controller clock input, MCLK to the Audio Codec is provided through a 12.288MHz oscillator. Audio serial data bus bit clock BCLK of the codec is driven by the AM62x SoC through a buffer. Audio serial data bus input and output DIN, DOUT are connected to SoC’s MCASP1_AXR0 and MCASP1_AXR2 through buffers. An AND output of RESETSTATz and a GPIO sourced via IO expander are used to reset the Audio Codec. The TLV320AIC3106 is powered by an analog supply of 3.3V, a digital core supply of 1.8V, and a digital I/O supply 3.3V.

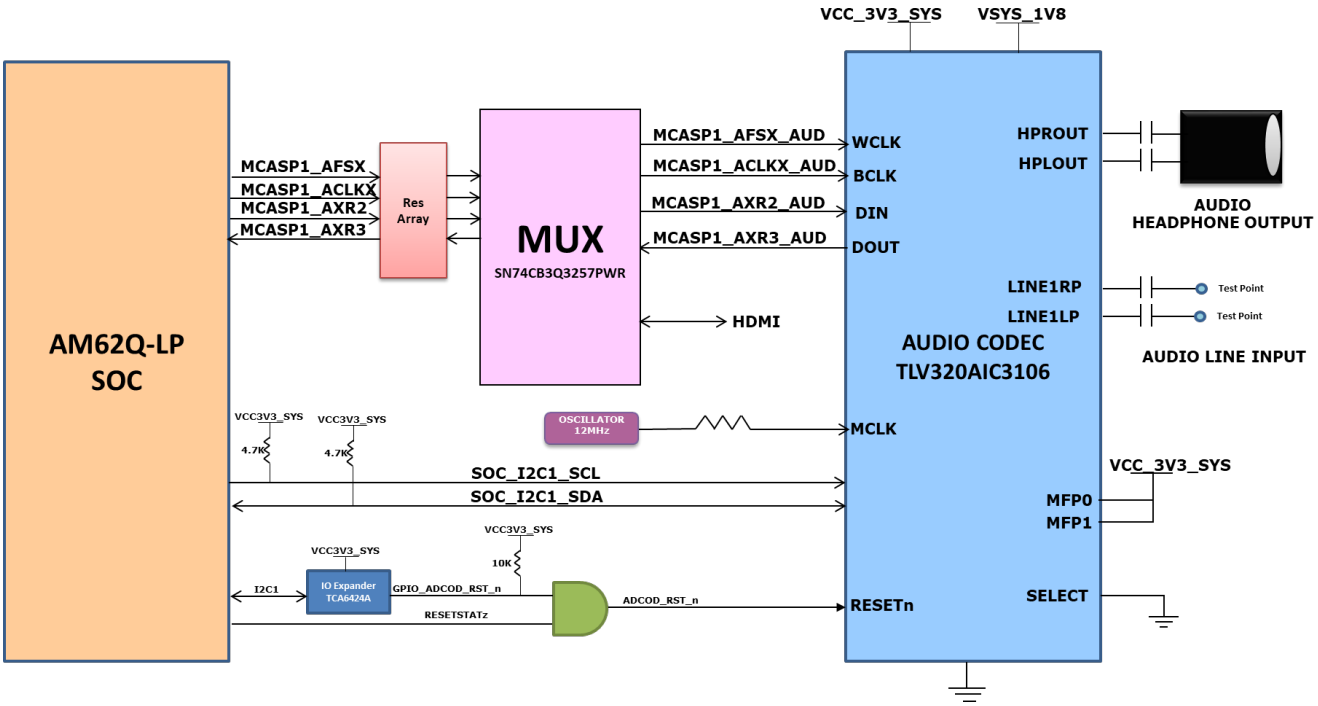


Figure 2-11. Audio Codec Interface Block Diagram

2.10 HDMI Display Interface

The DSS (Display Sub system) interface from AM62X 17x17 SoC is used on the SK EVM to provide a HDMI Interface through a standard Type-A Connector. The SK EVM features a SiI9022A HDMI Transmitter from Lattice semiconductors to convert the 24bit Parallel RGB DSS output stream as well as a McASP to a HDMI-compliant digital audio and video signal. The Data mapping format used is RGB888. The data bus width is 24-bits. SoC_I2C1 is connected to the HDMI Transmitter accesses the compatible mode registers, the TPI registers, and the CPI registers. To use the SiI9022A, the SoC needs to setup the device. This is done through the I2C interface between the SoC and the SiI9022A. Audio Data is sent from SoC to HDMI transmitter through the McASP1 instance. HDMI_I2C Bus accesses the EDID and HDCP data on an attached sink device. TMDS

Differential data pairs along with the differential clock signals from the transmitter are connected to the HDMI connector through HDMI ESD device (manufacturer part number TPD12S016PWR), which also acts as a load switch to limit current supplied to the HDMI connector from board 5V supply. The HDMI Framer is powered using 3.3V board IO supply and 1.2V by a dedicated PMIC LDO.

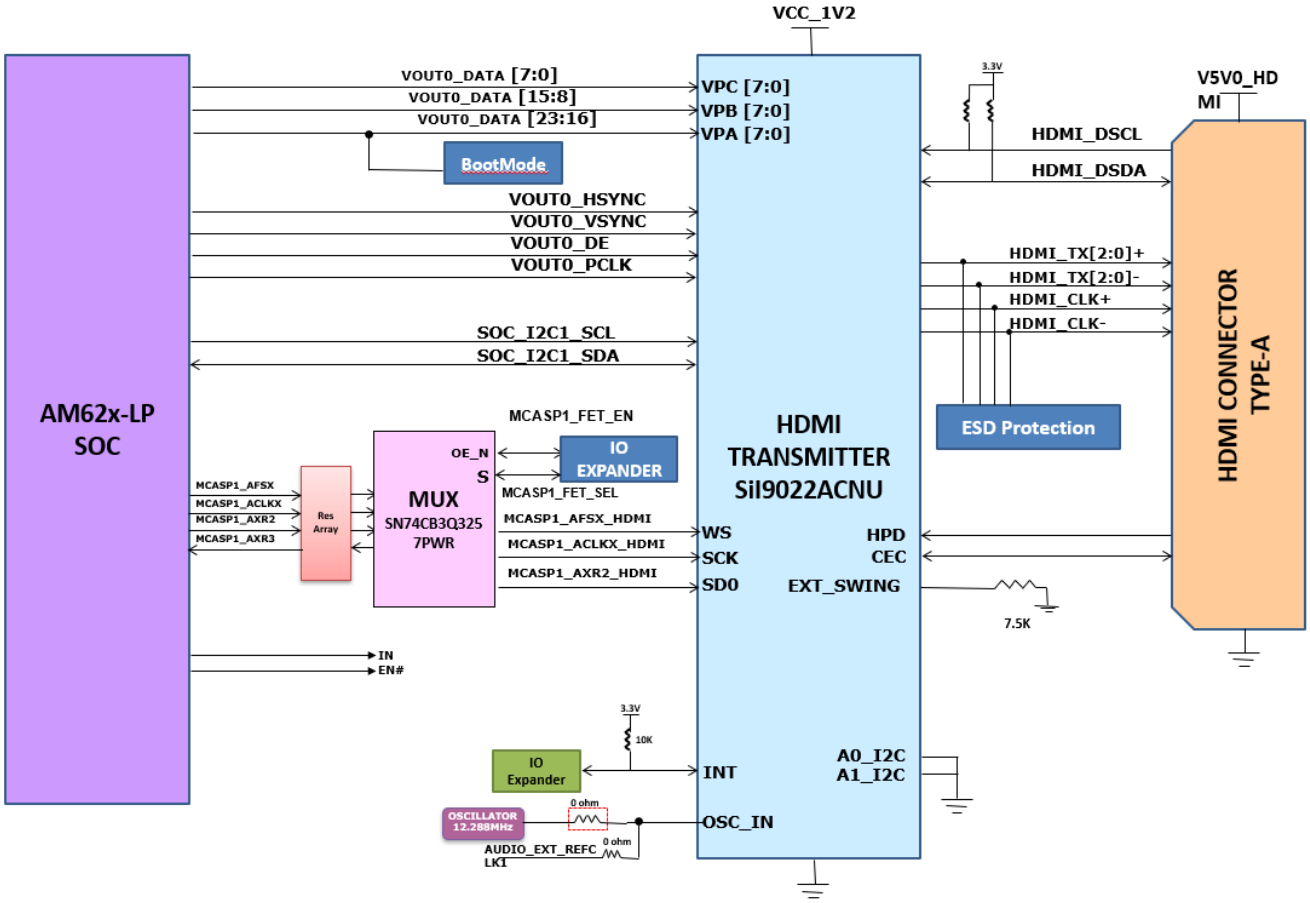


Figure 2-12. HDMI Interface Block Diagram

2.11 JTAG Interface

The AM62x Low-Power SK EVM board includes XDS110 class on board emulation. The connection for the emulator uses an USB 2.0 micro-B connector and the circuit acts as a Bus powered USB device. The VBUS power from the connector powers the emulation circuit such that connection to the emulator is not lost when the power to the SKEVM is removed. Voltage translation buffers are used to isolate the XDS110 circuit from the rest of the SKEVM. Optionally, JTAG Interface on SKEVM is also provided through 20 Pin Standard JTAG cTI Header J19. This allows the user to connect an external JTAG Emulator Cable. Voltage translation buffers are used to isolate the JTAG signals from cTI header from the rest of the SKEVM. The output from the voltage translators from XDS110 Section and cTI Header Section are muxed and connected to AM62X JTAG Interface. If a connection to the cTI 20 Pin JTAG connector is sensed using a presence detect circuit, the mux will be set to route the 20 pin signals from the cTI connector to the AM62X SoC in place of the on-board emulation circuit.

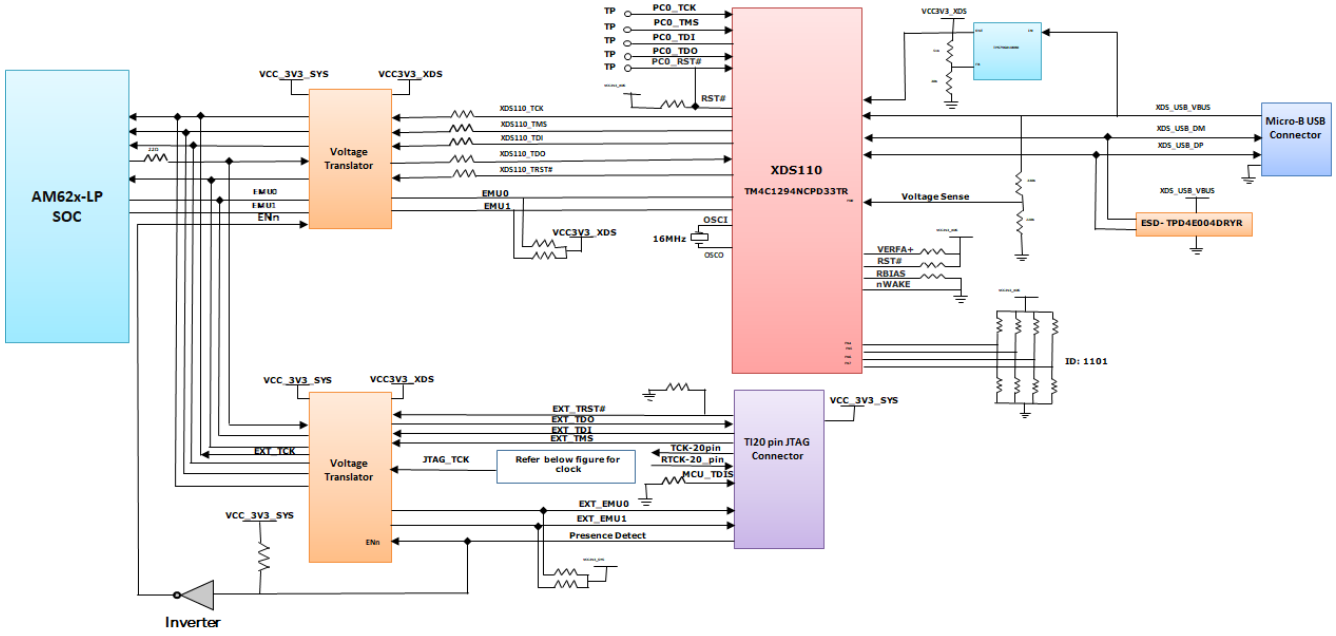


Figure 2-13. JTAG Interface Block Diagram

The pin-out of the cTI 20 pin JTAG connector are given in Table 2-12. A ESD protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against ESD pulses up to ±15kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ±8kV contact discharge and ±12kV air-gap discharge.

Table 2-12. JTAG Connector (J19) Pinout

Pin Number	Signal
1	JTAG_TMS
2	JTAG_TRST#
3	JTAG_TDI
4	JTAG_TDIS
5	VCC3V3_SYS
6	NC
7	JTAG_TDO
8	SEL_XDS110_INV
9	JTAG_cTI_RTCK
10	DGND
11	JTAG_cTI_TCK
12	DGND
13	JTAG_EMU0
14	JTAG_EMU1
15	JTAG_EMU_RSTn
16	DGND
17	NC
18	NC
19	NC
20	DGND

The pin-outs of the cTI 20 pin JTAG connector are given in Table 2-12. A ESD protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against

ESD pulses up to ±15kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ±8kV contact discharge and ±12kV air-gap discharge.

2.12 Test Automation Header

The AM62x-Low Power SK EVM has a 40-pin test automation header (FH12A-40S-0.5SH) to allow an external controller to manipulate some basic operations like power down, POR, warm reset, or boot mode control.

The 3.3V supply generated by a dedicated regulator (manufacturer part number: TPS62177DQCR) powers the test automation circuit. The I2C1 of the SoC is connected to the test automation header. Another I2C instance (BOOTMODE_I2C) from the test automation header connects to the 24-bit I2C boot mode IO expander of TCA6424ARGJR to allow control of the boot modes for the AM62X SoC.

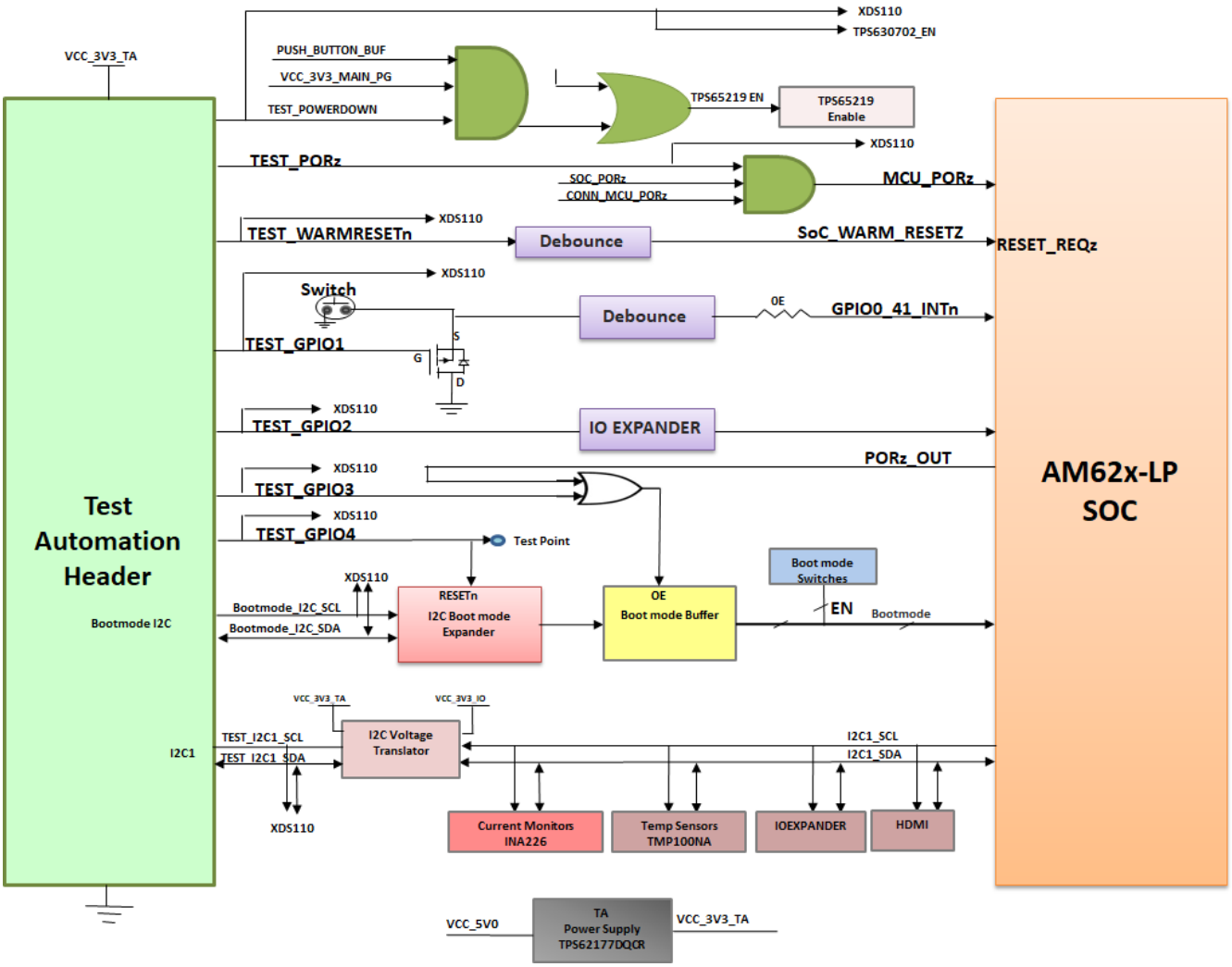


Figure 2-14. Test Automation Interface Block Diagram

The test automation circuit has voltage translation circuits so that the controller is isolated from the IO voltages used by the AM62x SoC. Control the boot mode for the AM62x SoC using DIP switches or the test automation header through the I2C IO expander. Boot mode buffers are used to isolate the boot mode controls driven through DIP Switches or I2C IO expander. The user controls the boot mode using two 8-bit DIP switches on the board. The switches connect a pull-up resistor to the output of a buffer when the switch is set to the ON position. The switches connect to a weaker pull-down resistor when set to the OFF position. The output of the buffer connects to the boot mode pins on the AM62x SoC. The output is enabled when the boot mode is needed during a reset cycle.

When boot mode is set through the test automation header, the required switch values are set at the I2C IO expander output, which overwrites the DIP switch values to give the desired boot values to the SoC. The pins used for boot mode also have other functions which can be isolated by disabling the boot mode buffer during normal operation.

The power down signal from the test automation header instructs the SK EVM to power down all the rails except for dedicated power supplies on the board. Similarly, use the PORZn signal to give a hard reset to the SoC and WARM_RESETn for warm reset of the SoC.

Table 2-13. Test Automation Connector (J24) Pinout

Pin Number	Signal	IO Direction	Pin Number	Signal	IO Direction
1	VCC3V3_TA	Power	21	NC	NA
2	VCC3V3_TA	Power	22	NC	NA
3	VCC3V3_TA	Power	23	NC	NA
4	NC	NA	24	NC	NA
5	NC	NA	25	DGND	Power
6	NC	NA	26	TEST_POWERDOWN	Input
7	DGND	Power	27	TEST_PORZn	Input
8	NC	NA	28	TEST_WARMRESETn	Input
9	NC	NA	29	NC	NA
10	NC	NA	30	TEST_GPIO1	Bidirectional
11	NC	NA	31	TEST_GPIO2	Bidirectional
12	NC	NA	32	TEST_GPIO3	Input
13	NC	NA	33	TEST_GPIO4	Input
14	NC	NA	34	DGND	Power
15	NC	NA	35	NC	NA
16	DGND	Power	36	SoC_I2C1_TA_SCL	Bidirectional
17	NC	NA	37	BOOTMODE_I2C_SCL	Bidirectional
18	NC	NA	38	SoC_I2C1_TA_SDA	Bidirectional
19	NC	NA	39	BOOTMODE_I2C_SDA	Bidirectional
20	NC	NA	40	DGND	Power

2.13 UART Interface

The four UART ports of the AM62x SoC (MCU UART0, WKUP UART0, SOC UART0 and SOC UART1) are interfaced with an FTDI FT4232HL for UART-to-USB functionality and terminated on a USB micro-B connector (J17) on board. When the AM62x-Low Power SK EVM is connected to a Host using USB cable, the computer can establish a Virtual Com Port which can be used with any terminal emulation application. The FT4232HL is bus powered.

Since the circuit is powered through BUS power, the connection to the COM port will not be lost when the SK EVM power is removed.

Table 2-14. UART Port Interface

UART Port	USB to UART Bridge	USB Connector	COM Port
SOC_UART0	FT4232HL	J17	COM1
SOC_UART1			COM2
WKUP_UART0			COM3
MCU_UART0			COM4

The FT4232 chip is configured to operate in ‘Single chip USB to four channel UART’ mode and sources the configuration file from the external SPI EEPROM connected to the chip. The EEPROM (93LC46B) supports 1Mbit/s clock rate. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG

available from the FTDI website. The FT_PROG is also used for programming the board serial number so that users can identify the connected COM port using the board serial number when one or more boards are connected to the computer.

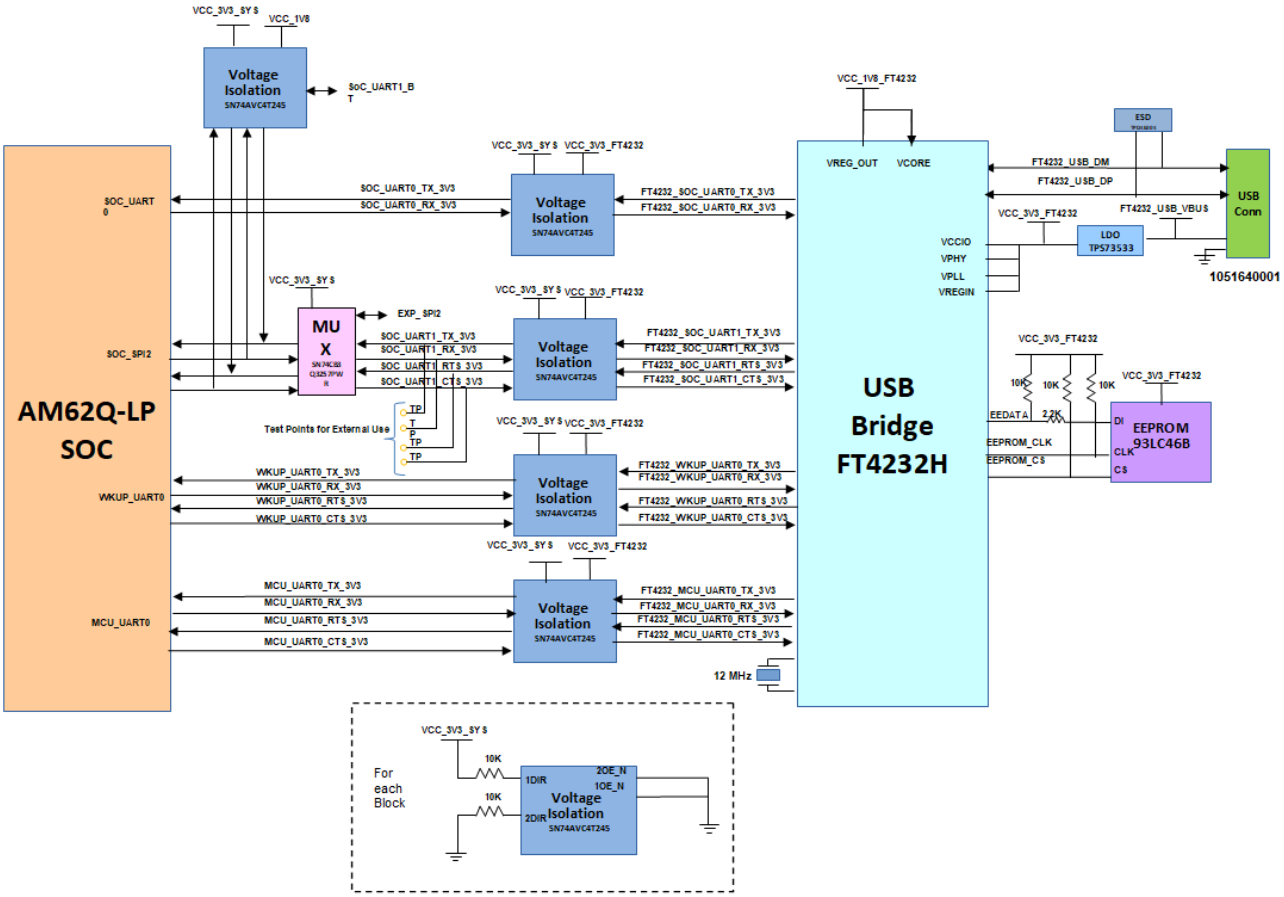


Figure 2-15. UART Interface Block Diagram

2.14 USB Interface

2.14.1 USB2.0 Type A Interface

USB2.0 data lines from Type A connector J9 are connected to the USB1 interface of the AM62x 17x17 SOC to provide USB high-speed/full-speed communication. USB1_VBUS to the SOC is provided through a resistor divider network to support (5V-30V) VBUS operation. USB1_DRVVBUS from SOC is connected to the enable pin of Load switch (manufacturer part number: TPD3S014DBVR) to allow on board 5V supply to power the VBUS..

A common mode choke of DLW21SZ900HQ2B is provided on USB Data lines to take care of EMI/ EMC.

USB Data lines from Type-A connectors are also connected to the current limit load switch and ESD Protection IC (manufacturer part number: TPD3S014DBVR). This switch limits the current to 500mA and dissipates the ESD strikes above the maximum level specified in the IEC 61000-4-2.

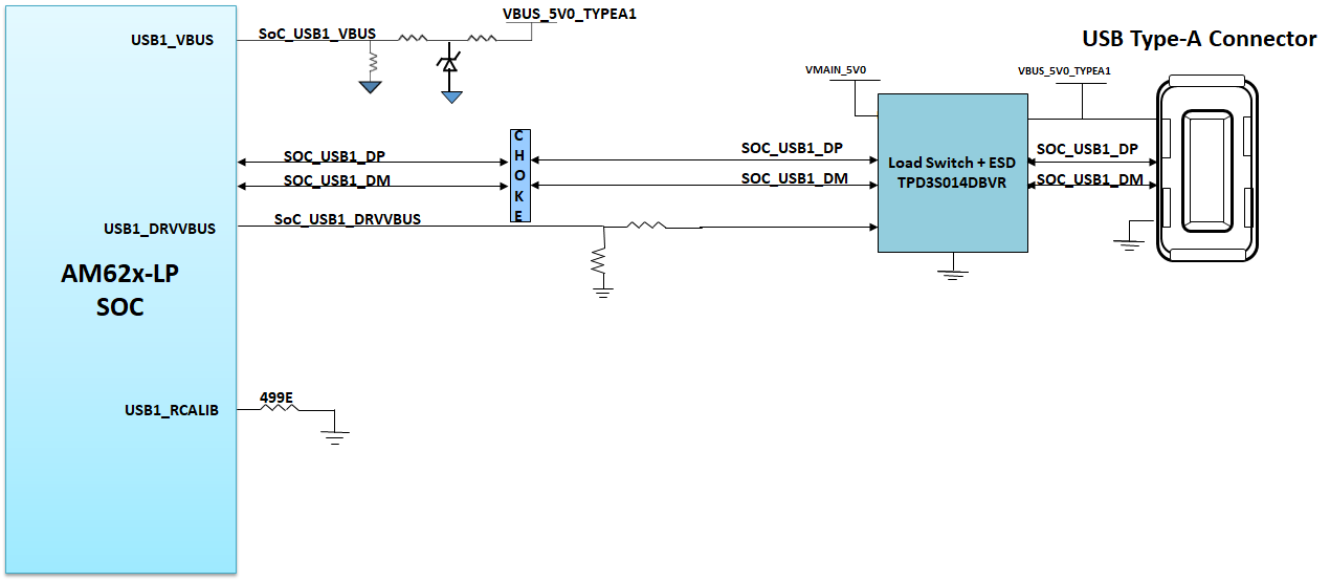


Figure 2-16. USB Type A Interface Block Diagram

2.14.2 USB2.0 Type-C Interface

On AM62x-Low Power SK EVM, USB 2.0 Interface is offered through USB Type-C™ connector J15 (manufacturer part number: 2012670005) which supports data rate up to 480Mbps. J15 is used for data communication and also as power connector. J15 is configured as a DRP port using PD controller TPS65988DHRSHR IC. So J15 can act as either the Host or Device. The role of the port depends on the type of the device getting connected on the connector and the ability to either sink or source. When the port is acting as DFP, the port can source up to 5V at 500mA.

USB2.0 Data lines DP and DM from J15 are connected to the USB0 interface of AM62X LOW POWER SoC using choke and ESD protection device. USB0_VBUS to the SOC is provided through a resistor divider network.

A common mode choke of DLW21SZ900HQ2B is provided on USB Data lines to take care of EMI and EMC. An ESD protection device of part number ESD122DMXR is included to dissipate ESD strikes on USB2.0 DP and DM signals. An ESD protection device of part number TPD1E01B04DPLT is included on CC signals and TVS2200DRVR IC is included on VBUS rail of Type-C Connector J15 to dissipate ESD strikes.

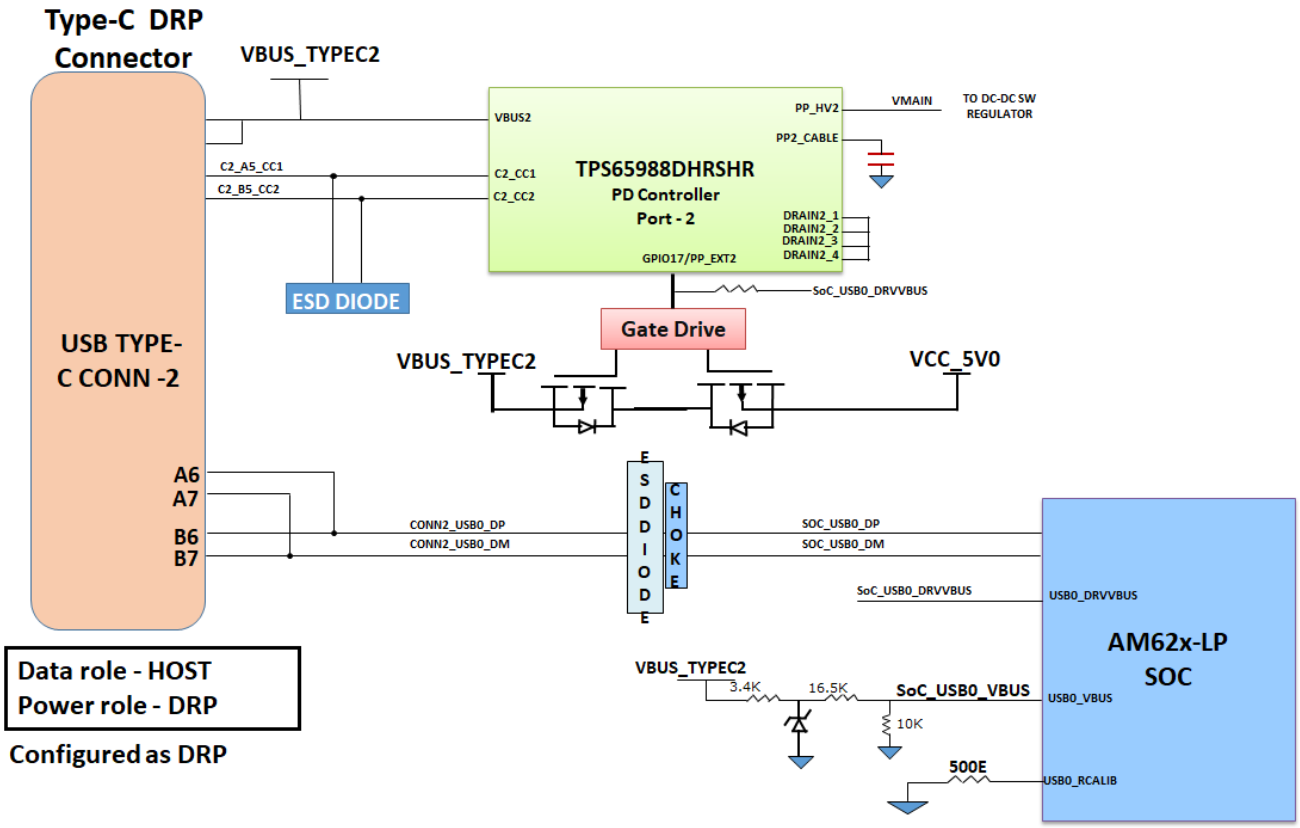


Figure 2-17. USB2.0 Type-C Interface Block Diagram

2.15 Memory Interfaces

2.15.1 LPDDR4 Interface

AM62x-Low Power SK EVM has 2GB, 16bit wide LPDDR4 memory with operating speed of up to 2133MT/s. The MT53E1G16D1FW-046 WT:A from Micron is used. This device uses two x8 8Gb Micron dies to make one x16 interface. The LPDDR memory is mounted on-board (single chip). The Placement and routing of LPDDR4 device is point to point.

The LPDDR4 requires 1.8V and thus reduces power demand. The devices require I/O power of 1.1V. LPDDR4 reset is an active low signal, which is controlled by SoC and the signal is pulled down to set the default active state. A footprint for pull-up is also provided.

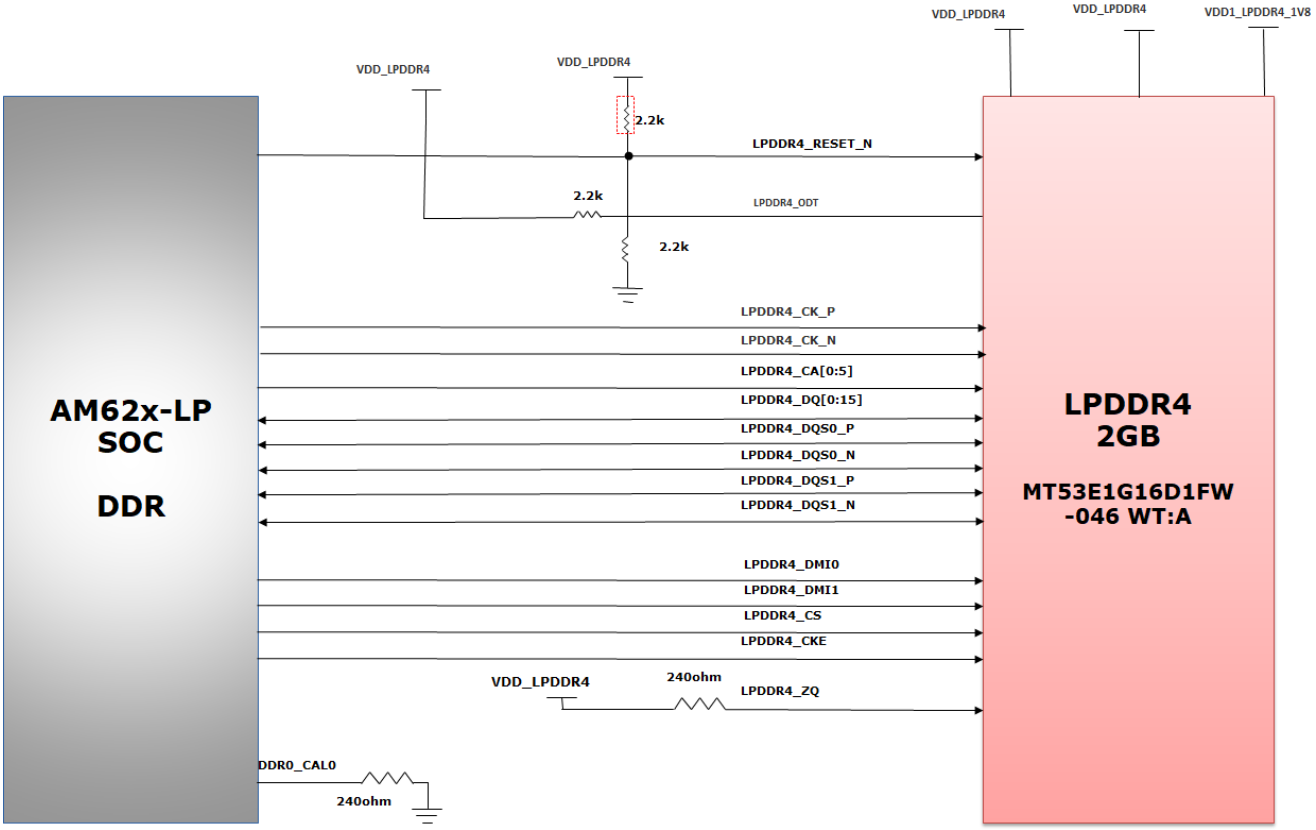


Figure 2-18. LPDDR4 Interface Block Diagram

2.15.2 OSPI

The AM62x Low-Power SK EVM board has a 1-Gbit OSPI memory device from Cypress part number W35N01JWTBAG which is connected to OSPI0 of the AM62x 17x17 SoC. OSPI supports single and double data rates with clock speeds up to 166Mhz STR and 120Mhz DTR.

OSPI & QSPI implementation: 0 ohm resistors are provided for DATA[7:0], DQS, INT# and CLK signals. Footprints to mount external pull up resistors are provided on DATA[7:0] to prevent bus floating. The footprint for the OSPI memory also allows the installation of either a QSPI memory or an OSPI memory. The 0 ohm series resistors provided for pins OSPI_DATA[4:7] will be removed if QSPI flash is to be mounted.

The reset for the OSPI flash is connected to a circuit that ANDs the RESETSTATz from the SoC with the signal GPIO_OSPI_RSTn from the SoC GPIO. This will apply reset for warm and cold reset. A pull-up is provided on GPIO_OSPI_RSTn coming from SoC pin to set the default active state.

The OSPI flash is powered by 1.8V IO supply. The 1.8V supply is provided to both VCC and VCCQ pins of the OSPI flash memory. OSPI of the SOC is powered by VDDSHV1 Power group of SoC and is connected to 1.8V IO supply.

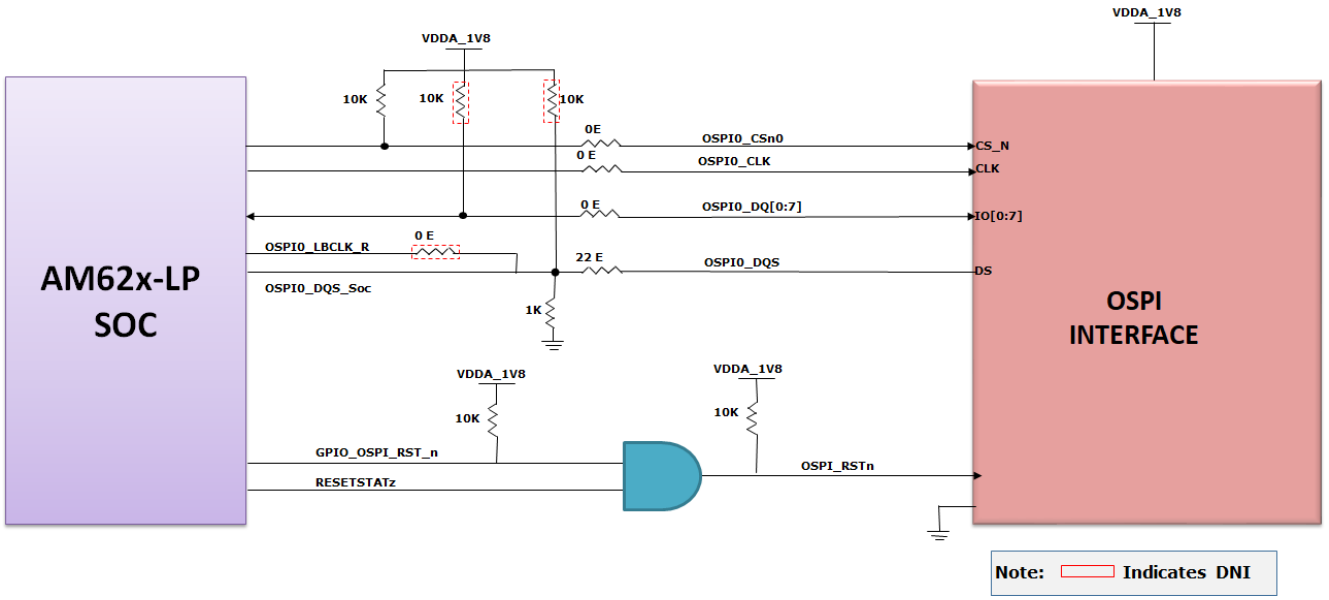


Figure 2-19. OSPI Block Diagram

2.15.3 MMC Interfaces

The AM62x 17x17 SoC has three MMC ports. MMC0 is connected to an eMMC flash, MMC1 is interfaced with Micro SD Socket on the board and MMC2 is connected to an optional M.2 module for WiFi and Bluetooth.

2.15.3.1 MMC0 - eMMC Interface

The AM62x-Low Power SK EVM board contains 16GB of eMMC flash memory from Micron part number MTFC16GAPALBH-IT connected to MMC0 port of the AM62X 17x17 SoC. The flash is connected to 8 bits of the MMC0 interface supporting HS400 double data rates up to 200MHz.

The eMMC device requires two power supplies, 3.3V for NAND memory and 1.8V for the eMMC interface. The MMC0 interface of the SOC is powered by the VDDSHV4 power domain, which is connected to 1.8V IO supply.

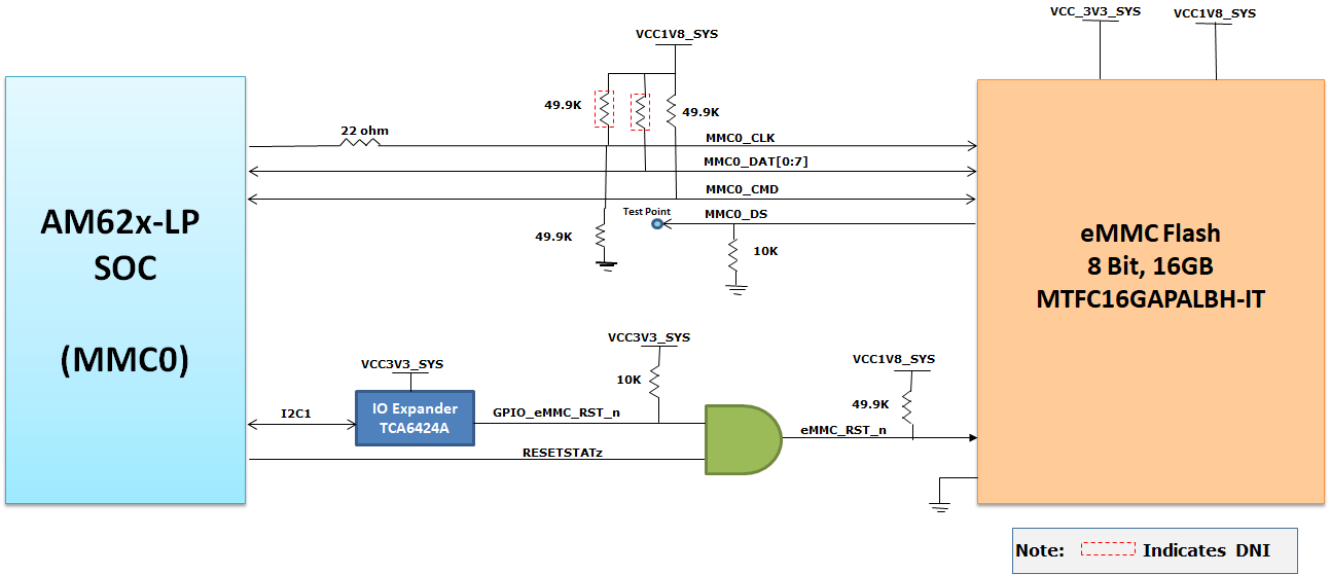


Figure 2-20. EMMC Interface Block Diagram

2.15.3.2 MMC1 - Micro SD Interface

The AM62x-Low Power SK EVM board provides a Micro SD™ card interface connected to the MMC1 port of the AM62x 17x17 SoC. The MicroSD card socket of MEM2051-00-195-00-A is used to interface with the MMC1 port of the AM62x 17x17 SoC. UHS1 operation is supported, including IO operations at both 1.8V and 3.3V. The Micro SD™ card interface is set to operate in SD mode by default. For high-speed cards, the ROM Code of the SOC tries to find the fastest speed that the card and controller can support and can have a transition to 1.8V.

The SD™ card connector power is provided using a load switch of TPS22918DBVR, which is controlled by ANDing the output of RESETSTATz, PORz_OUT and a GPIO from an IO Expander. An ESD protection device of part number TPD6E001RSE is provided for data, clock, and command signals. TPD6E001RSE is a line termination device with integrated TVS diodes providing system-level IEC 61000-4-2 ESD protection, ± 8kV contact discharge and ± 15kV air-gap discharge.

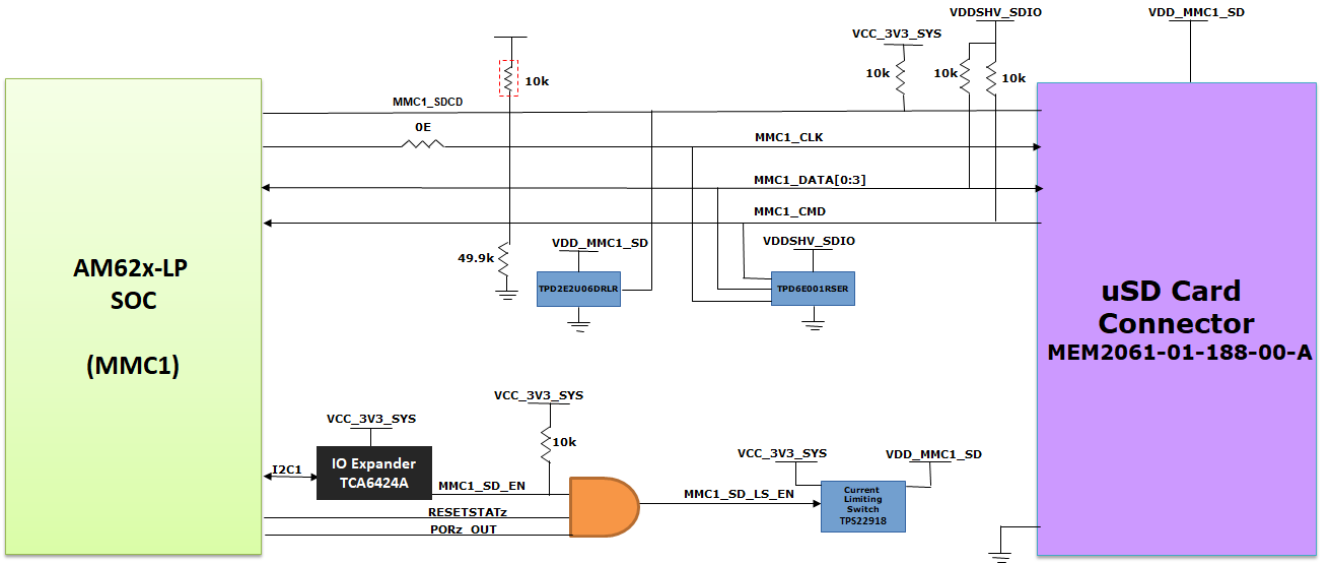


Figure 2-21. Micro SD Interface Block Diagram

2.15.3.3 MMC2 - M2 Key E Interface

The AM62x-Low Power SK EVM has an M.2 Key E interface for connecting WiFi BT modules connected to MMC2, UART2 instances and McASP1 interface through buffers. The M.2 module is connected to 4-bit IO of the MMC2 interface. The Module requires one power supply, 3.3V. Power to M.2 module is supplied from on-board power supply rails.

The MMC2 interface of the SoC is powered by the VDDSHV6 power domain, which is connected to 1.8V IO supply.

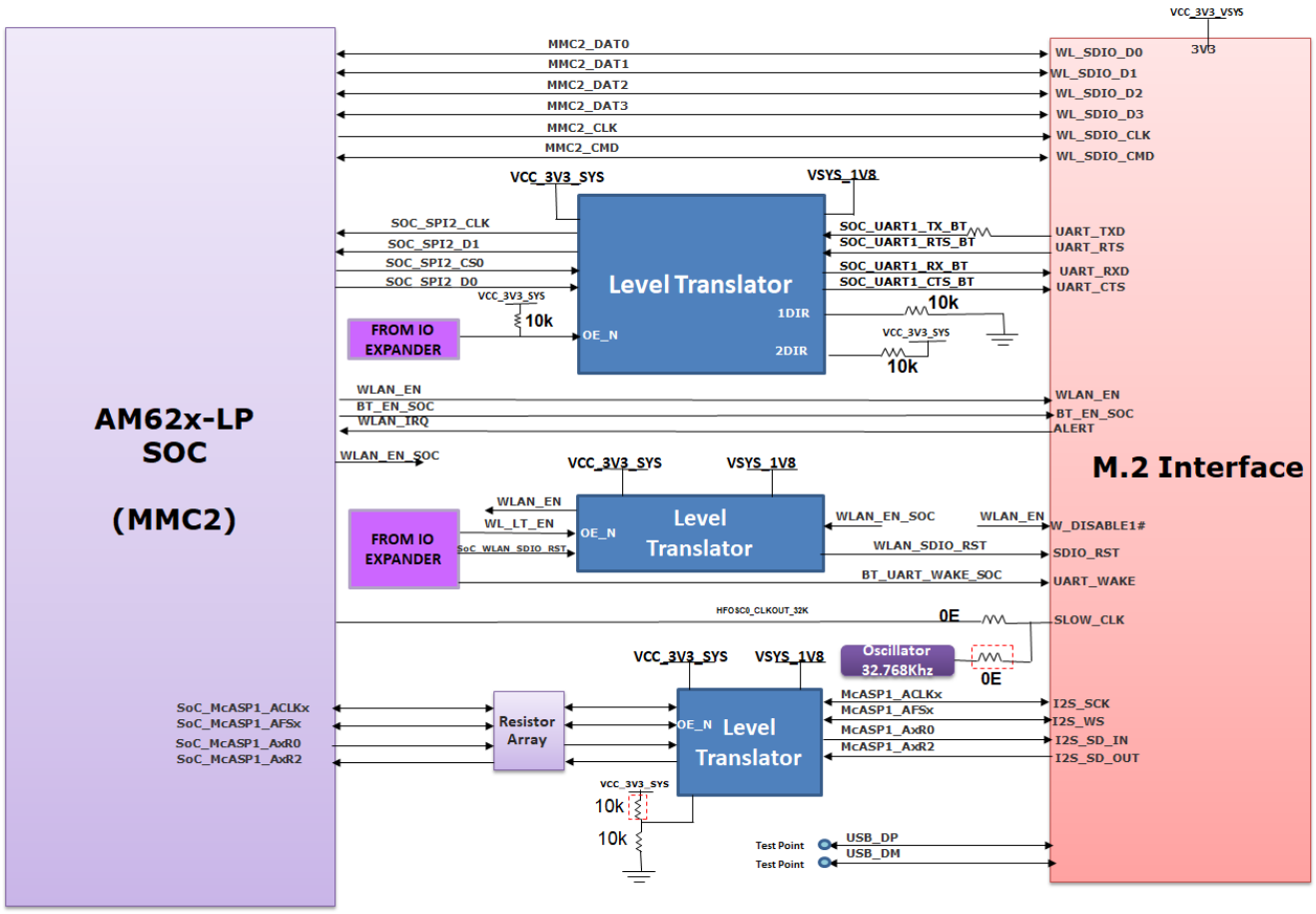


Figure 2-22. M.2 Interface Block Diagram

2.15.4 EEPROM

AM62x-Low Power SK EVM boards are identified by version and serial number, which are stored on the onboard EEPROM. The EEPROM is accessible from AM62x 17x17 SoC I2C0 port.

The Board ID EEPROM I2C address is set to 0x51. The AM62x-Low Power SK EVM includes an M24512-DFMC6TG 512kb EEPROM. The first 259 bytes of memory are preprogrammed with identification information for each board. The remaining 65277 bytes are available to the user for data or code storage.

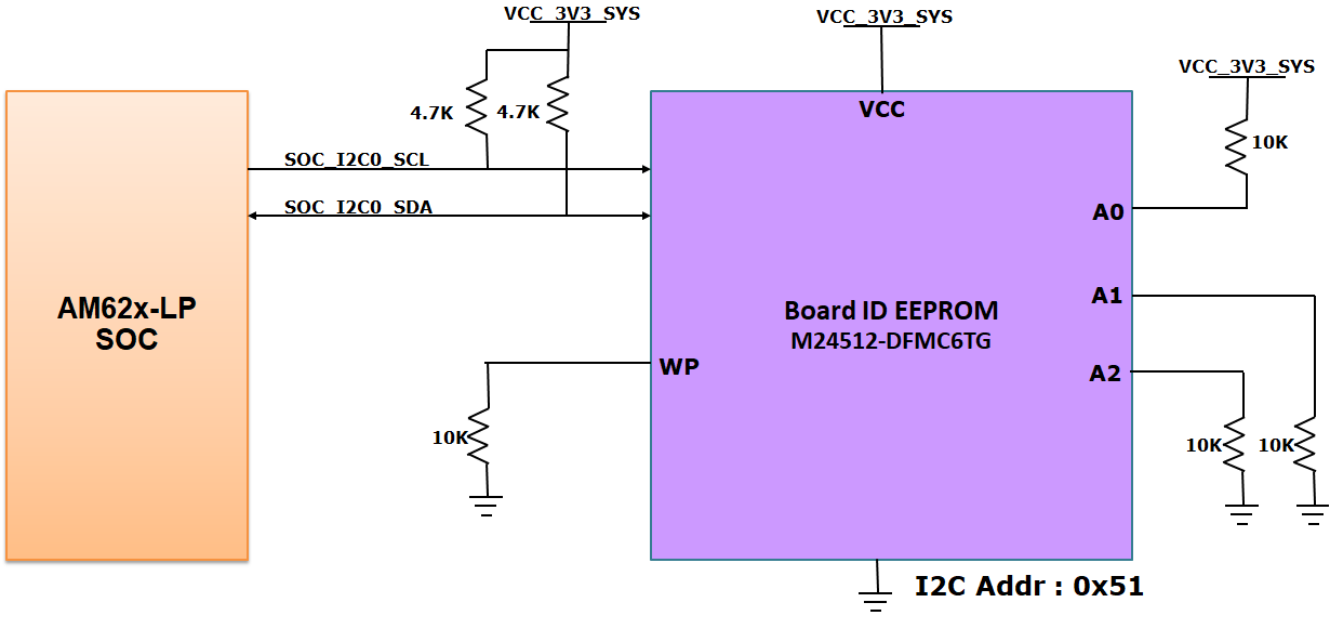


Figure 2-23. Board ID EEPROM Interface Block Diagram

2.16 Ethernet Interface

The AM62x-Low Power SK EVM offers two Ethernet Ports of 1 Gigabit Speed for external Communication. RGMII1 Gigabit Ethernet CPSW Port from AM62x 17x17 SOC is connected to the On-Board PHY Transceiver DP83867 while RGMII2 Gigabit Ethernet CPSW Port signals are terminated to a Board to Board connector providing flexibility of interfacing either to an optional daughter card. CPSW_RGMII1and CPSW_RGMII2 Ports share a common MDIO Bus to communicate with the external PHY Transceiver.

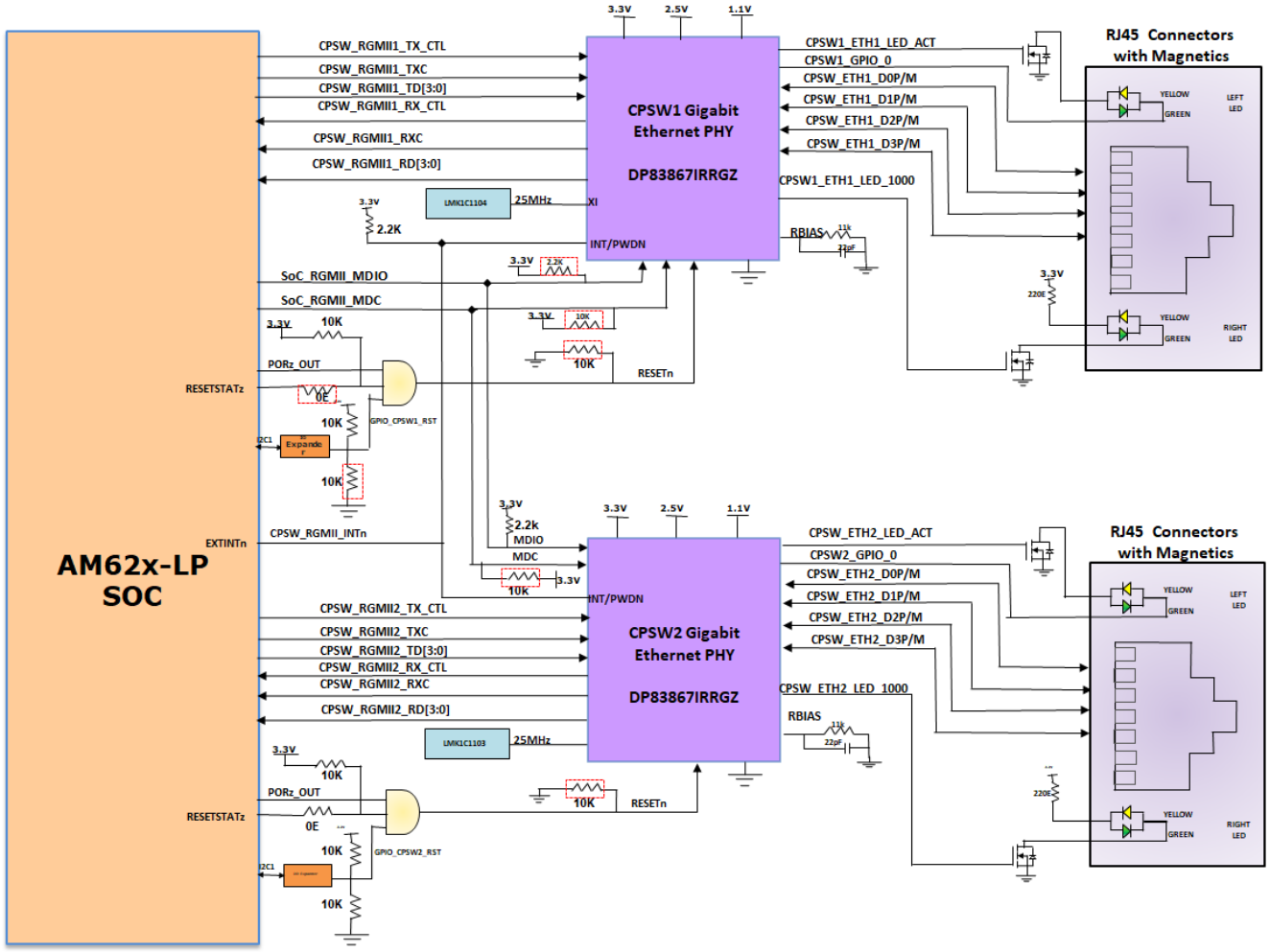


Figure 2-24. Ethernet Interface Block Diagram

2.16.1 CPSW Ethernet PHY1 Default Configuration

The default configuration of the DP83867 is determined using many resistor pull-up and pull-down values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes by using the pull up and pull down options provided. The AM62x-Low Power SK EVM uses the 48-pin QFN package which supports the RGMII interface.

The DP83867 PHY uses four level configurations based on resistor strapping which generate four distinct voltage ranges. The resistors are connected to the RX data and control pins which are normally driven by the PHY and are inputs to the processor. The voltage range for each mode is shown below:

- Mode1 – 0V to 0.3V
- Mode 2 – 0.462V to 0.6303V
- Mode3 – 0.7425V to 0.9372V
- Mode4 – 2.2902V to 2.9304V

Footprints for both pull-up and pull-down is provided on all the strapping pins except LED_0. LED_0 is for Mirror Enable, which is set to mode 1 by default, Mode 4 is not applicable and Mode2, Mode3 option is not desired.CPSW_RGMII1 port of the AM62X 17x17 SoC is connected to DP83867 with the configuration given below:

- PHY ADDR: 00000
- Auto_neg: Disabled
- ANG_sel: 10/100/1000
- RGMIIClk skew Tx: 0ns

- RGMIIClk skew Rx: 2ns

Table 2-15. CPSW Ethernet PHY–1 Strap values

Strap Setting	Pin Name	Strap Function	Mode	Value of Strap Function	Description
PHY Address	RX_D2	PHY_AD3	1	0	PHY Address: 0000
		PHY_AD2	1	0	
	RX_D0	PHY_AD1	1	0	
		PHY_AD0	1	0	
Auto Negotiation	RX_DV/ RX_CTRL	Auto- neg	3	0	Autoneg Disabled
Modes of Operation	LED2	RGMIIClock Skew TX[1]	5	0	RGMIITX Clock Skew is set to 0ns
		RGMIIClock Skew TX[0]	5	0	
	LED_1	RGMIIClock Skew TX[2]	5	1	
		ANEG_SEL	1	0	advertiseability of 10/100/1000
	LED_0	Mirror Enable	1	0	Mirror Enable Disabled
	GPIO_1	RGMIIClock Skew RX[2]	1	0	RGMIIRX Clock Skew is set to 2ns
		RGMIIClock Skew RX[1]	1	0	
	GPIO_0	RGMIIClock Skew RX[0]	1	0	

2.16.2 CPSW Ethernet PHY2 Default Configuration

CPSW_RGMII2 port of the AM62x 17x17 SoC is connected to DP83867 whose configuration is as given below.

Table 2-16. CPSW Ethernet PHY–2 Strap values

Strap Setting	Pin Name	Strap Function	Mode	Value of Strap Function	Description
PHY Address	RX_D2	PHY_AD3	1	0	PHY Address: 0001
		PHY_AD2	1	0	
	RX_D0	PHY_AD1	2	0	
		PHY_AD0	2	1	
Auto Negotiation	RX_DV/ RX_CTRL	Auto- neg	3	0	Autoneg Disabled
Modes of Operation	LED2	RGMII Clock Skew TX[1]	5	0	RGMIITX Clock Skew is set to 0ns
		RGMII Clock Skew TX[0]	5	0	
	LED_1	RGMII Clock Skew TX[2]	5	1	
		ANEG_SEL	1	0	advertise ability of 10/100/1000
	LED_0	Mirror Enable	1	0	Mirror Enable Disabled
	GPIO_1	RGMII Clock Skew RX[2]	1	0	RGMIIRX Clock Skew is set to 2ns
		RGMII Clock Skew RX[1]	1	0	
	GPIO_0	RGMII Clock Skew RX[0]	1	0	

The interrupts generated from two CPSW RGMII PHYs are tied together and is connected to EXTINTn pin of AM62x SoC.

LED_0is connected to RJ45 Right LED (Green) to indicate 1000MHz link (status).

LED_1is connected to RJ45 Left LED (Green) to indicate transmit/receive activity.

2.17 GPIO Port Expander

The AM62x-Low Power SK EVM uses a 24-Bit I2C based I/O expander for daughtercard plug-in detection, generating resets, and enable signals to various peripheral devices that are connected to the expander. The SoC_I2C1 bus of the AM62X 17x17 SoC is used to interface with the I/O expanders. The I2C device address of the I/O expander is 0x21 and 0x23. Table 2-17 lists the signals that the expander control.

Table 2-17. IO Expander 1 Signal Details

IO EXPANDER - 01			
PIN NUMBER	**SIGNAL**	**DIRECTION**	**DEVICE**
P11	GPIO_EMMC_RSTN	OUTPUT	eMMC Reset control GPIO
P01	GPIO_CPSW1_RST	OUTPUT	CPSW Ethernet PHY-1 Reset Control GPIO
P00	GPIO_CPSW2_RST	OUTPUT	CPSW Ethernet PHY-2 Reset Control GPIO
P03	MMC1_SD_EN	OUTPUT	SD Card Load Switch Enable
P04	VPP_LDO_EN	OUTPUT	SOC eFuse Voltage(VPP=1.8V) Regulator Enable
P05	EXP_PS_3V3_EN	OUTPUT	EXP CONN 3.3V Power Switch Enable
P06	EXP_PS_5V0_EN	OUTPUT	EXP CONN 5V Power Switch Enable
P10	GPIO_AUD_RSTN	OUTPUT	Audio Codec Reset Control GPIO
P07	EXP_HAT_DETECT	INPUT	EXP CONN HAT Board Detection
P02	PRU_DETECT	INPUT	PRU Board Detection
P12	UART1_FET_BUF_EN	OUTPUT	SOC UART1 Mux Select
P13	BT_UART_WAKE_SOC	INPUT	BT UART WKUP Signal
P14	GPIO_HDMI_RSTN	OUTPUT	HDMI Transmitter Reset Control GPIO
P15	CSI_GPIO0	NA	Raspberry Pi Camera CSI0 GPIO1
P16	CSI_GPIO1	NA	Raspberry Pi Camera CSI0 GPIO2
P17	GPIO_OLDI_INT	INPUT	OLDI Interrupt
P20	HDMI_INTN	INPUT	HDMI Interrupt
P21	TEST_GPIO2	INPUT	TEST GPIO2 from Test Automation Connector
P22	MCASP1_FET_EN	OUTPUT	MCASP1 Enable and Direction Control
P23	MCASP1_BUF_BT_EN	OUTPUT	
P24	MCASP1_FET_SEL	OUTPUT	
P25	UART1_FET_SEL	OUTPUT	
P27	IO_EXP_TEST_LED	OUTPUT	User Test LED 2

Table 2-18. IO Expander 2 Signal Details

IO EXPANDER - 02			
Pin no	**SIGNAL**	**DIRECTION**	**DEVICE**
P20	SPI0_FET_SEL	OUTPUT	SoC SPI0 MUX Selection
P21	SPI0_FET_OE	OUTPUT	SoC SPI0 MUX Enable

Table 2-18. IO Expander 2 Signal Details (continued)

IO EXPANDER - 02			
Pin no	**SIGNAL**	**DIRECTION**	**DEVICE**
P22	GPIO_OLDI_RSTn	OUTPUT	OLDI Reset
P23	PRU_3V3_EN	OUTPUT	PRU Power Switch Enable
P26	CSI_VLDO_SEL	OUTPUT	CSI Regulator Enable (VCC_CSI_IO)
P27	SOC_WLAN_SDIO_RST	OUTPUT	WLAN Reset control GPIO
P10	WL_LT_EN	OUTPUT	Wilink Enable
P11	CSI_RSTZ	OUTPUT	CSI Reset control GPIO

2.18 GPIO Mapping

The table below describes the detailed GPIO mapping of AM62x 17x17 SoC with AM62x-Low Power SK EVM peripherals

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN	VOLTAGE CONNECTED
									ON SOC SIDE	ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_0	MCU_SPI0_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt PRU Connector Interrupt	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	SoC_DVDD3V3
7	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	SoC_DVDD3V3
8	PMIC Interrupt	PMIC_INT_B	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV3	SoC_DVDD3V3
9	IO Expander Interrupt									
10	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button		INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
11	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	CAN_FD_WKUP_SW signal from switch	ETH_CAN_INH_SOC	INTERRUPT	MCU_GPIO0_19	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
13	CAN_FD_WKUP_HDR_INH signal from header									
14	User EXP Conn GPIO	EXP_GPIO1_22	GPIO	GPIO1_22	UART0_CTSn	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
16	User Interrupt									
17	User EXP Conn GPIO	EXP_GPIO0_14_LT	GPIO	GPIO0_14	OSPI0_CSn3	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
18	PMIC Standby Enable	PMIC_STBY	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	HIGH	HIGH	VDDSHV_CANUART	SoC_DVDD3V3
19	User EXP Conn GPIO	EXP_EHRPWM1_B	GPIO	GPIO1_10	MCASP0_AXR0	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
				IO EXPANDER - 01						
1	eMMC Reset control GPIO	GPIO_EMMC_RSTN	RESET	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P00		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	LOW		VCC_3V3_SYS
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER-P04		OUTPUT	LOW	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P06		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	Audio Codec Reset Control GPIO	GPIO_AUD_RSTN	RESET	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
10	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER-P02		INPUT	HIGH	LOW		VCC_3V3_SYS
11	SOC UART1 Mux Select	UART1_FET_BUF_EN	SELECT	IO EXPANDER-P12		OUTPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTN	RESET	IO EXPANDER-P14		OUTPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		NA	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		NA	NA	NA		VCC_3V3_SYS
16	OLDI Interrupt	GPIO_OLDI_INT	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTN	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		INPUT	HIGH	LOW		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
22		UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
23	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
				IO EXPANDER - 02						
1	SoC SPI0 MUX Selection	SPI0_FET_SEL	ENABLE	IO EXPANDER-P20		OUTPUT	LOW	HIGH		VCC_3V3_SYS
2	SoC SPI0 MUX Enable	SPI0_FET_OE	CONTROL	IO EXPANDER-P21		OUTPUT	LOW	LOW		VCC_3V3_SYS
3	OLDI Reset	GPIO_OLDI_RSTn	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
5	CSI Regulator Enable (VCC_CSI_IO)	CSI_VLDO_SEL	ENABLE	IO EXPANDER-P26		OUTPUT	LOW	HIGH		VCC_3V3_SYS
6	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	Wilink Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	CSI Reset control GPIO	CSI_RSTZ	RESET	IO EXPANDER-P11		OUTPUT	LOW	HIGH		VCC_3V3_SYS

2.19 AM62x-Low Power SK EVM User Setup and Configuration

2.19.1 EVM DIP Switches

AM62x-Low Power SK EVM has two 8 - position DIP Switch to set the SoC Boot mode and related parameters.

2.19.2 Boot Modes

The boot mode for the AM62x-Low power SK EVM board is defined by two banks of switches SW3 and SW4 or by the I2C buffer connected to the Test automation connector. This allows for AM62x SoC Boot mode control by either the user (DIP Switch Control) or by the Test Automation connector.

All the bits of switch (SW3 and SW4) have week pull down resistor and a strong pull up resistor as shown in below picture. Note that OFF setting provides a low logic level (‘0’) and an ON setting provides a high logic level (‘1’).

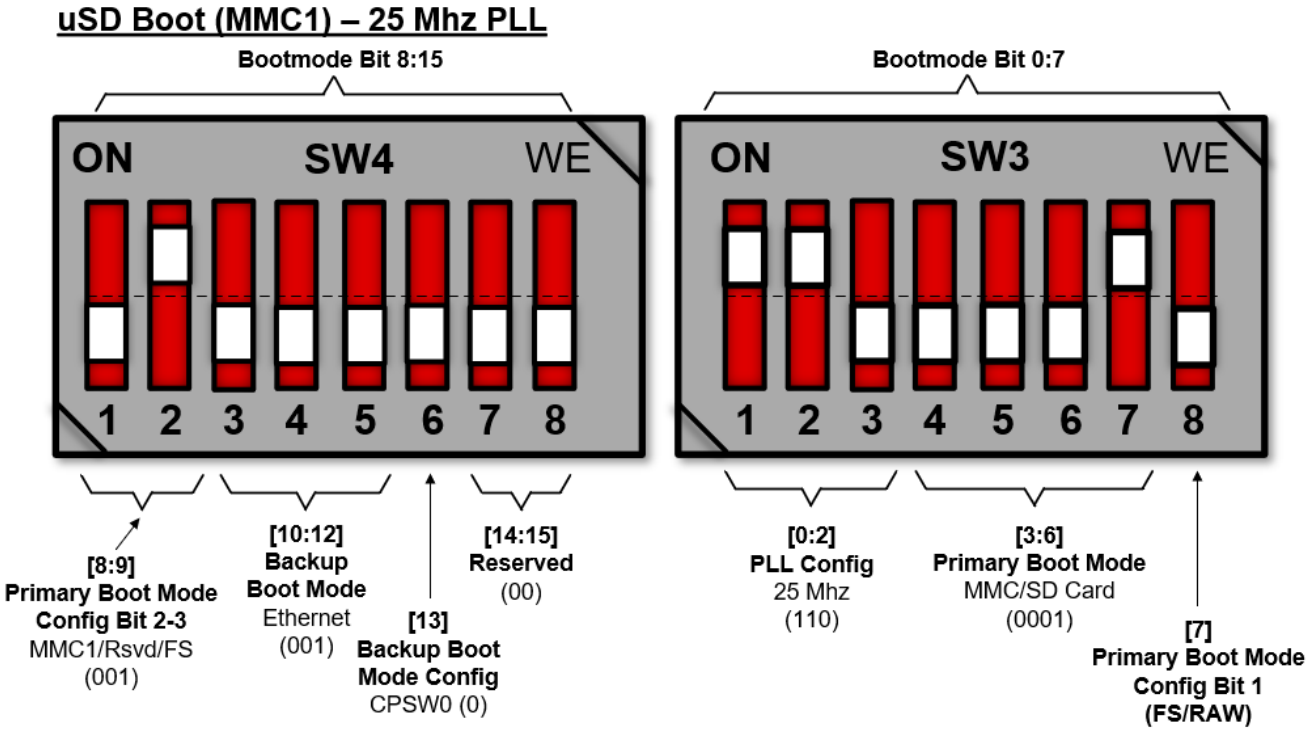


Figure 2-25. Boot Mode Switch Example

The boot mode pins of the SoC have associated alternate functions during normal operation. Hence isolation is provided using Buffer IC’s to cater for alternate pin functionality. The output of the buffer is connected to the bootmode pins on the AM62x Low Power SK EVM. The output is enabled when the bootmode is needed during a reset cycle.

The input to the buffer is connected to the DIP switch circuit and to the output of an I2C buffer set by the test automation circuit. If the test automation circuit is going to control the bootmode, all the switches will manually be set to the OFF position. Keep the bootmode buffer powered by an always ON power supply so that the bootmode remains present even if the SoC power is cycled.

Switch SW1 and SW2 bits [15:0] are used to set the SoC Boot mode.

The switch map to the boot mode functions is provided in the tables below.

Table 2-19. Boot Mode Pin Mapping

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Backup Boot Mode Configuration	Backup Boot Mode			Primary Boot Mode Configuration			Primary Boot Mode				PLL Configuration		

BOOT-MODE[0:2] – Denote system clock frequency for PLL configuration. By default this bits are set for 25MHz.

Table 2-20. PLL Reference Clock Selection

SW3.3	SW3.2	SW3.1	PLL REF CLK (MHz)
OFF	OFF	OFF	RSVD
OFF	OFF	ON	RSVD
OFF	ON	OFF	24

Table 2-20. PLL Reference Clock Selection (continued)

SW3.3	SW3.2	SW3.1	PLL REF CLK (MHz)
OFF	ON	ON	25
ON	OFF	OFF	26
ON	OFF	ON	RSVD
ON	ON	OFF	RSVD
ON	ON	ON	RSVD

BOOT-MODE [3:6] – This provides primary boot mode configuration to select the requested boot mode after POR, that is, the peripheral/memory to boot from primary boot device selection details.

Table 2-21. Boot Device Selection BOOT-MODE [6:3]

SW3.7	SW3.6	SW3.5	SW3.4	Primary Boot Device Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	Ethernet RGMII1
OFF	ON	OFF	ON	Ethernet RMII1
OFF	ON	ON	OFF	I2C
OFF	ON	ON	ON	UART
ON	OFF	OFF	OFF	MMC/SD card
ON	OFF	OFF	ON	eMMC
ON	OFF	ON	OFF	USB0
ON	OFF	ON	ON	GPMC NAND
ON	ON	OFF	OFF	GPMC NOR
ON	ON	OFF	ON	Rsvd
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	No boot/Dev Boot

BOOT-MODE [9:7] – These pins provide optional settings and are used in conjunction with the primary boot device selected.

Table 2-22. Primary Boot Mode Configuration[9:7]

SW4.2 (B9)	SW4.1 (B8)		SW3.8 (B7)		Primary Boot Mode
RVSD	Read Mode2	0: RSVD (Read mode is taken from Read Mode 1)	Read Mode1	0: OSPI/ 1-1-8 Mode (valid only when Read Mode 2 is 0)	Serial NAND
		1: SPI/ 1-1-1 Mode (Read mode is taken from Read Mode 2 and Read Mode 1 is ignored)		1: OSPI/ 1-1-4 Mode (valid only when Read Mode 2 is 0)	
RVSD	Iclk	0: Iclock source external	Csel	0: Boot Flash is on CS 0	OSPI
		1: Iclock source internal (pad loopback)		1: Boot Flash is on CS 1	
RVSD	Iclk	0: Iclock source external	Csel	0: Boot Flash is on CS 0	QSPI
		1: Iclock source internal (pad loopback)		1: Boot Flash is on CS 1	
RVSD	Mode	0: SPI Mode 0	Csel	0: Boot Flash is on CS 0	SPI
		1: SPI Mode 3		1: Boot Flash is on CS 1	

Table 2-22. Primary Boot Mode Configuration[9:7] (continued)

SW4.2 (B9)		SW4.1 (B8)		SW3.8 (B7)		Primary Boot Mode
0		0		Link stat	0: Phy scan used for speed/ duplex setup	RGMII1
					1: RGMII status register used for speed/ duplex setup	
CLKOUT	0: 50MHz clock not generated on CLKOUT0	CLK SRC	0: External clock source	0		RMII1
	1: 50MHz clock generated on CLKOUT0		1: Internal clock source			
Bus reset	0: Hung bus reset attempt after 1ms	RSVD		Addr	0: 0x50	I2C0
	1: No hung Bus reset attempted				1: 0x51	
RSVD		RSVD		RSVD		UART0
1		RSVD		Fs/Raw	0: FileSystem Mode	MMC/SD Card
					1: Raw Mode	
RSVD		RSVD		RSVD		eMMC
Core Volt	0: 0.85V Core Voltage	Mode	0: DFU(Device)	Lane Swap	0: No swapping of DP/DM	USB
	1: 0.75V Core Voltage		1: MSC(Host)		1: DP/DM is swapped	
RSVD		RSVD		RSVD		GPMC NAND
RSVD		RSVD		RSVD		GPMC NOR
RSVD		RSVD		RSVD		RSVD
SFDP	0: SFDP disabled	Read Cmd	0: 0x0B Read Command	Mode	0: 1S-1S-1S mode at 50MHz	xSPI
	1: SFDP enabled		1: 0xEE Read Command		1:8D-8D-8D mode at 25MHz	
RSVD		ARM/ Thumb	0: ARM mode	No/Dev	0: Development Boot	No-boot/Dev boot
			1: Thumb mode		1: No Boot	

• BOOT-MODE [10:12] – Select the backup boot mode, used when the primary boot mode is not available.

Table 2-23. Backup Boot Mode Selection BOOT-MODE [12:10]

SW4.5	SW4.4	SW4.3	Backup Boot Device Selected
OFF	OFF	OFF	None (No backup mode)
OFF	OFF	ON	USB
OFF	ON	OFF	Reserved
OFF	ON	ON	UART
ON	OFF	OFF	Ethernet
ON	OFF	ON	MMC/SD
ON	ON	OFF	SPI
ON	ON	ON	I2C

BOOT-MODE[13] – These pins provide optional settings and are used in conjunction with the backup boot device devices. Switch SW4.6 when ON sets 1 and sets 0 if OFF, see the device-specific TRM.

BOOT-MODE [14:15] – Reserved. Provides backup boot media configuration options.

Table 2-24. Backup Boot Mode Configuration BOOTMODE[13]

SW4.6 (B13)		Backup Boot Mode	Defaulted Values for Back up Boot Mode
RSVD		None	
Mode	0: DFU (Device)	USB	Core Volt bit = 0 Lane Swap bit = 0
	1: MSC(Host)		

Table 2-24. Backup Boot Mode Configuration BOOTMODE[13] (continued)

SW4.6 (B13)		Backup Boot Mode	Defaulted Values for Back up Boot Mode
RSVD		RSVD	
RSVD		UART	
Interface	0: RGMII with internal Delay	Ethernet	Link Stat bit = 0 (If RGMII)
	1: RGMII with external clock source		ClkOut bit= 0 and Clksrc bit = 1 (If RMII)
1		MMC	Mode bit = 0
RSVD		SPI	Csel bit = 0 Mode = 0
RSVD		I2C	Addr = 0 Bus Rest = 0

2.19.3 User Test LEDs

The AM62x-Low Power SK EVM contains two LEDs for user defined functions.

Table 2-25 lists the user test LEDs and the associated GPIOs used to control the LEDs.

Table 2-25. User Test LEDs

SI Number	LED	GPIO used	SCH Net Names
1	LD3	GPIO1_49	SOC_GPIO1_49
2	LD7	U70.24(P27)	IO_EXP_TEST_LED

2.20 Expansion Headers

The AM62x-Low Power SK EVM features three expansion headers: the 40 pin User expansion connector, 20 pin PRU Header and the 28 pin MCU Header.

2.20.1 User Expansion Connector

The AM62x-Low Power SK EVM supports RPi expansion interface using a 40-pin User expansion connector (manufacturer part number: PEC20DAAN. Four mounting holes must be oriented with the connector to allow for connection of these boards.

The following interfaces and IOs are included on to the 40-pin User Expansion connector.

- 2x SPI: SPI0 with 2 CS and SPI2 with 3 CS
- 2x I2C: SoC_I2C0 and SoC_I2C2
- 1x UART: UART5
- 2x PWM: EHRPWM0_A, EHRPWM1_B1xCLK: CLKOUT0
- 10x GPI0: GPIOs from main domain
- 5V and 3.3V supply (current limited to 155mA and 500mA)

Each of the power supplies 5V and 3.3V are current limited to 155mA and 500mA respectively. This is achieved by using two individual load switches TPS22902YFPR and TPS22946YZPR. The Enable signals for the load switches is driven through the I2C-based GPIO port expander.

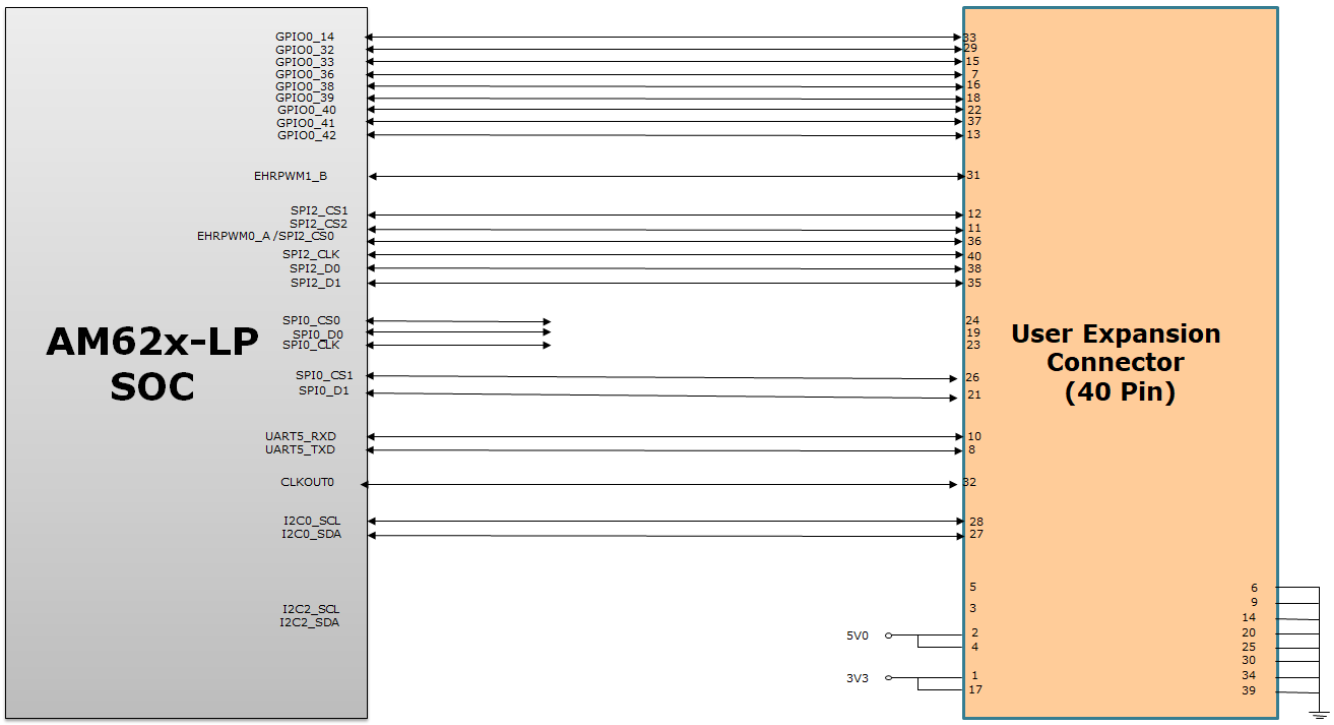


Table 2-26. 40 Pin User Expansion Connector (J3)

Pin Number	SoC Ball	Net name	Comments
1	-	VCC3V3_EXP	
2	-	VCC5V0_EXP	
3	H19	EXP_I2C2_SDA	I2C SW
4	-	VCC5V0_EXP	
5	H18	EXP_I2C2_SCL	I2C SW
6	-	DGND	
7	C14	EXP_CLKOUT0	
8	A15	EXP_UART5_TXD	
9	-	DGND	
10	B13	EXP_UART5_RXD	
11	C17	EXP_SPI2_CS1	
12	D15	EXP_SPI2_CS0/EHRPWM0_A	MUX
13	H17	EXP_GPIO0_42	
14	-	DGND	
15	-	EXP_GPIO0_22	
16	P17	EXP_GPIO0_38	
17	-	VCC3V3_EXP	
18	J20	EXP_GPIO0_39	
19	C12	EXP_SPI0_D0	
20	-	DGND	
21	A14	EXP_SPI0_D1	
22	E18	EXP_GPIO0_14	
23	D12	EXP_SPI0_CLK	
24	C11	EXP_SPI0_CS0	
25	-	DGND	
26	D13	EXP_SPI0_CS1	
27	D14	SoC_I2C0_SDA	

Table 2-26. 40 Pin User Expansion Connector (J3) (continued)

Pin Number	SoC Ball	Net name	Comments
28	E12	SoC_I2C0_SCL	
29	K18	EXP_GPIO0_36	
30	K20	EXP_GPIO0_32	
31	K21	EXP_GPIO0_33	
32	J19	EXP_GPIO0_40/ PR0_ECAP0_IN_APWM_OUT	
33	D18	EXP_EHRPWM1_B	
34	-	DGND	
35	B17	EXP_SPI2_D1/ ECAP2_IN_APWM_OUT	MUX
36	A18	EXP_SPI2_CS2	
37	J18	EXP_GPIO0_41	
38	B18	EXP_SPI2_D0	MUX
39	-	EXP_HAT_DETECT	
40	D16	EXP_SPI2_CLK	MUX

2.20.2 MCU Connector

The AM62x-Low Power SK EVM has a 14x2 standard 0.1 spaced MCU connector which includes signals connected to the MCU Domain of SoC. 13 Signals include MCU_I2C0, MCU_UART0 (with flow control), MCU_SPI0 and MCU_MCAN0 signals are connected to the MCU Header. Additional control signals provided on the Header include CONN_MCU_RESETz, CONN_MCU_PORz, MCU_RESETSTATz, MCU_SAFETY_ERRORn, 3.3V IO and GND. MCU_UART0 signals from AM62x SoC are connected to both MCU Header and FT4232 Bridge through MUX (manufacturer part number: SN74CB3Q3257PWR). The MCU Header does not include the Board ID memory interface. Allowed current limit is 100mA on 3.3V rail.

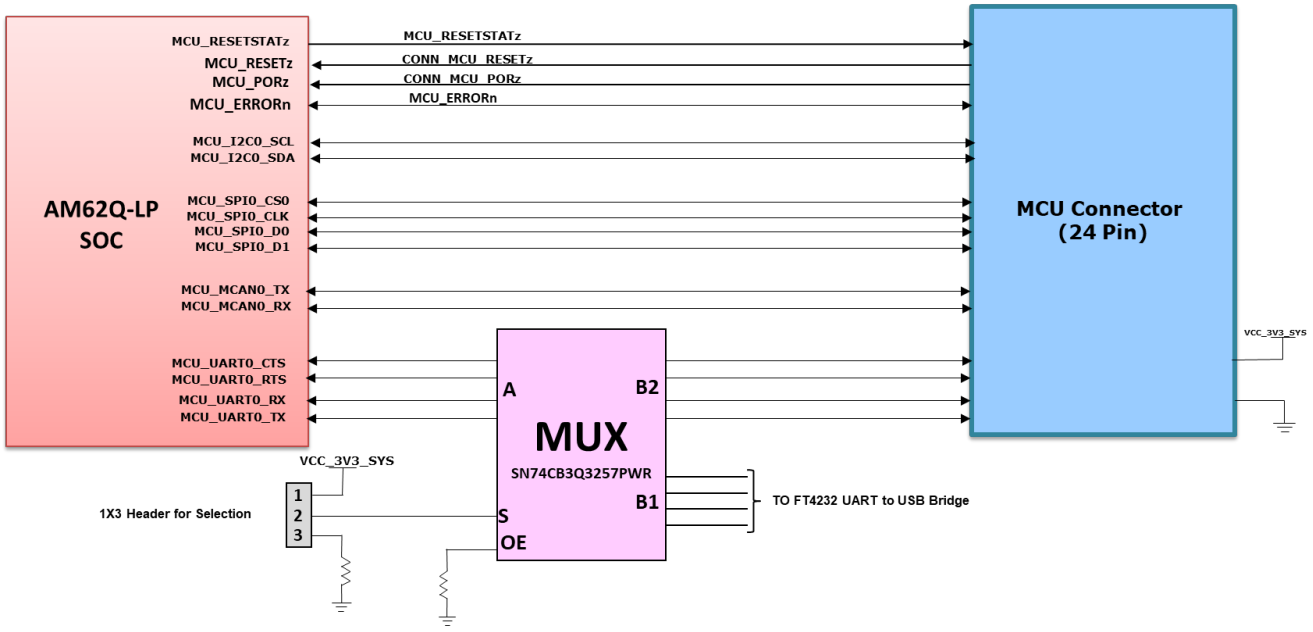


Figure 2-26. MCU Connector Interface

Table 2-27. MCU Connector (J10) Pinout

Pin Number	SoC Ball Number	Netname
1	-	VCC_3V3_SYS
2	-	DGND
3	-	DGND

Table 2-27. MCU Connector (J10) Pinout (continued)

Pin Number	SoC Ball Number	Netname
4	D8	MCU_SPI0_D1
5	-	CAN_FD_WKUP_HDR_INH
6	E8	MCU_SPI0_D0
7	-	DGND
8	C8	MCU_SPI0_CS1
9	-	DGND
10	D5	MCU_GPIO0_15
11	D6	MCU_GPIO0_16
12	B8	MCU_UART0_CTS_CONN
13	A8	MCU_UART0_RXD_CONN
14	-	DGND
15	-	DGND
16	C5	MCU_MCAN0_TX
17	D7	MCU_UART0_RTS_CONN
18	B7	MCU_SPI0_CLK
19	B6	MCU_UART0_TXD_CONN
20	-	DGND
21	A10	MCU_I2C0_SDA
22	C4	MCU_MCAN0_RX
23	A12	MCU_RESETSTATz
24	B9	MCU_I2C0_SCL
25	-	CONN_MCU_RESETz
26	-	MCU_SAFETY_ERRORz_3V3
27	-	DGND
28	-	CONN_MCU_PORz

2.20.3 PRU Connector

The AM62x-Low Power SK EVM has a 20 pin PRU Header which offers a low speed connection to the PRG0 Interface using a connector manufacturer Part # PREC010DAAN-RC. The connector features PR0_PRU0_GPO [0: 7], SoC_I2C0, +3.3V PRU_ICSSG signals from PRG0 Port (PRG0_PRU0) are connected to a 10x2 standard 0.1” spaced Receptacle PWR and Ground reference. INTn signal from PRU Header is wired along with the CPSW PHY interrupts and connected to the EXTINTn pin of the SoC.

The 3.3V supply is current limited to 500mA. This is achieved by using load switch TPS22902YFPR. Enable for the load switch is controlled by IO expander. Signals routed from the PRU Connector are listed in Table 2-28.

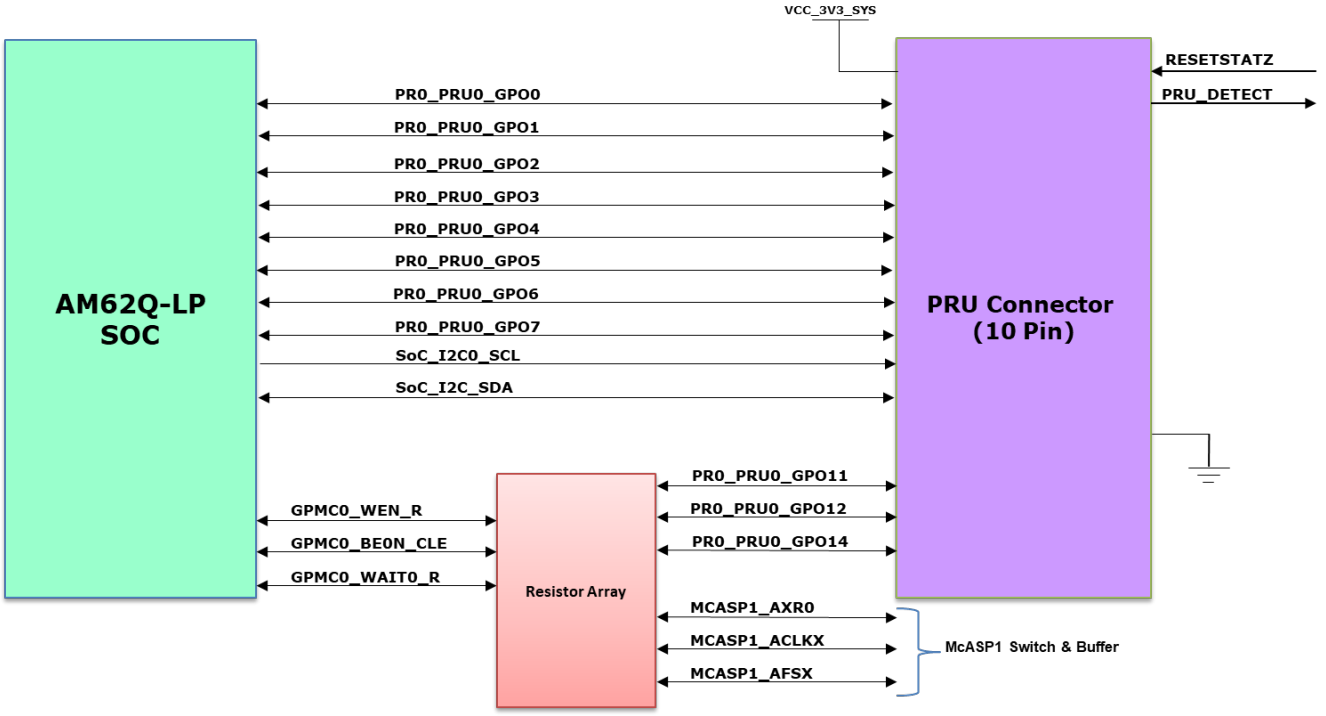


Figure 2-27. PRU Connector Interface

Table 2-28. PRU Header (J11) Pinout

Pin Number	SoC Ball Number	Net name
1	-	VCC3V3_PRU
2	-	DGND
3	-	PRU_DETECT
4	-	PRU_RESETz
5	B16	PRU_INTn
6	E12	SoC_I2C0_SCL
7	J17	PR0_PRU0_GPO11
8	D14	SoC_I2C0_SDA
9	P21	PR0_PRU0_GPO12
10	-	NC
11	K17	PR0_PRU0_GPO14
12	-	NC
13	K19	PR0_PRU0_GPO0
14	L19	PR0_PRU0_GPO1
15	L20	PR0_PRU0_GPO2
16	L21	PR0_PRU0_GPO3
17	M21	PR0_PRU0_GPO4
18	L17	PR0_PRU0_GPO5
19	L18	PR0_PRU0_GPO6
20	M20	PR0_PRU0_GPO7

2.21 Push Buttons

AM62x-Low Power SK EVM supports two interrupts for providing Reset input and User Interrupt to the processor. The interrupts are push buttons placed on the Top side of the Board and are listed in the table below.

Table 2-29. EVM Push Buttons

Sl #	Push Buttons	Signal	Function
1	SW5	SoC_WARM_RESETZ	Main domain Warm Reset input
2	SW6	GPIO_MCU	Generates interrupt on MCU_GPIO0_15

2.22 I2C Address Mapping

There are three I2C interfaces used in AM62x-Low Power SK EVM board.

- SoC_I2C0 Interface: SoC I2C [0] is connected to Board ID EEPROM, User Expansion Connector Header, USB PD controller, PRU header, PMIC and OLDI Display Touch interface.
- SOC I2C1 Interface: SoC I2C [1] is connected to Test Automation Header, Current Monitors, Temperature Sensors, Audio Codec, HDMI Transmitter, , GPIO Port Expander.
- SOC I2C2 Interface: Soc I2C [2] is Connected to the User Expansion Connector Header and CSI Camera Connector.
- MCU I2C0 Interface: MCU I2C [0] is Connected to MCU Header.

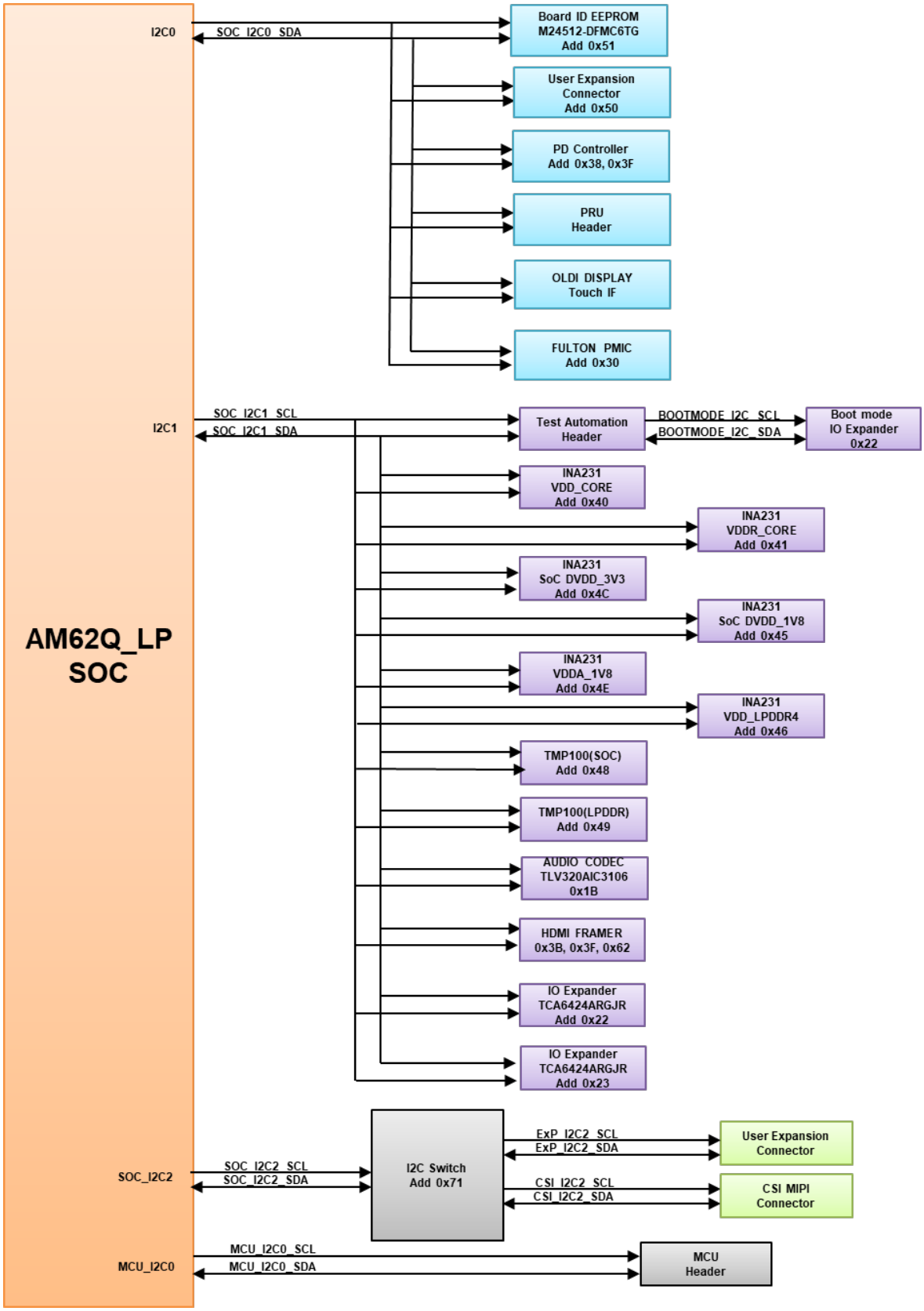


Figure 2-28. I2C Interface Block Diagram

Table 2-30. I2C Mapping Table

I2C Port	Device/Function	part number	I2C Address
SoC_I2C0	Board ID EEPROM	M24512-DFMC6TG	0x51
SoC_I2C0	User Expansion Connector	<connector interface>	
SoC_I2C0	USB PD Controller	TPS65988DHRSHR	0x38, 0x3F
SoC_I2C0	PRU Header	<connector interface>	
SoC_I2C0	OLDI Display Touch Interface	<connector interface>	
SoC_I2C1	PMIC	TPS65219	0x30
SoC_I2C1	Test Automation Header	<connector interface>	
SoC_I2C1	Current Monitors	INA231AIYFDR	0x40, 0x41, 0x4C, 0x45, 0x4E & 0x46
SoC_I2C1	Temperature Sensors	TMP100NA/3K	0x48, 0x49
SoC_I2C1	Audio Codec	TLV320AIC3106IRGZT	0x1B
SoC_I2C1	HDMI Transmitter	SiI9022ACNU	0x3B, 0x3F, 0x62
SoC_I2C1	GPIO Port Expander	TCA6424ARGJR	0x22, 0x23
SoC_I2C2	CSI Camera Connector	<connector interface>	
SoC_I2C2	User Expansion Connector	<connector interface>	
MCU_I2C0	MCU Header	<connector interface>	
Others			
BOOTMODE_I2C	I2C Bootmode Buffer	TCA6424ARGJR	0x22
BOOTMODE_I2C	Test Automation Header	<connector interface>	

3 Hardware Design Files

The hardware design files such as schematics, BOM, PCB Layout, Assembly Files and Gerber files are available in the link below.

Design Files

4 Compliance Information

4.1 EMC, EMI and ESD Compliance

Components installed on the product are sensitive to Electric Static Discharge (ESD). TI recommends using this product in an ESD controlled environment, such as a temperature and humidity controlled environment to limit the buildup of ESD. Also use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

5 Additional Information

5.1 Known Hardware or Software Issues

This section describes the currently known issues on each EVM revision and applicable workarounds. Issues that have been patched have modification labels attached to the EVM assembly.

Issue Number	Issue Title	Issue Description	Affected Variant
Issue 1	Wake-up from LPM Through MCU and WKUP UART Not Functioning	Wake-up functionality does not operate correctly when triggered through the FT4232 chip to the MCU UART and WAKEUP UART interfaces	E2A
Issue 2	Partial IO Low Power Mode entry/exit failure	On the SK-AM62-LP EVM, the device fails to wake up from LPM mode through the wake-up source even when the wake-up source is correctly configured in software	E2A

5.1.1 Issue 1 – Wake-up from LPM Through MCU and WKUP UART Not Functioning

Applicable EVM Revisions: E2A

Issue Description: Wake-up from LPM functionality does not operate correctly when triggered through the FT4232 chip to the MCU UART and WAKEUP UART interfaces.

Workaround: To resolve this issue, perform the following hardware modifications, cut the trace between U91 pin 3 and U83 pin 3 connected to VCC_3V3_SYS, Remove C437, C460, R510, R534 and resolder these components rotated 90 degrees from the original orientation (refer to Figure 5-1 for correct placement). Then solder a wire from U83.3 to the following connection points C437.2, R510.2, R516.1 and from U91.3 to the following connection points C460.2, R534.2, R528.1. Additionally, solder a wire from U27.8 to C113.2 on the PCB as shown in Figure 5-2. Lift the U26.16 pin and solder a wire from Lifted Pin16 to C113.2 other side pin as per Figure 5-2. Refer to Figure 5-1, Figure 5-2 for visual guidance on component locations and wire routing.

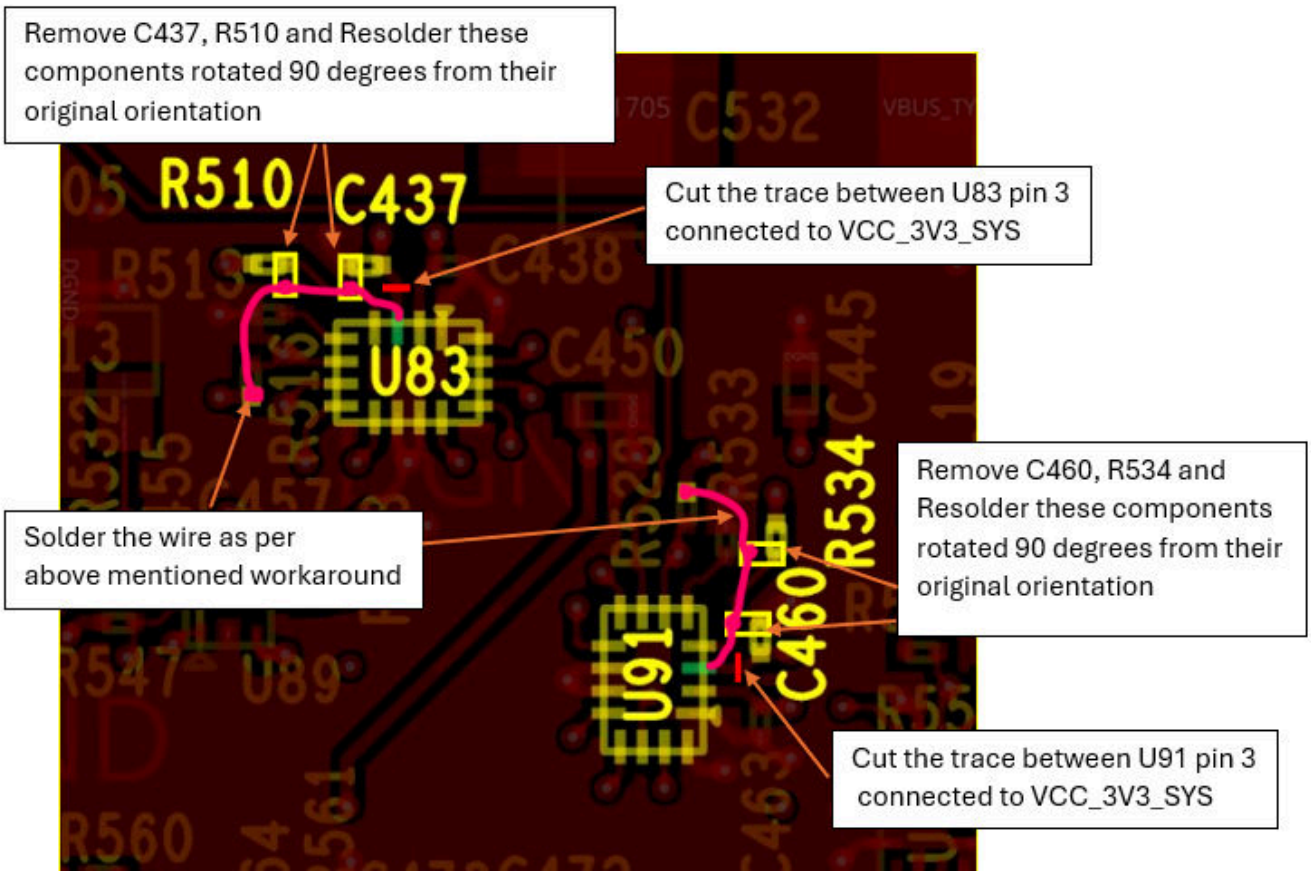


Figure 5-1. SK-AM62-LP Bottom Side

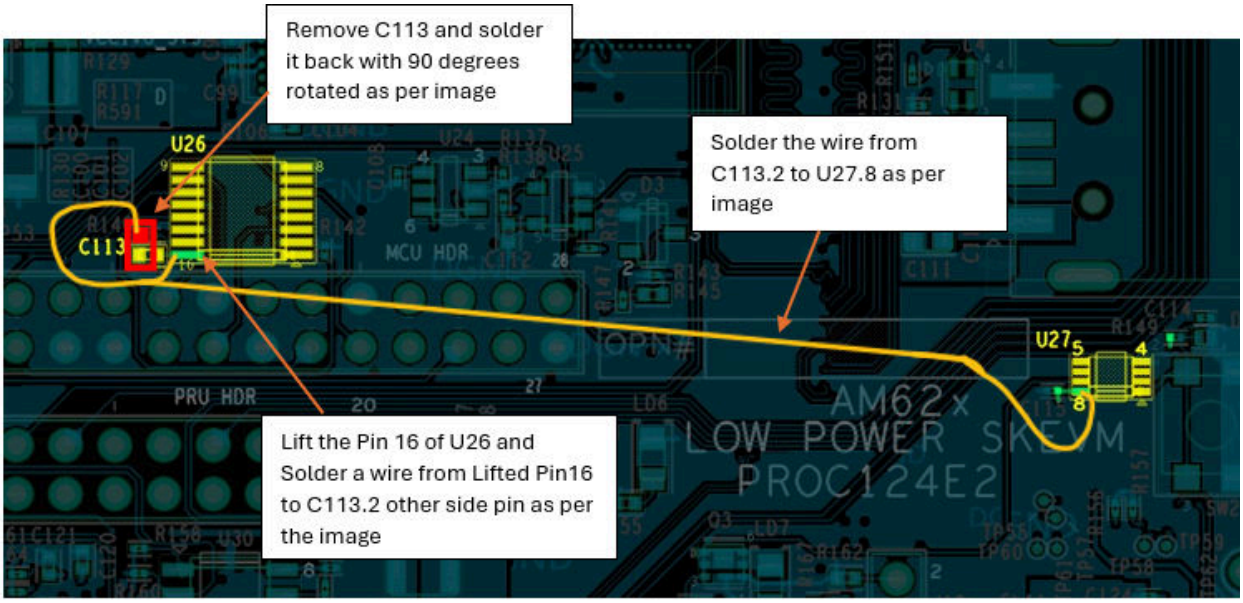


Figure 5-2. SK-AM62-LP Top Side

5.1.2 Issue 2 – Partial IO Low Power Mode entry/exit failure

Applicable EVM Revisions: E2A

Issue Description: On the SK-AM62-LP EVM, the device fails to wake up from LPM mode via wake-up source even when the wake-up source is correctly configured in software.

The root cause is a hardware design consideration on the SK-AM62-LP EVM. The **PMIC_LPM_EN** signal is connected to the PMIC Enable pin through **R590** Resistor. However, the **SN74LVC1G11DRYR AND gate** is also connected to the same **PMIC_EN** line. When the **PMIC_LPM_EN** pin drives low during LPM mode and the AND gate output drives high simultaneously, this conflict can cause **damage to the AND gate** and lead to **PMIC turn-on uncertainty**. To avoid this, **R405 must be removed** to isolate the AND gate from the PMIC_EN line, providing reliable LPM mode operation.

Workaround: Remove resistor R405 (while keeping R590 populated) to isolate the SN74LVC1G11DRYR AND gate from the PMIC_EN line, preventing signal conflict and providing proper PMIC_LPM_EN operation.

Note

Figure 5-3 shows the location of resistor R405, which is populated on the bottom side of the PCBA. Make sure that the board is carefully flipped and the correct component is identified before performing the modification.

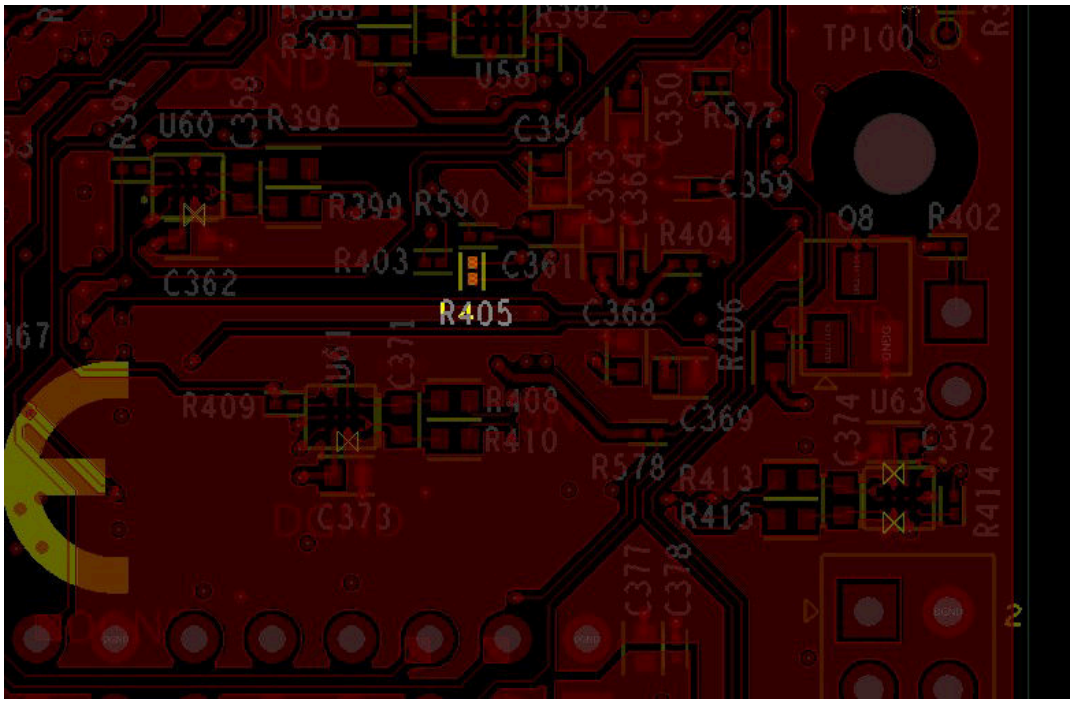


Figure 5-3. SK-AM62-LP Bottom Side for R405

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6 References

- Texas Instruments, *[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP - Collaterals for reference during different phases of custom board design, self-review and bring-up* forum post
- Texas Instruments, *[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM243x, AM335x) families* forum post
- Texas Instruments, *[FAQ] AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit* forum post
- Texas Instruments, *[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Design Recommendations / Custom board hardware design - Custom board schematics self-review* forum post

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 30, 2025 to August 19, 2026 (from Revision A (November 2025) to Revision B (August 2026)) **Page**

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

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2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

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