Application Note

TAS2573 Design and Layout Guidelines

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ABSTRACT

The TAS2573 audio amplifier is a class of digital input Class-D audio amplifiers optimized for efficiency and battery life in real music and voice applications. The amplifier is capable of delivering high output power using an integrated Class-H boost converter.

This application note describes the recommended practices in the design and PCB layout for designs that use this family of devices to provide high quality and reliability of the device in the system, and enable higher efficiency and performance once integrated into the system.

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1 Introduction

TAS2573 is a boosted digital-input Class-D smart amplifier. The device takes a voltage supply from a single or multi-cell battery source, and boosts the supply to a high voltage. This feature enables the user to play audio and deliver high power into a speaker load.

When using this device in audio solutions, the PCB design is a critical factor. To verify that the device is reliable and meets the required performance and functionality criteria, while minimizing losses to maintain system efficiency, certain design and layout practices need to be accounted for while designing the application.

This application note provides a set of recommended guidelines that need to be followed, which enable the user to operate the device at optimal performance and efficiency. The TAS2573EVM is used as a reference to highlight these guidelines.

2 Pin Configuration and Functions

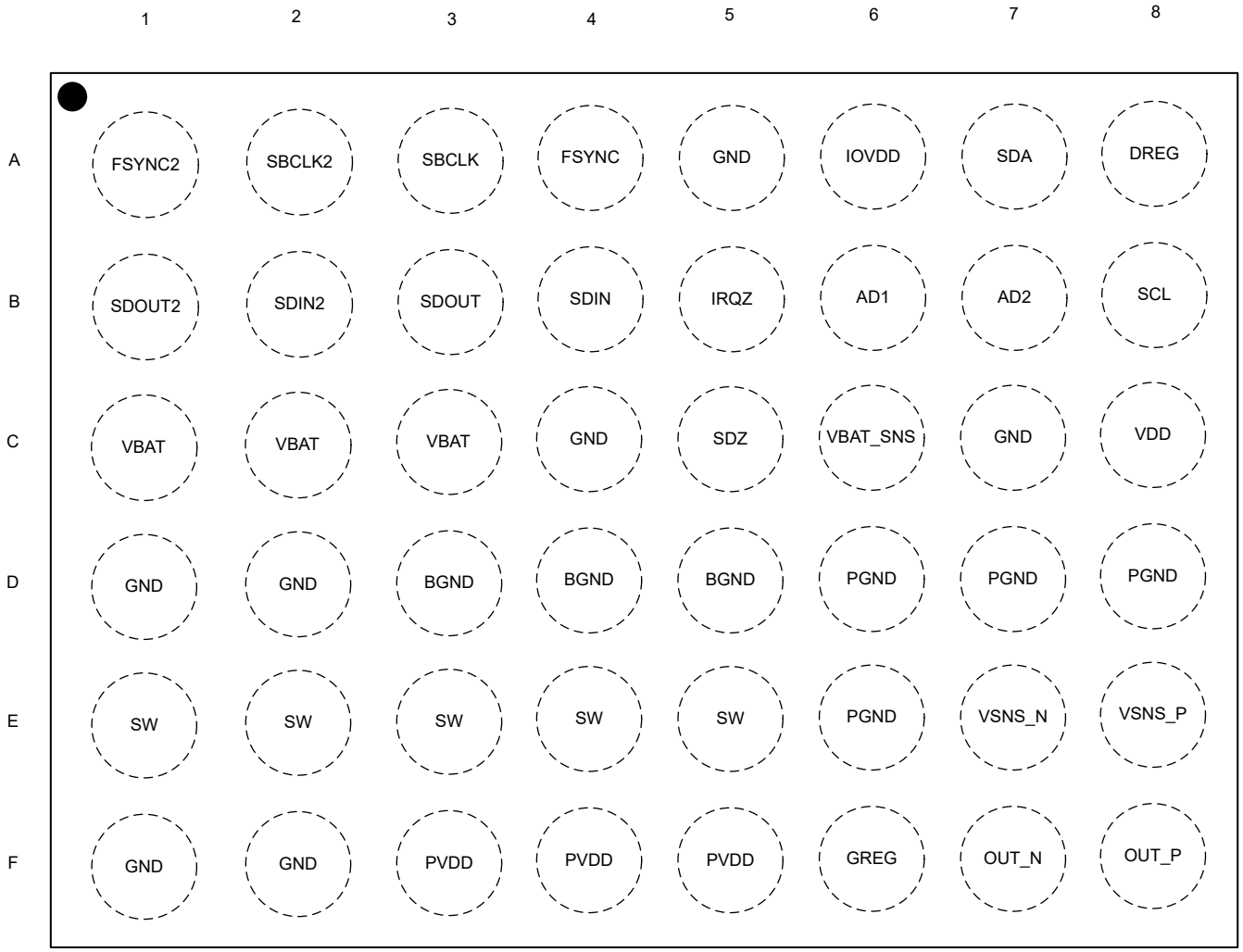

Figure 2-1. Package Top Level View Pinout

Pin Functions

PIN		Type[1]	DESCRIPTION
NAME	NO.		
AD1	B6	I	I²C address pin LSB.
AD2	B7	I	I²C address pin LSB+1.
BGND	D3	P	Boost ground. Connect to PCB GND plane strongly with multiple vias.
	D4		
	D5		
DREG	A8	P	Digital core voltage regulator output. Bypass to GND with a capacitor. Do not connect to external load.
FSYNC	A4	I	I²S word clock or TDM frame sync for Primary Audio Interface.
GREG	F6	P	High-side gate CP regulator output. Do not connect to external load.
GND	A5	P	Digital ground. Connect to PCB GND plane. Strong connection to ground plane required through multiple vias.
	C4		
	C7		
	D1		
	D2		
	F1		
	F2		
IOVDD	A6	P	1.2V or 1.8V Digital IO supply. Decouple to GND with capacitor.
IRQZ	B5	O	Open drain, active low interrupt pin. Pull up to IOVDD with resistor if optional internal pullup is not used.
OUT_N	F7	O	Class-D negative output.
OUT_P	F8	O	Class-D positive output.
PGND	D6	P	Class-D Power stage ground. Connect to PCB GND plane strongly through multiple vias.
	D7		
	D8		
	E6		
PVDD	F3	P	Integrated boost output and Class-D power stage supply.
	F4		
	F5		
SBCLK	A3	I	I²S/TDM serial bit clock for Primary Audio Interface.
SCL	B8	I	I²C Clock Pin. Pull up to IOVDD with a resistor.
SDA	A7	I/O	I²C Data Pin. Pull up to IOVDD with a resistor.
SDIN	B4	I	I²S or TDM serial data input for Primary Audio Interface.
SDOUT	B3	O	I²S or TDM serial data output for Primary Audio Interface.
SDZ	C5	I	Active low hardware shutdown.
SW	E1	P	Boost converter switch input.
	E2		
	E3		
	E4		
	E5		
VBAT	C1	P	Battery power supply input. Connect to 2.5V to 5.5V supply and decouple with a capacitor.
	C2		
	C3		
VBAT_SNS	C6	I	Battery sense terminal. Connect to 1S or 2S battery supply for remote battery sensing. Ground the pin if remote sensing is not used.
GND	C6	P	Ground Pin. This pin can also be used as battery sense terminal. Connect to 1S or 2S battery supply for remote battery sensing. Ground the pin if remote sensing is not used.
VDD	C8	P	Analog, digital power supply. Connect to 1.8V supply and decouple to GND with capacitor.

Pin Functions (continued)

PIN		Type[1]	DESCRIPTION
NAME	NO.		
VSNS_N	E7	I	Voltage sense negative input. Connect to speaker negative terminal as close to speaker as possible. Add series resistor if EMI filter is used.
VSNS_P	E8	I	Voltage sense positive input. Connect to speaker positive terminal as close to speaker as possible. Add series resistor if EMI filter is used.
FSYNC2	A1	I	I^2S word clock or TDM frame sync for Secondary Audio Interface.
SBCLK2	A2	I	I^2S/TDM serial bit clock for Secondary Audio Interface.
SDIN2	B2	I	I^2S or TDM serial data input for Secondary Audio Interface.
SDOUT2	B1	O	I^2S or TDM serial data output for Secondary Audio Interface.

1. I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

3 Application Schematics

The following figures show the various configurations that the TAS2573 can be connected in. Figure 3-1 shows the TAS2573 in 1S configuration, where a single-cell battery is used as the voltage source to power up the device.

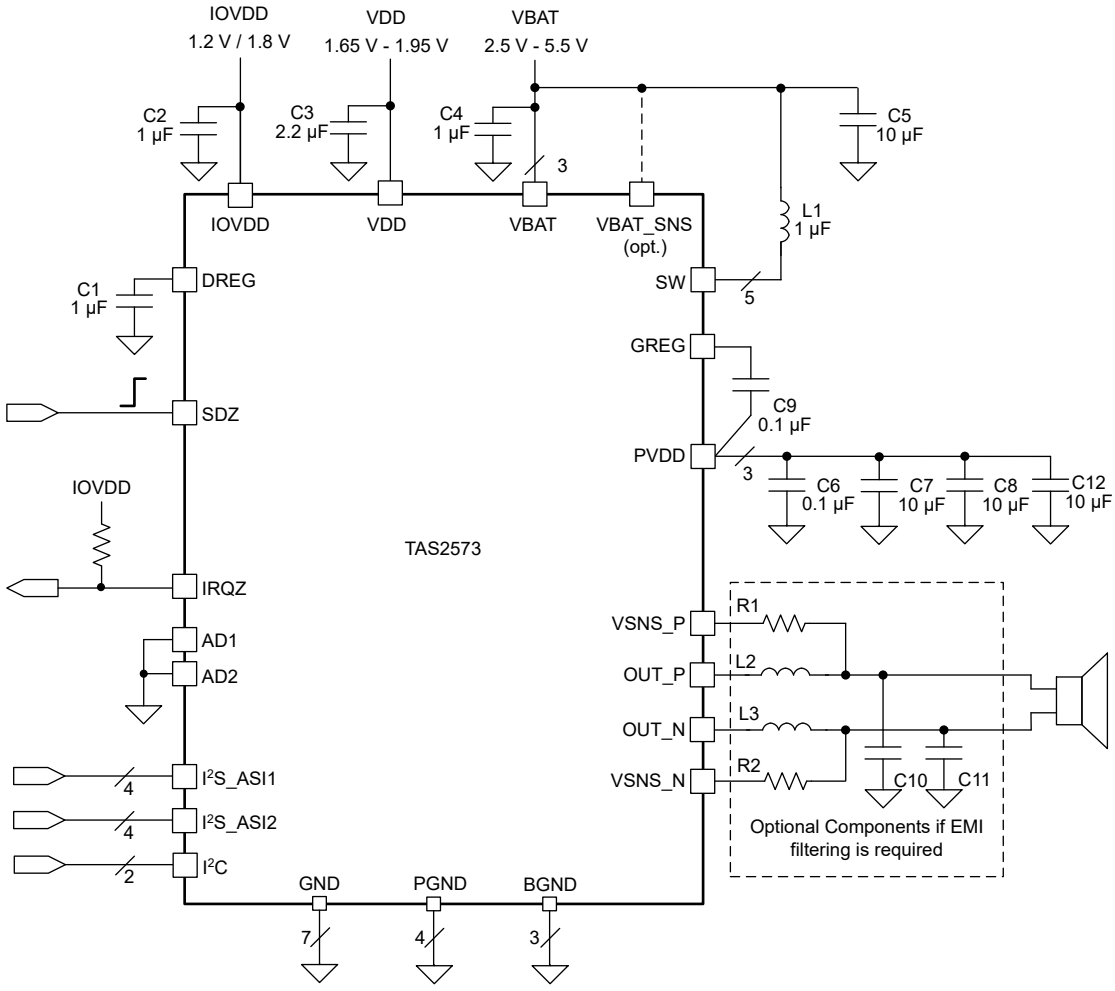

Figure 3-1. TAS2573 in 1S Configuration

Figure 3-2 shows the device being connected in 2S configuration, with a 2-cell battery acting as the power source for the device.

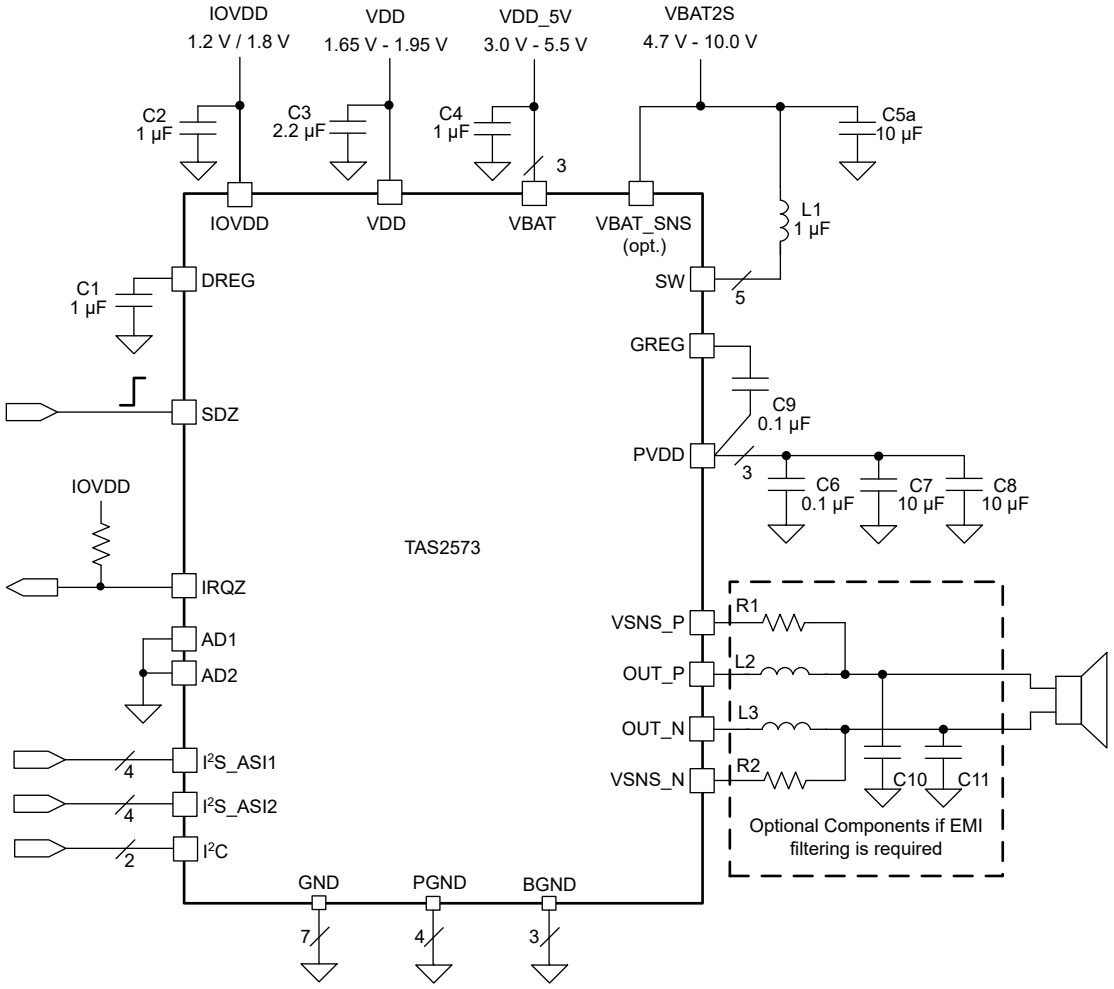

Figure 3-2. TAS2573 in 2S Configuration

Figure 3-3 shows an external PVDD configuration for the TAS2573 where the internal boost converter of the device is disabled, and the PVDD can be provided externally from a 3-cell battery.

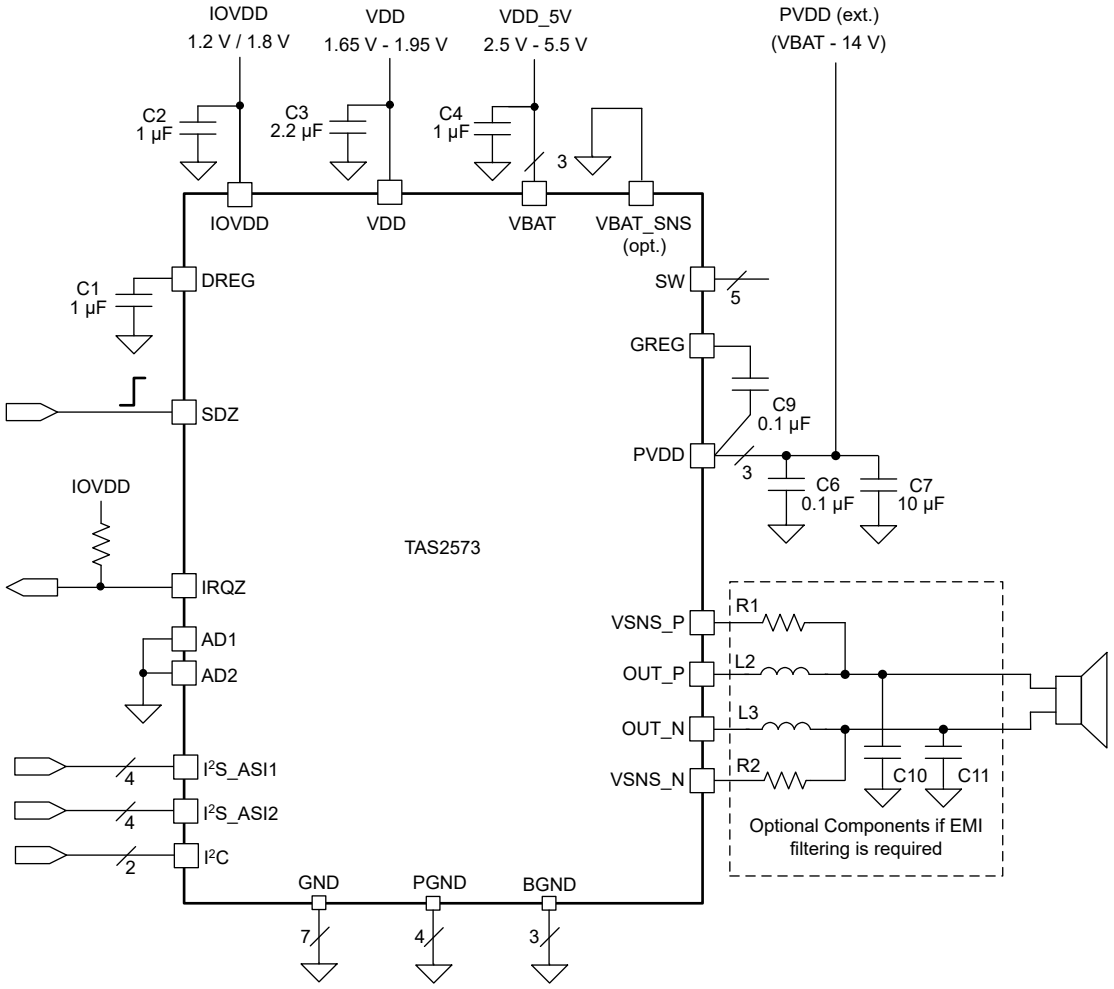

Figure 3-3. TAS2573 in External PVDD Configuration

3.1 Recommended Component Ratings

Table 3-1 shows the recommended component ratings for the components shown in Figure 3-1, Figure 3-2, and Figure 3-3.

Table 3-1. Component Ratings

Component	Description	Specification	Min	Typical	Max	Unit
L1	Boost Converter Inductor	Inductance	0.47	1	-	µH
		Saturation Current	-	5.3	-	A
L2, L3	Optional EMI Filter Inductors (must use R1, R2 if L2, L3 are used)	DC Current	2	-	-	A
C1, C2	DREG, IOVDD decoupling capacitors	Capacitance 20% tolerance	-	1	-	µF
		Voltage Rating	2	6.3	-	V
C3	VDD decoupling capacitor	Capacitance 20% tolerance	-	2.2	-	µF
		Voltage Rating	2	6.3	-	V
C4	VBAT decoupling capacitor	Capacitance 20% tolerance	-	1	-	µF
		Voltage Rating	6.3	10	-	V
C5	VBAT power decoupling capacitor	Capacitance 20% tolerance	-	10	-	µF
		Voltage Rating	6.3	10	-	V
C5a	VBAT2S decoupling capacitor	Capacitance 20% tolerance	-	10	-	µF
		Voltage Rating	10	16	-	V
C6	PVDD Low-ESL decoupling capacitor	Capacitance 20% tolerance	-	0.1	-	µF
		Voltage Rating	16	25	-	V
C7, C8, C12	PVDD Power decoupling capacitors	Capacitance 20% tolerance	-	10	-	µF
		Voltage Rating	16	25	-	V
		De-rated capacitance at 13V of the combined PVDD capacitor	3	-	-	µF
C9	GREG decoupling capacitor	Capacitance 20% tolerance	-	0.1	-	µF
		Voltage Rating	6.3	10	-	V
C10, C11	Optional EMI Filter capacitors (must use L2, L3 if C10, C11 are used)	Voltage Rating	2xPVDD		-	V
R1, R2	Optional Voltage sense resistors (Must be used if L2, L3 are used)	Resistance, 5% tolerance	1	2.2	4.7	kΩ
		Temperature Coefficient	-	-	300	ppm / °C
		Rated Power	-	0.01	-	W

4 Layout Guidelines

This section describes in detail the best layout practices to be followed for individual pin sections of the device.

4.1 VDD Pin

The VDD pin is used to power up various critical analog and digital blocks within the device. The VDD pin also acts as a power source for driving the Class-D output stage at lower power, if and when the device is operating in the Y-bridge mode.

The following guidelines need to be taken into account when routing the VDD pin to the corresponding power source on the PCB:

- When the Y-Bridge is enabled at power levels below the Y-Bridge threshold, the Class-D amplifier draws switching currents from the VDD pin. This current can be in the order of 200mA due to the fast edge rates.
- Any parasitic inductance in the path between the VDD pin and the corresponding power source results in significant voltage ripple on the pin, due to the L.dI/dT inductive kickback to the switching currents. This effect can potentially impact the performance and functionality of the device.
- Decoupling the VDD pin with a capacitor of value ≥ 2.2µF to the GND pin is recommended. This capacitor needs to be placed as close to the VDD pin as possible in the same layer.
- The decoupling capacitor must have the lowest possible parasitic inductance (ESL). Using a 0201 package capacitor is recommended.
- In case of space constraints in the PCB, place the capacitor such that the top plate connects directly to the VDD pin, and the bottom plate is connected to the PCB ground plane using multiple vias (a minimum of 3 vias is recommended).

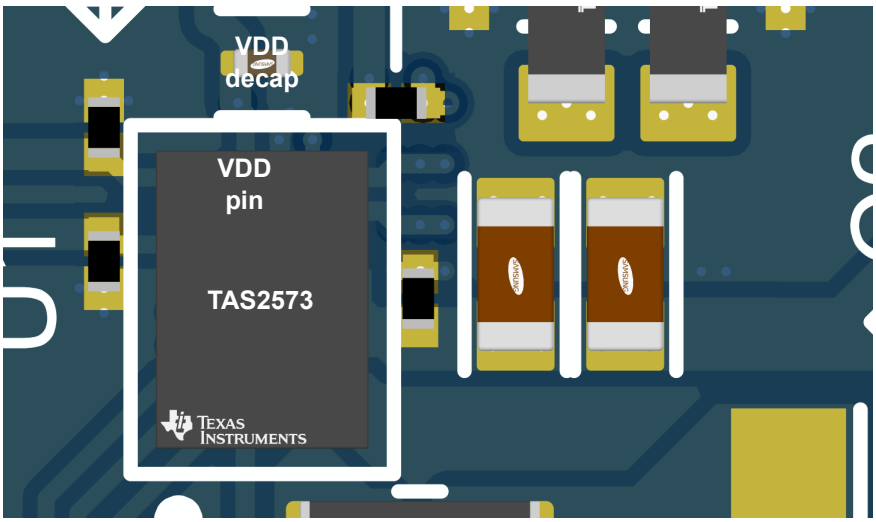

Figure 4-1. Placement of VDD Decoupling Capacitor

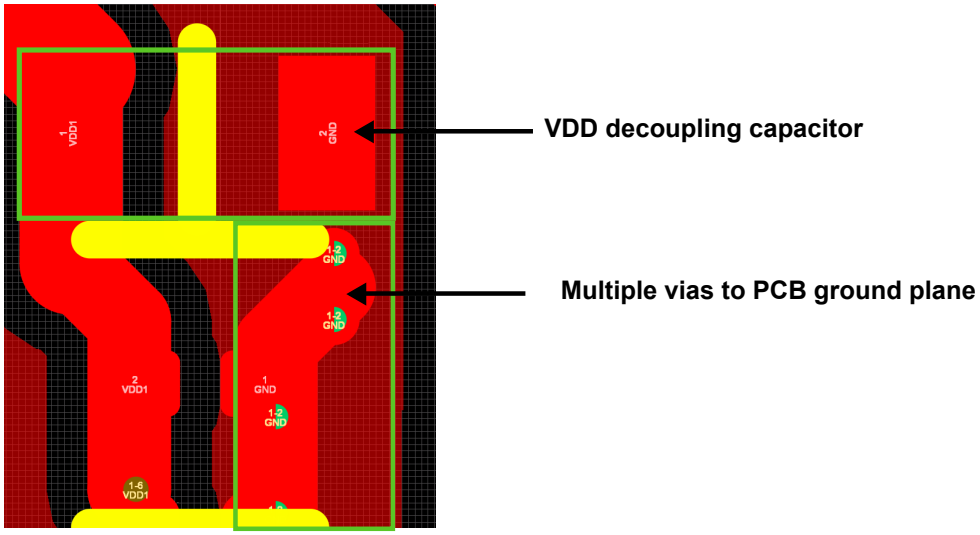

Figure 4-2. Routing from VDD Pin on Layer 1

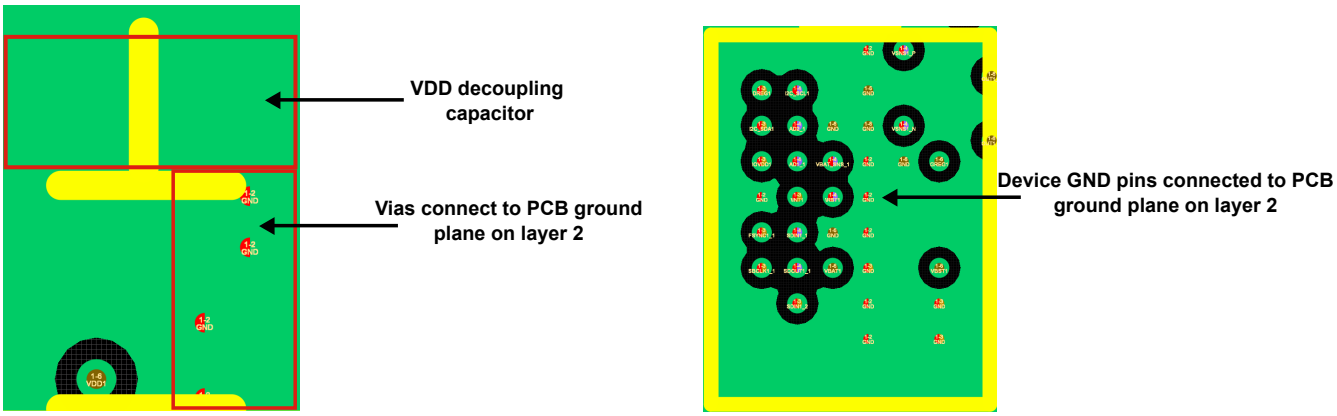

Figure 4-3. Connection of Decoupling Capacitor to PCB Ground Plane on Layer 2

4.2 PVDD Pin

The PVDD pins correspond to the output of the internal boost converter. The PVDD pins also act as the power source for driving the Class-D output stage when the output power level is higher than the Y-Bridge threshold.

The following recommendations need to be taken into account when routing the PVDD pin on to the PCB:

- When the output power level is beyond the Y-Bridge threshold, the Class-D output stage draws high switching currents from the PVDD pin due to the fast edge rates.
- This pin must not be loaded through external circuitry when the device is operating with the boost converter.
- To minimize voltage ripple on the PVDD pin due to these transient currents, the PVDD pin must be bypassed with capacitors of value ≥ 3 x 10µF.
- This capacitance can see a level of derating due to:
  - Tolerance
  - Voltage coefficient near maximum PVDD voltage
- This derated capacitance must be at least 3µF at 13V.
- The PVDD pin also needs to be bypassed with a low-ESL capacitor (ESL must be ≤ 250pH) of 0.1µF, to minimize the loop inductance from PVDD to PGND. Use a 0201 package capacitor to achieve this bypass. The low-ESL capacitor must be placed as close to the device as possible.

- The decoupling capacitors need to be bypassed to the PGND pins. When bypassing through the PCB ground plane, use multiple vias (a minimum of three vias is recommended), to minimize parasitic inductance between the ground connection on the bypass capacitor and the PGND pins of the device.
- When operating in external PVDD mode, the PVDD pins need to be connected to the power source using wide traces that are capable of carrying high current, and have low parasitic resistances, to minimize I^2R losses.

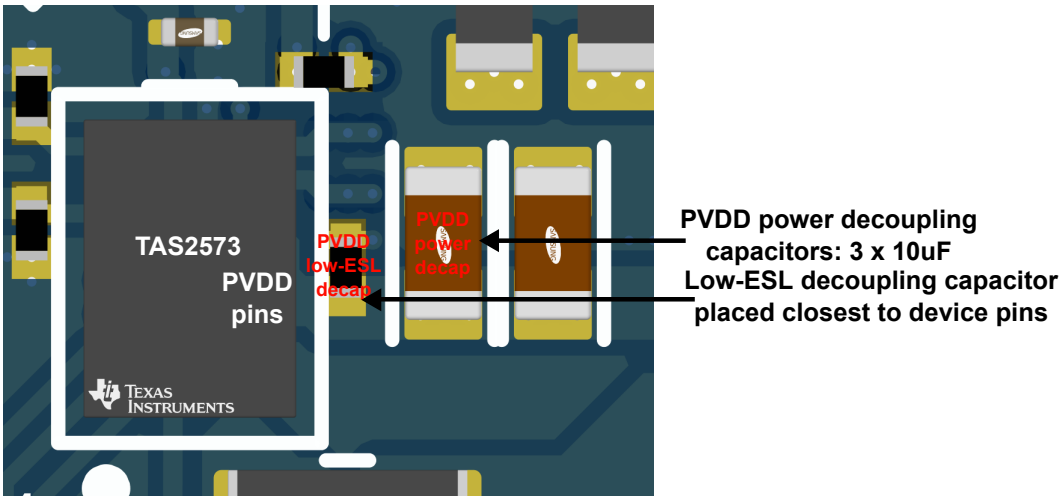

Figure 4-4. Placement of PVDD Decoupling Capacitors

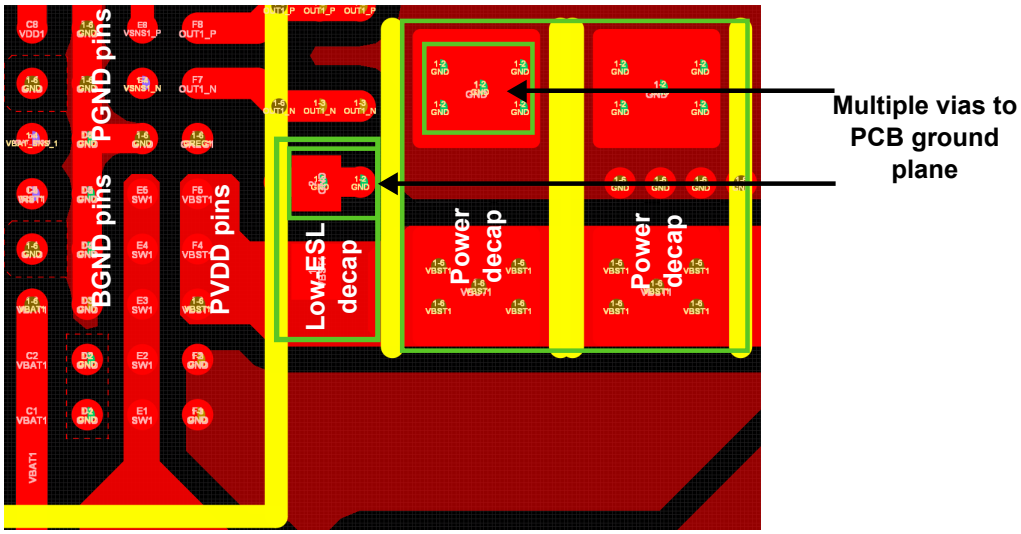

Figure 4-5. Routing From PVDD Pins on Layer 1

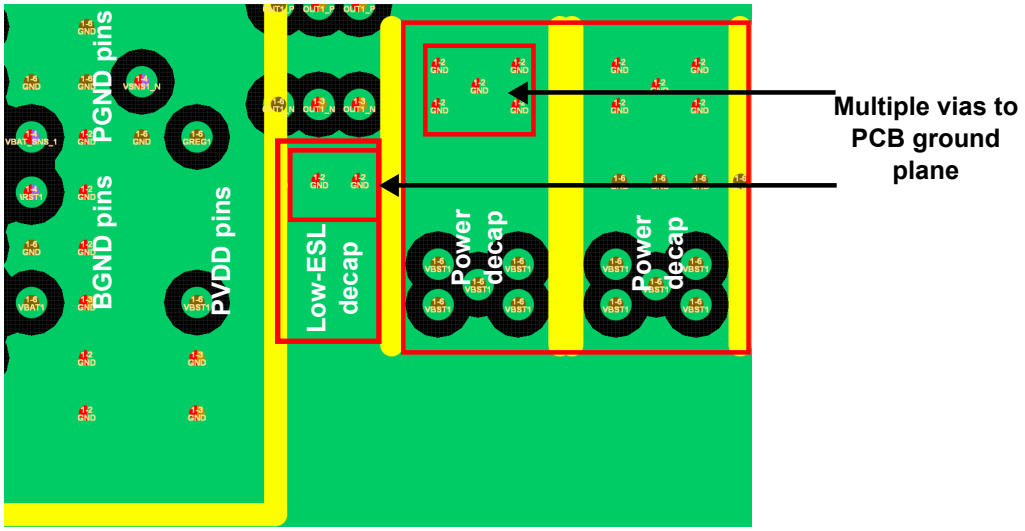

Figure 4-6. Connection of Decoupling Capacitors to PCB Ground Plane on Layer 2

4.3 GREG Pin

The GREG pin acts as the supply pin for the high-side gate drivers in the boost converter and the Class-D output stages. The GREG pin is powered using the voltage on the VBAT pin.

The following recommendations need to be taken into account when routing the GREG pin on to the PCB:

- The GREG pin needs to be decoupled to the PVDD pin using a capacitor of value 0.1µF (recommendation is to use a 0201 package to minimize ESL and ESR).
- The top plate needs to be connected to the GREG pin, and the bottom plate needs to use a star-connection directly to the PVDD pins, and not to the PVDD PCB plane or the top plate of the PVDD decoupling capacitor, to avoid common inductance to the PVDD pins.
- The voltage rating of the decoupling capacitor must be ≥ 6.3V.
- If the connection is made in inner PCB layers, use multiple vias to reduce parasitic inductance in the path.

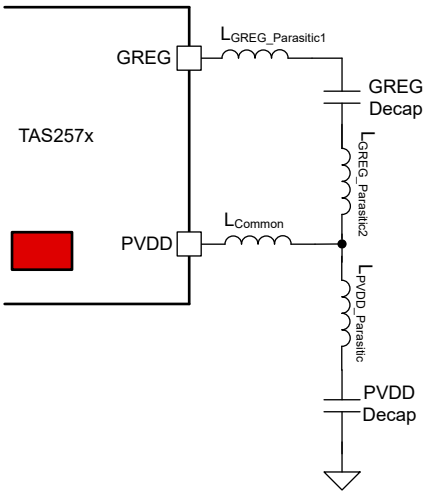

Figure 4-7. Incorrect Routing of GREG Decoupling Capacitor

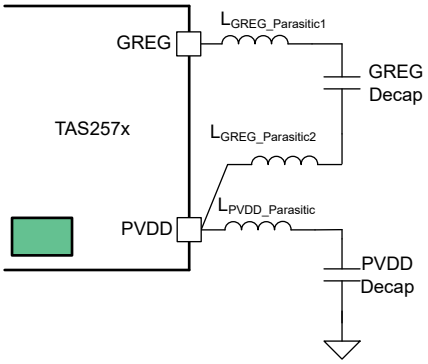

Figure 4-8. Correct Routing of GREG Decoupling Capacitor

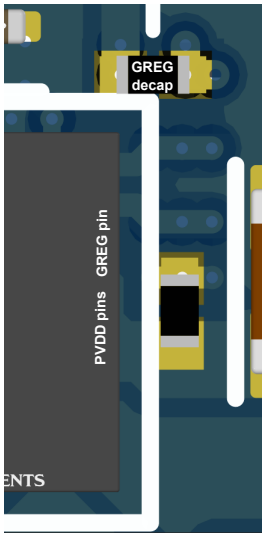

Figure 4-9. Placement of GREG Decoupling Capacitor on EVM

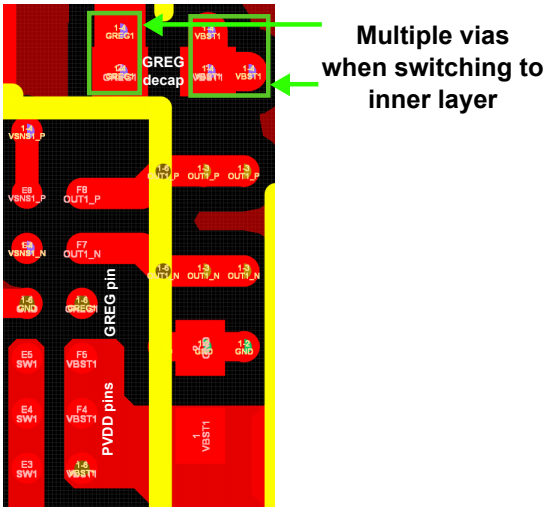

Figure 4-10. Connection of GREG Decoupling Capacitor to Inner Layer Using Vias

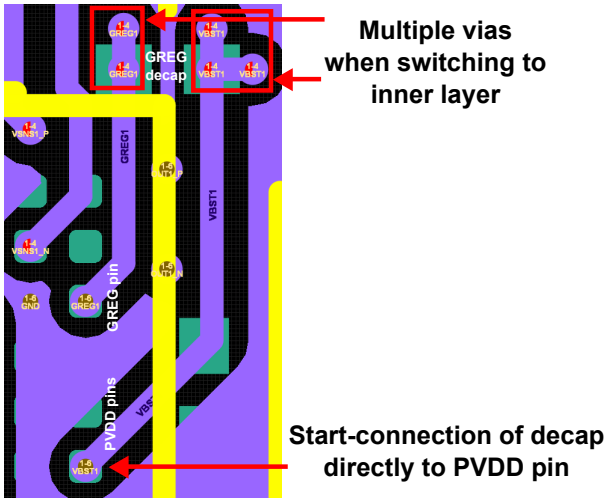

Figure 4-11. Routing of Decoupling Capacitor to GREG and PVDD Pins in Layer 4

4.4 SW Pin

The SW pins correspond to the switching input to the internal boost converter of the device. The following recommendations need to be taken into account while routing the power source to the SW pins on the PCB:

- This node is expected to carry high transient current. The node needs to be routed with wide traces with high current carrying capability and minimal parasitic resistance and inductance.
- This node can switch at high voltages. Avoiding routing any low-voltage traces is recommended, including BCLK, FSYNC, SDIN SDOUT and more across this node to avoid coupling.
- Place the inductor that connects to the SW pins close to the device. Using inductors with lower ESR helps to achieve higher efficiency.
- The routing from the power source to the SW inductor must have minimal parasitic resistance to minimize efficiency impact from I^2R losses.
- Decouple the SW inductor with a capacitor of value ≥ 10µF, placed as close to the inductor as possible. This placement is meant to reduce ripple on the node stemming from transient currents. This capacitor must be placed between the power source and the inductor, and not between the inductor and the SW pins of the device.
- Minimize parasitic capacitance on the SW node path, to reduce switching losses, which impacts efficiency.
- When the device is operating in external PVDD mode, the SW pin must be left unconnected.

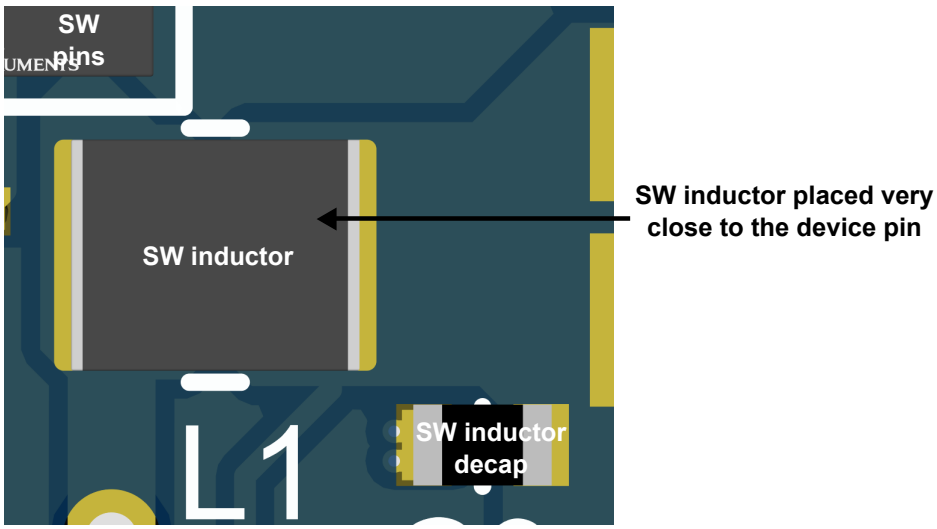

Figure 4-12. Placement of Boost Inductor and Decoupling Capacitor Near SW Pins

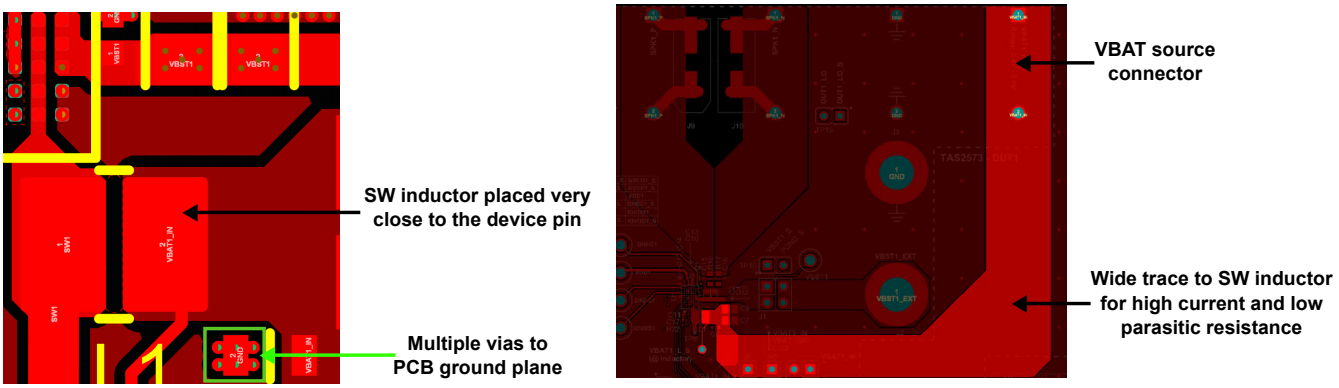

Figure 4-13. Routing of Power Source to SW Inductor on Layer 1

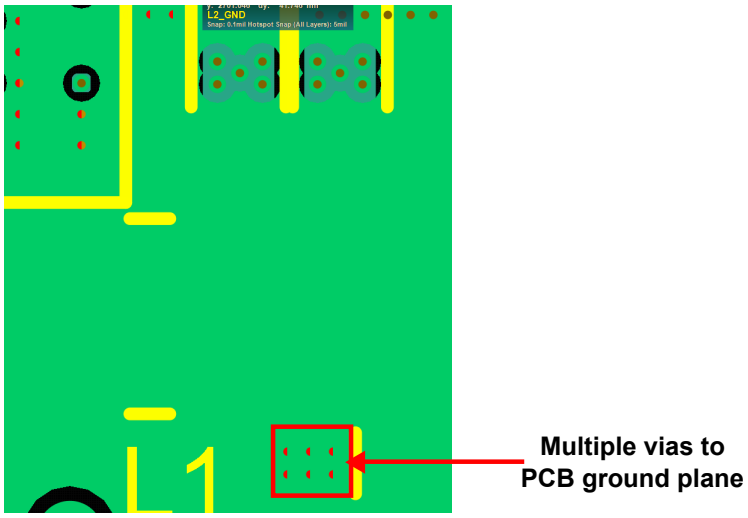

Figure 4-14. Connection of the Decoupling Capacitor for the SW Inductor to PCB GND Plane on Layer 2

4.5 VBAT Pin

The VBAT pin acts as a device power supply pin, used to power up some of the internal analog blocks within the device. This pin also acts as a voltage sense pin when the device is configured to sense the supply voltage on the VBAT pin. This pin is used for various battery monitoring decisions like voltage limiting, brown-out detection, boost turn-on, and more, especially in VBAT1S mode.

The following guidelines need to be taken into account while routing the VBAT pin on to the PCB:

- The VBAT pin carries a current up to 10mA. The trace routed to this pin can be narrower compared to the previously mentioned pins.
- The VBAT pin needs to be routed to the power source through a trace that is independent of the high current path used to route to the SW inductor.
- The VBAT pin needs to be decoupled to GND with a capacitor of value ≥ 1µF, that is placed as close to the device as possible. Using a 0201 package capacitor for lower ESL and ESR is recommended.
- The bottom plate of the capacitor, if connected to GND through the ground plane of the PCB, needs to be connected using multiple vias to minimize parasitic inductance to the GND pin.

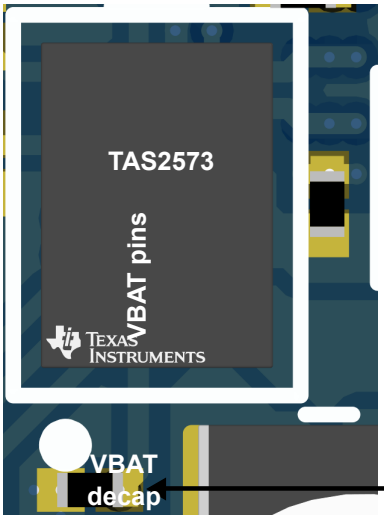

Figure 4-15. Placement of Decoupling Capacitor Near the VBAT Pin

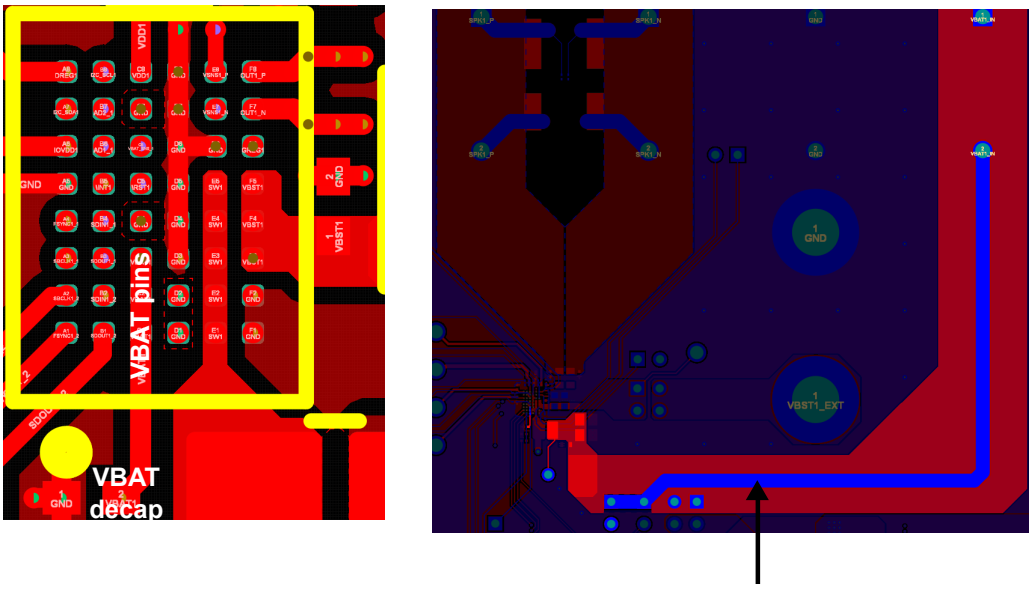

Figure 4-16. Routing of Power Source to VBAT Pin on Layer 1

4.6 VBAT_SNS Pin

The VBAT_SNS pin is an additional battery sense pin present in the device.

The following guidelines need to be accounted for in PCB routing of the VBAT_SNS pin:

- In VBAT1S mode, this pin acts as an optional Kelvin sense pin.
- If unused, connect this pin to ground.
- In VBAT2S mode, this pin is connected to the 2S power source. This pin is then monitored for internal decisions on voltage limiter, boost turn-on, and more.
- When used, this pin needs to be routed to the power source through a separate trace that is independent of the high current path that is routed to the SW inductor.

4.7 OUT_P and OUT_N Pins

The OUT_P and OUT_N pins correspond to the differential output of the Class-D amplifier. The following guidelines need to be taken into account for routing these pins on the PCB:

- These pins switch from 0 - VDD in Y-bridge mode, and 0 - PVDD when Y-bridge threshold is exceeded.
- This switching happens at fast edge rates, and results in high switching current at these nodes. Therefore these pins need to be routed to the speaker with wide traces capable of carrying high current.
- When the routing switches into inner layers of the PCB, multiple vias need to be used to provide current carrying capacity, and reduced parasitic inductance.
- The parasitic capacitance on these pins need to be kept to a minimum, since these parasitic capacitance results in increased switching losses, impacting efficiency. If the capacitance is high enough, the switching can also potentially trigger over-current interrupts.
- Since these nodes are high-voltage switching nodes, avoid routing any low-voltage nodes across this path, like BCLK, FSYNC, SDIN, SDOUT, and more, to avoid coupling.

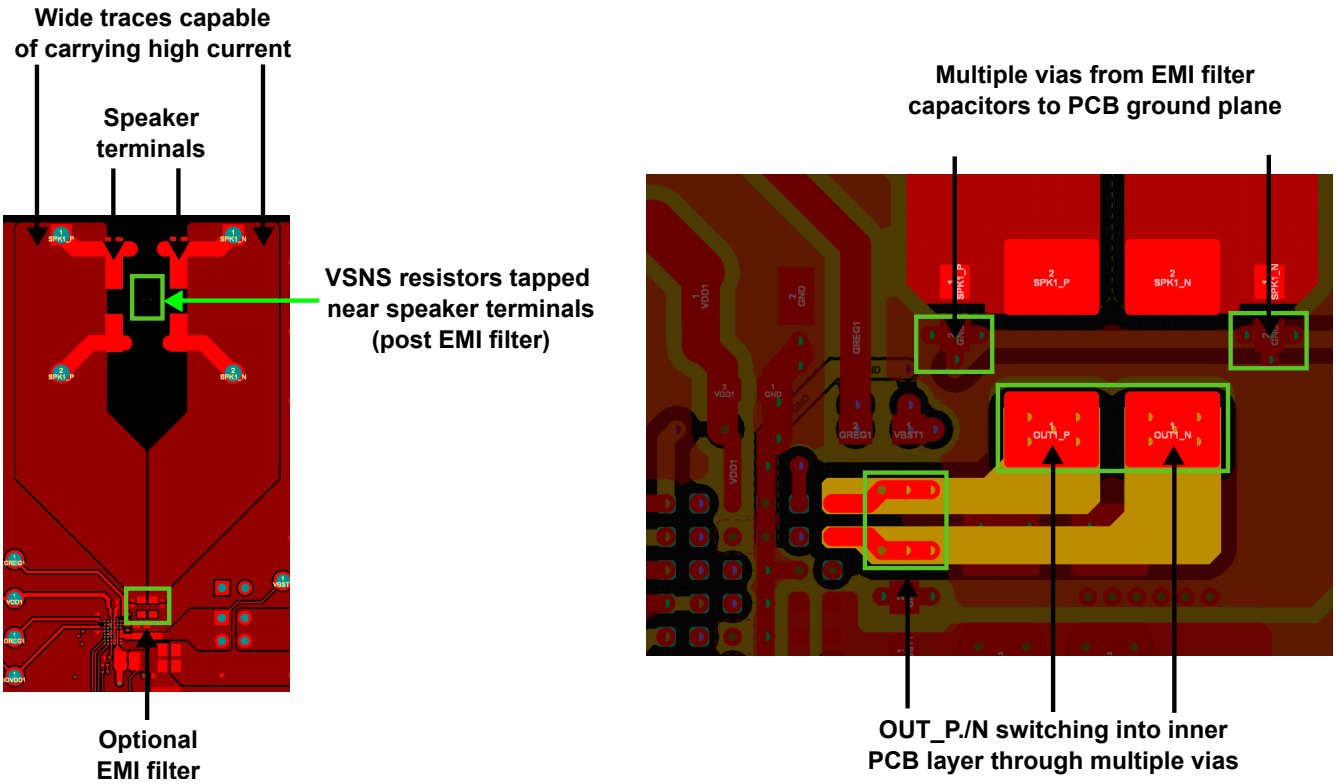

Figure 4-17. Routing of OUT_P/N to Speaker Terminals on Layer 1

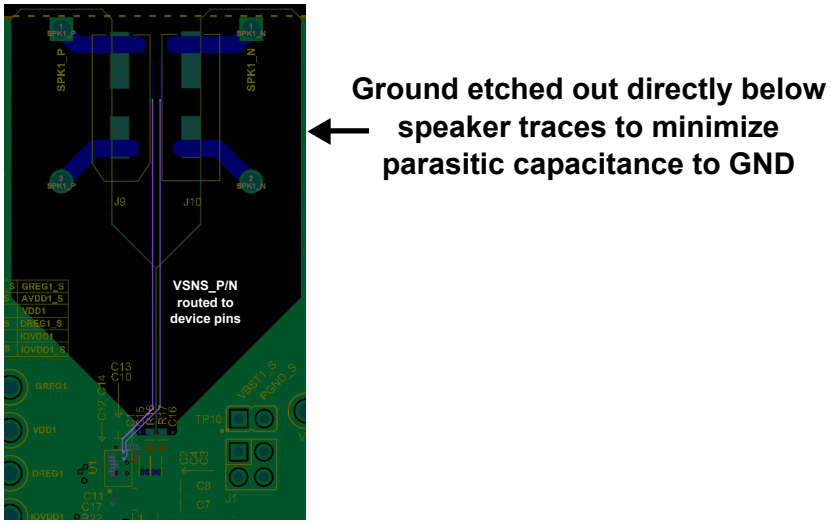

Figure 4-18. Routing Below OUT_P/N Paths in Inner PCB Layers

4.7.1 Optional EMI Filter on Output

The TAS2573 supports edge-rate control to minimize EMI, however the system designer can include passive EMI filter on the Class-D outputs if desired.

When using an EMI filter on the OUT_P or OUT_N pins, the following must be accounted for:

- The L - C cutoff frequency of the filter must be > 3MHz to avoid resonance with the Class-D switching frequency.
- The value of the capacitor, C, used in the filter must be selected, such that the (C / L) ratio is ≤ 1.5. This measure avoids false over-current interrupts during peak output power delivery.
- The VSNS_P or VSNS_N path must be routed from near the speaker terminals to the device pins. If an EMI filter is used, this routing is taken after the EMI filter.
- When using an EMI filter, 2.2kΩ series resistance on the VSNS_P or VSNS_N routing paths is recommended. This resistance must be kept to a maximum of 4.7kΩ.

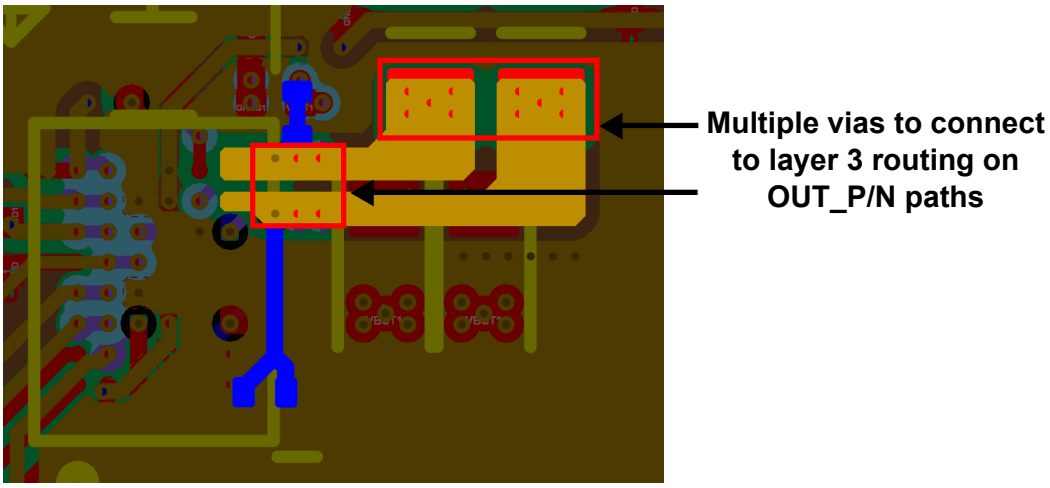

Figure 4-19. Routing From OUT_P/N Pins to EMI Filter Through Layer 3

4.8 IOVDD Pin

The IOVDD pin is the power supply pin for the digital I/Os of the device. The following recommendations need to be taken into account while routing the IOVDD pin on to the PCB:

- Decouple the IOVDD pin to GND using a capacitor of value ≥ 1µF, placed as close to the device as possible.
- When a common power source is used to power up both the VDD and IOVDD pins, verify the sharing of the source occurs near the device, (as an example, the VDD and IOVDD pins need to be shorted as close to the device as possible), and the common routing needs to be connected to the power source.
- When using such a connection, the combined decoupling capacitors need to be placed close to the VDD pin.

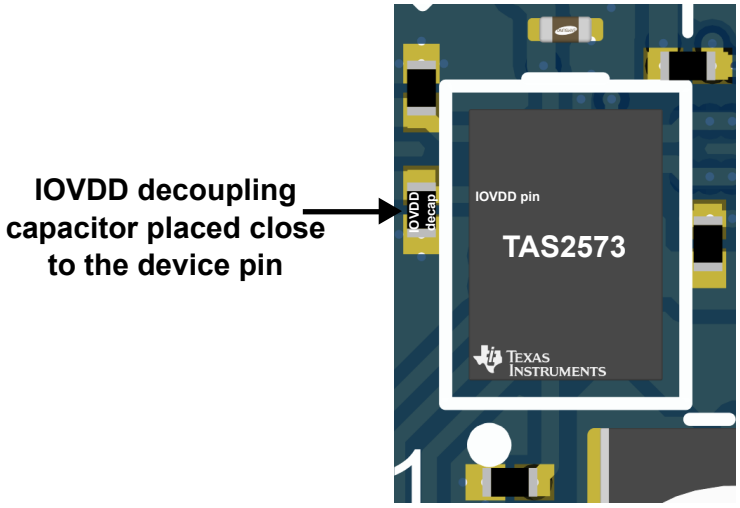

Figure 4-20. Placement of IOVDD Decoupling Capacitor

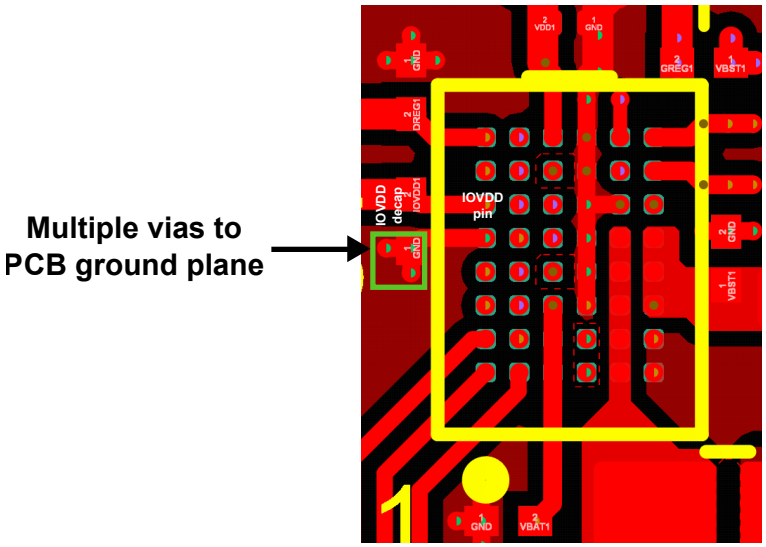

Figure 4-21. Routing of IOVDD Decoupling Capacitor to Pin on Layer 1

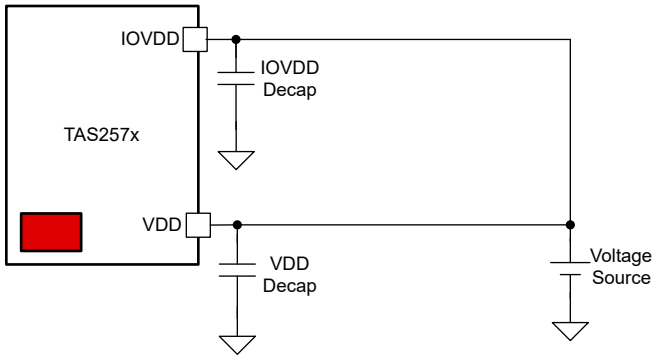

Figure 4-22. Incorrect Connection for Sharing VDD and IOVDD

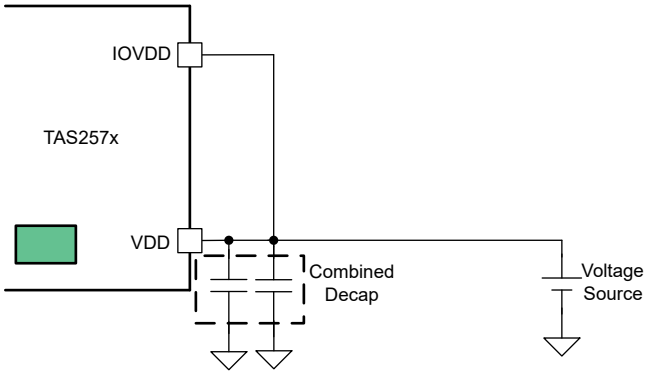

Figure 4-23. Recommended Connection for Sharing VDD and IOVDD

4.9 DREG Pin

The DREG pin corresponds to an internally generated LDO voltage. The DREG pin acts as a power supply for the internal digital blocks of the device. The following guidelines need to be taken into consideration while routing the DREG pin on to the PCB:

- The DREG pin must be decoupled to the GND pin with a capacitor of value ≥ 1µF. This capacitor needs to be placed as close to the device as possible. Use a 0201 capacitor to minimize ESR and ESL.
- The DREG pin must not be loaded by any external circuit.
- If decoupling through the ground plane of the PCB, use multiple vias to minimize parasitic inductance between the ground connection of the capacitor and the GND pin of the device.

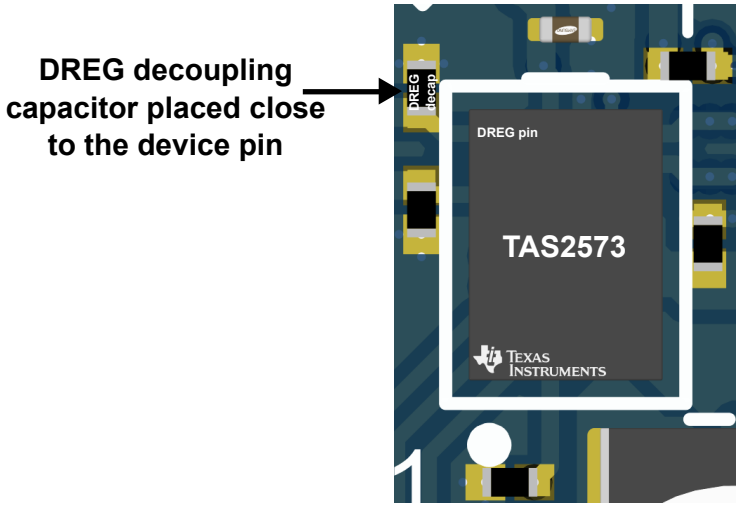

Figure 4-24. Placement of DREG Decoupling Capacitor

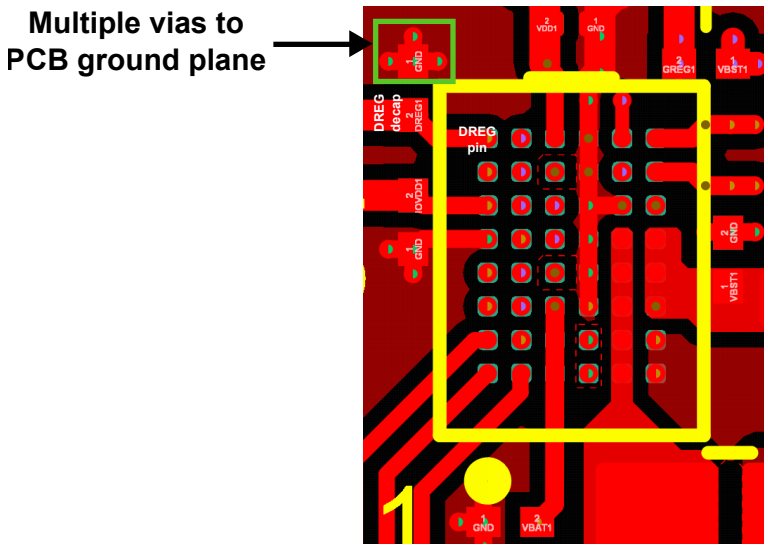

Figure 4-25. Routing of DREG Decoupling Capacitor to Pin on Layer 1

4.10 Digital I/O Pins

The device contains the following digital I/O pins, all referenced with respect to the IOVDD supply voltage:

- SCL, SDA for I^2C communication to the device.
- AD1, AD2 to set the I^2C device address.
- SBCLK, FSYNC, SDIN, SDOUT for the TDM/I^2S audio serial interface.
- IRQz for the device interrupt.
- SDz for hardware shutdown of the device.

These digital pins need to be routed away from the high-voltage switching nodes (SW, OUT_P, OUT_N, VSNS_P, VSNS_N), to avoid any coupling, which can corrupt the integrity of the digital signals.

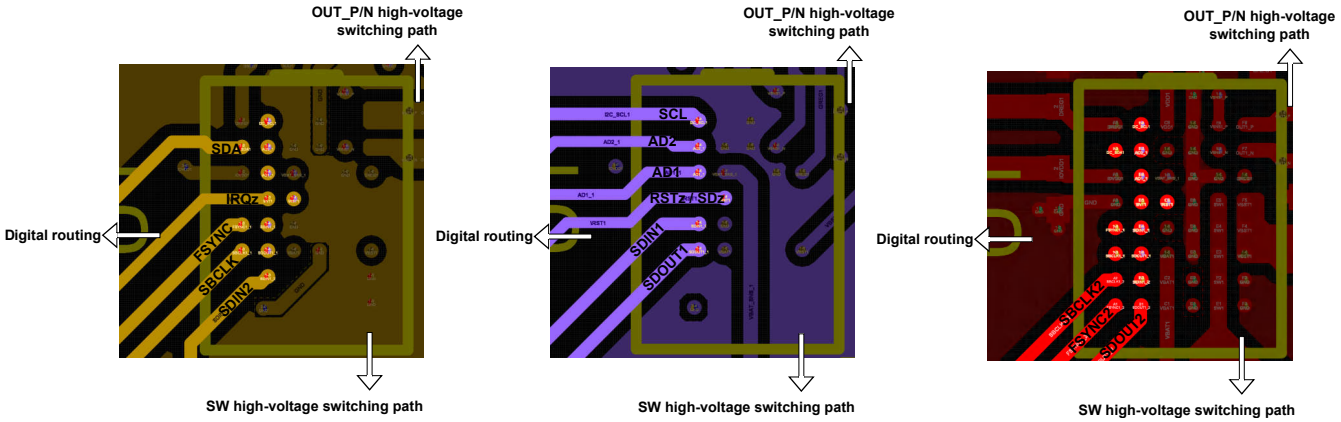

Figure 4-26. Routing of Digital Lines in Inner Layers (3 and 4) Away From the High-voltage Switching Lines

4.11 Ground Pins

The device contains multiple ground pins, which need to be connected to the ground planes in the PCB. While connecting the pins, the following guidelines must be taken into consideration:

- The device has three GND pins, for the analog and digital grounds. These three pins need to be connected independently to the PCB ground plane using vias. Avoid shorting these pins together at the top layer, to avoid common inductance to PCB ground.
- The device has three BGND pins referring to the boost converter, and four PGND pins referring to the Class-D power stage. These pins need to be shorted together on the top layer of the PCB, and then routed to the PCB ground plane using individual vias.
- Avoid shorting the BGND or PGND pins to the other GND pins of the device in the top layer, to avoid common inductance to the PCB ground.

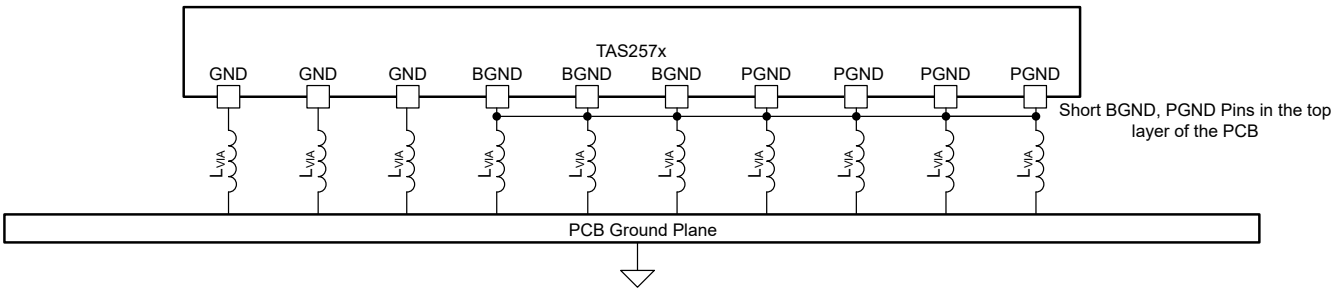

Figure 4-27. Connection of Ground Pins to PCB GND Plane

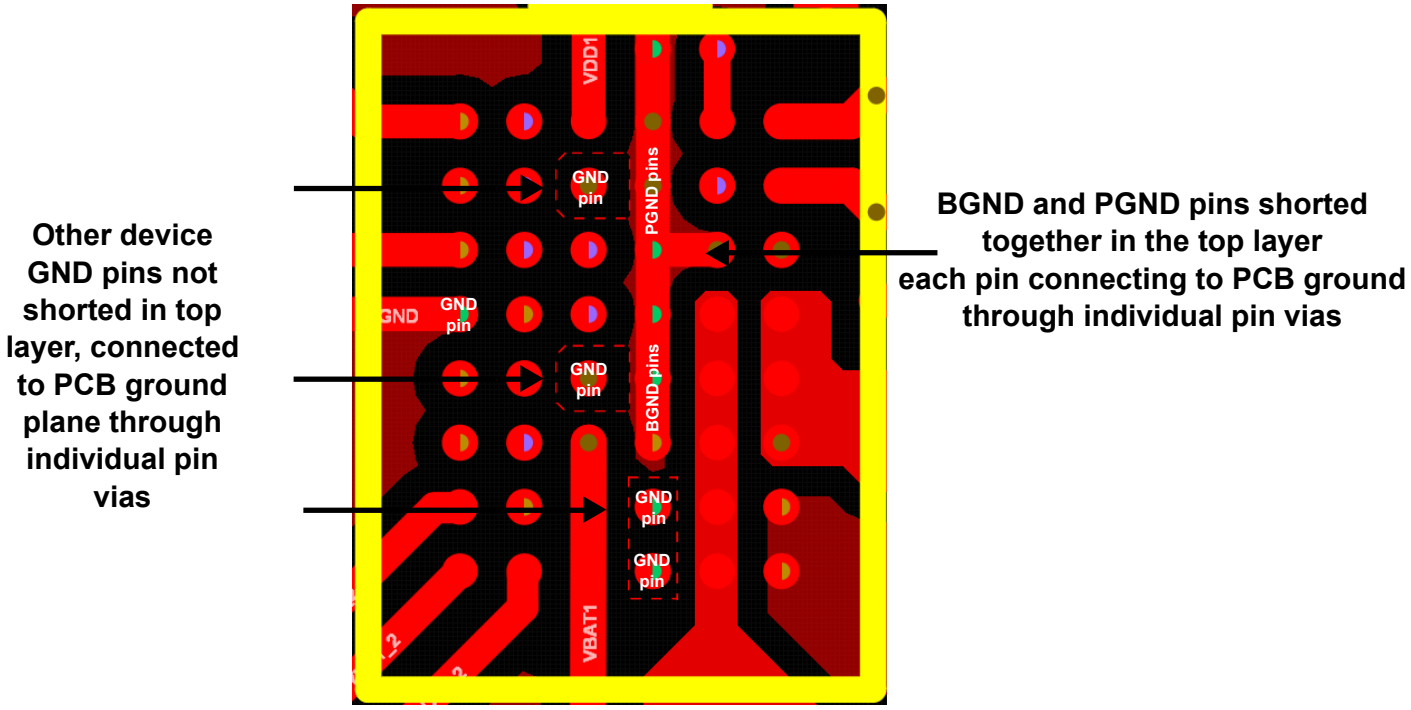

Figure 4-28. Connection of Device GND Pins on Layer 1

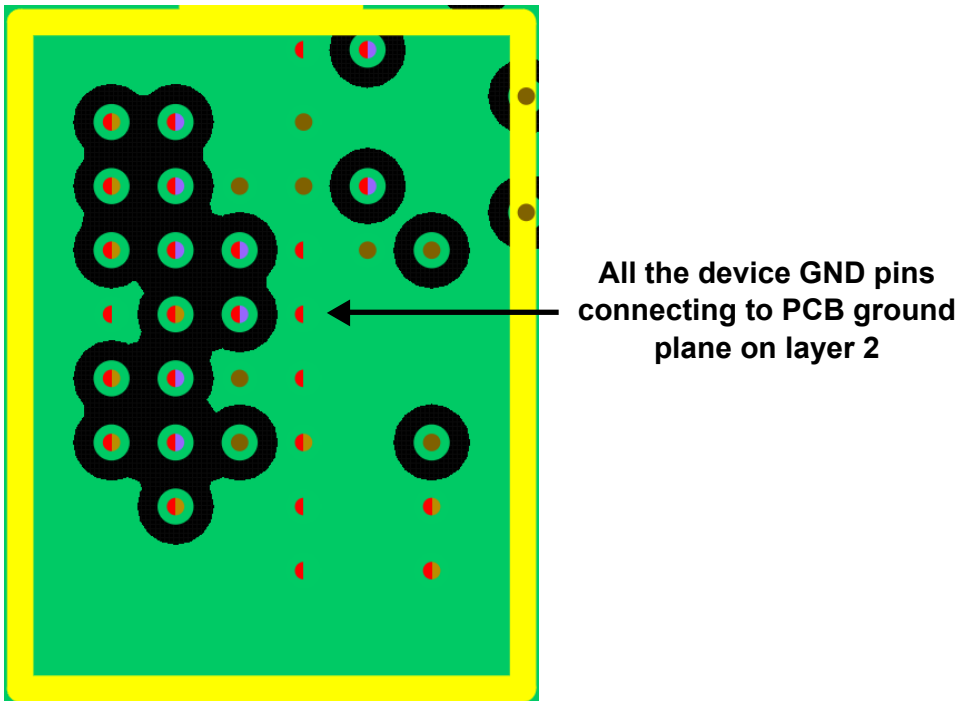

Figure 4-29. Connection to PCB GND Plane on Layer 2

5 Summary

Table 5-1 summarizes the recommended design and layout practices for the different pins of the device.

Table 5-1. Summarized Design and Layout Guidelines

Section	Pin or Section	Maximum Parasitic Trace Inductance (pH)	Recommended Guidelines
1	VDD	250	Decouple with a capacitor ≥ 2.2µF, placed as close to device as possible
2	PVDD	130	Decouple with capacitor 3 x 10µF, placed as close as possible to device
			Needs small package 0.1µF capacitor (0201) placed closest to the device, with minimal ESL
			Account for derating due to PVDD voltage
			Wide traces with high current carrying capability
3	GREG	3000	Decouple with 0.1µF capacitor to PVDD pin
			Connect directly to PVDD pin with star connection
4	SW		Place inductor as close as possible to device
			Wide traces to carry high current and minimize parasitic resistance critical for efficiency (reduced I^2R losses)
			Decouple with ≥ 10µF capacitor near inductor
			Minimize parasitic capacitance to ground to reduce switching losses
			Leave pin unconnected in external PVDD mode
5	VBAT	250	Connect directly to power source using star connection
			Decouple with ≥ 1µF capacitor, placed as close as possible to device
6	VBAT_SNS		Connect directly to power source using star connection
			Optional connection in VBAT1S mode, connect to ground if unused
7	OUT_P / OUT_N		Decouple with ≥ 1µF capacitor, placed as close as possible to device
			Wide traces capable of carrying high current
			Minimize parasitic capacitance to ground to reduce switching losses
8	VSNS_P / VSNS_N		Tap near speaker terminals (after EMI filter)
			Series resistance needed when using EMI filter (Recommended 2.2kΩ)
9	IOVDD	250	Decouple with ≥ 1µF capacitor as close as possible to device
			Can be shorted to VDD near the device pin if 1.8V is the required I/O supply. Recommended to use both C2 and C3 capacitors even when shorted, with the capacitors placed close to the VDD pin
10	DREG	250	Decouple with ≥ 1µF capacitor as close as possible to device
11	Digital		Avoid routing near high-voltage switching nodes like SW, OUT_P, OUT_N to avoid coupling
12	Ground	BGND - 35pH	Short BGND or PGND pins on top layer
		PGND - 30pH	Avoid common inductance to ground plane between PGND or BGND and GND pins
		GND - 100pH per pin	Total parasitic inductance to PCB ground critical for device performance. Use multiple vias to minimize inductance

6 References

- Texas Instruments, *TAS2573EVM User's Guide*, user's guide.
- Texas Instruments, *TAS2573 Data Sheet*, datasheet.

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