Technical Article

Solutions to ADS8686S Outputting Abnormal Fixed Values and Unresponsiveness Issue

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ADS8686S Working Principle and Key Parameter Overview

This document was translated from a simplified Chinese source. (ZHCTA18)

The ADS8686S is a 16bit 16ch dual-simultaneous-sampling SAR ADC with up to 1Msps throughput and integrated ATE features. It directly supports +-10V/+-5V/+-2.5V true bipolar analog inputs, and integrates a 1Mohm high-impedance buffer, PGA, programmable low-pass filter, reference, and reference buffer, significantly simplifying peripheral circuit design.

In fields such as industrial automation, smart grids, and high-speed test and measurement, increasingly stringent requirements are placed on the channel count, sampling synchronization, accuracy, input range, and immunity to interference for analog signal sampling. Traditional multi-channel acquisition solutions typically employ a multiplexer with a single-channel ADC or a combination of multiple discrete ADCs, which suffer from channel switching delays, poor synchronization, complex peripheral circuitry, large temperature drift, and difficulties in ensuring consistency. The ADS8686S utilizes a dual simultaneous sampling architecture, as shown in the figure below. It integrates two 16bit SAR ADC cores internally, which time-multiplex the input signals via two 9:1 MUXes respectively, enabling simultaneous sampling of up to two signals.

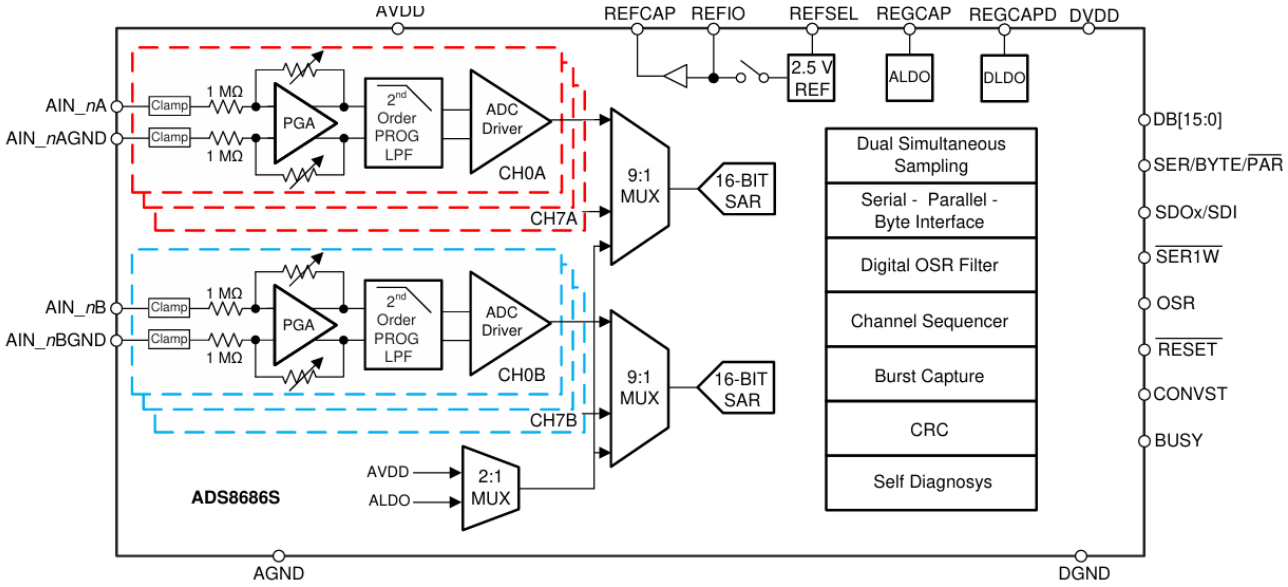

Figure 1. ADS8686S Simplified Block Diagram

Problem Description and Analysis

In smart grid application scenarios, an issue occurred where the ADS8686S exhibited abnormal outputs. The symptoms are summarized as follows:

- When power grid equipment is power cycled, the ADS8686S intermittently locks up, causing the DC output of certain channels to mismatch their inputs.
- Grounding the inputs of the channels with abnormal outputs reveals that the outputs do not change with the inputs.

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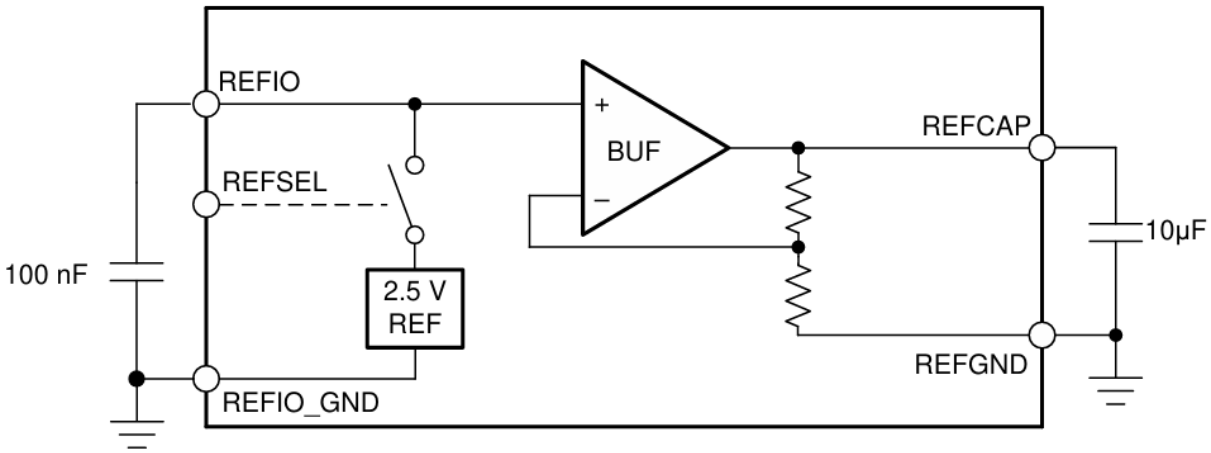
- The input and output of the reference buffer deviate from their configured values. When REFSEL is pulled high, REFIO connects to the internal 2.5V reference as the reference for the ADS8686S; actual measurements show that when the ADS8686S experiences an anomaly, REFIO drops to approximately 2.3V.



- nRESET toggle fails to recover from the issue, resulting in no response
- Power cycling restores normal operation

Experimental Reproduction

Since the issue occurs intermittently during repeated power-ups, it was suspected to be related to power supply noise, voltage slew rate, or incomplete power-down residual charge. Following experimental validation, the issue was successfully reproduced under incomplete power-down conditions. Using a programmable DC power supply, 5V AVDD was dropped to AVDD low level and then ramped back up to 5V, yielding the following test results:

AVDD low level V	REFCAP V	REFIO V	nRESET required?	Notes
5	4	2.5	N/A	Default
4	3.98	2.5	No	Recovers to normal as AVDD rises
3	2.98	2.5	No	Recovers to normal as AVDD rises
2	1.99	1.99	No	Recovers to normal as AVDD rises
1.5	1.47	1.49	No	Recovers to normal as AVDD rises
1.45	0.47	1.44	No	Recovers to normal as AVDD rises
1.443	0.47	0	Yes	AVDD ramps to 5V: 1. REFCAP=~2.3V 2. nRESET cannot recover
0.9	0	0	Yes	AVDD ramps to 5V: 1. REFCAP=~2.3V 2. nRESET can recover

Based on the above experiments and further validation across product lines, it was found that when AVDD drops to around >0.7V before power is re-applied, the issue is reproduced and cannot be reset via nRESET; when AVDD drops to <0.7V before power is re-applied, the issue also occurs, but nRESET can successfully reset and resolve the issue.

Taking the test waveforms of ramping down 5V AVDD to 0.9V and then restarting as an example, when AVDD drops from 5V to 0.9V and then rises back to 5V, the observed phenomena are as follows:

1. REFCAP decreases from 4V to 2.4V and remains stable
2. REFIO turns off, and the voltage continuously drops

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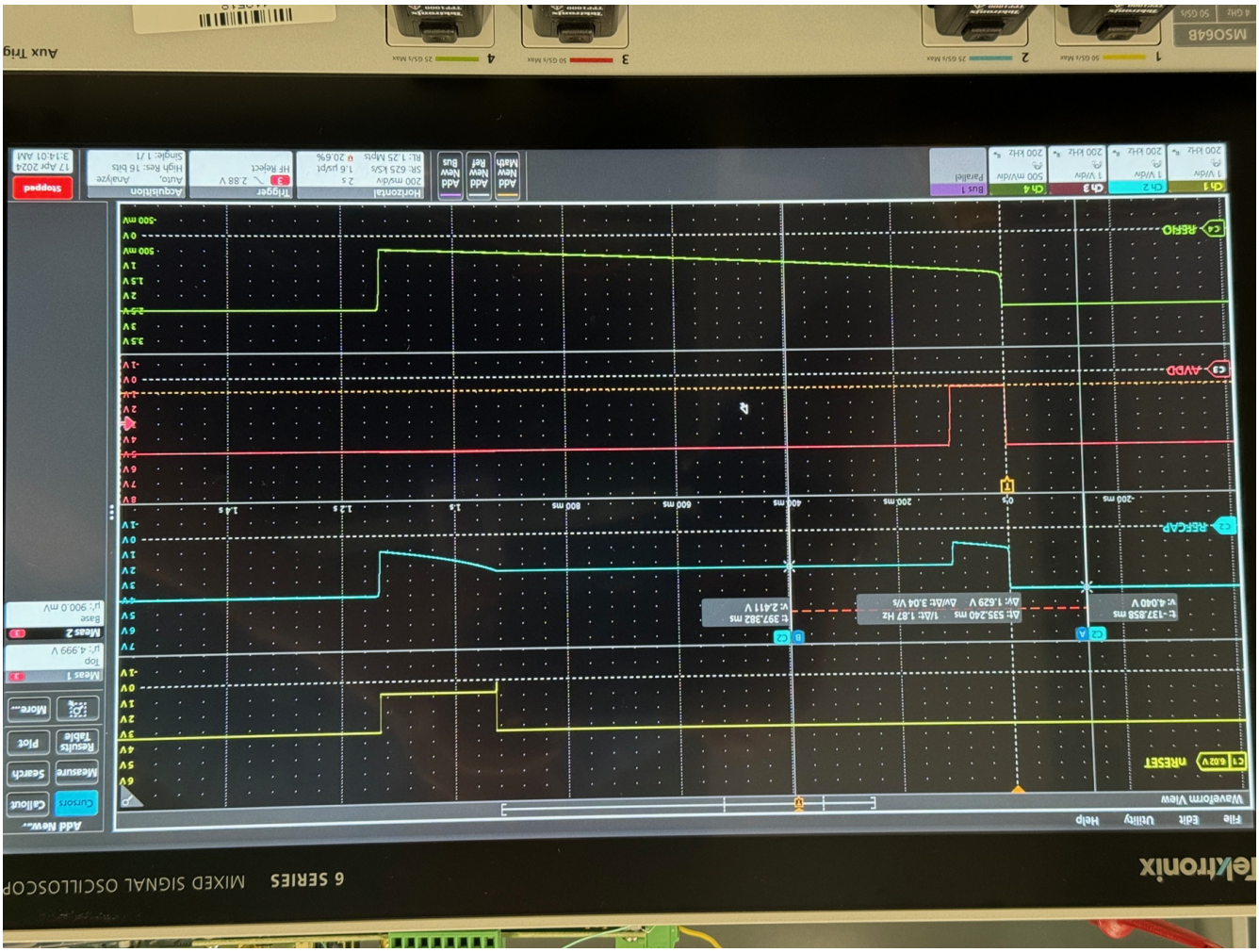
3. The abnormal output issue is reproduced

At this point, toggling nRESET results in the following phenomena:
1. REFCAP recovers to 4V
2. REFIO recovers to 2.5V
3. The abnormal output issue is resolved



Principle Analysis and Solutions

Confirmed with the design team, AVDD must discharge below the Analog POR threshold during power-down. The primary function of the Analog Power-On Reset (POR) circuit is to monitor the AVDD voltage rise during chip power-up, and forcibly hold internal digital logic—such as registers and state machines—in the RESET state until the voltage reaches a stable and reliable operating threshold. The specific functions of the POR circuit are as follows:
1. Preventing Startup Malfunction: Continuously outputs a reset signal before AVDD reaches the threshold to prevent digital circuits from executing erroneous commands under undervoltage conditions.
2. Initializing State: Ensures the chip starts execution from a known, deterministic initial state upon every power-up, rather than a random state.
3. Brown-out Detection: In addition to power-up monitoring, during normal operation, if the supply voltage unexpectedly drops below the threshold, the POR circuit re-triggers a reset to protect the system from low-voltage operation damages.

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The lockup issue with the ADS8686S output occurs because AVDD fails to drop below the 0.7V POR threshold during power-down, causing the POR circuit to not trigger and fail to output a proper analog reset signal. Consequently, even when nRESET is asserted, it cannot properly reset the ADC and digital core, leaving power cycling as the only way to resolve the state.

The final recommended solutions provided to the customer are as follows:

- Reduce AVDD capacitance to accelerate the power-down discharge rate as much as possible
- Introduce a delay between power-down and power-up to ensure AVDD discharges completely
- Keep nRESET pulled low until AVDD and DVDD are fully powered up

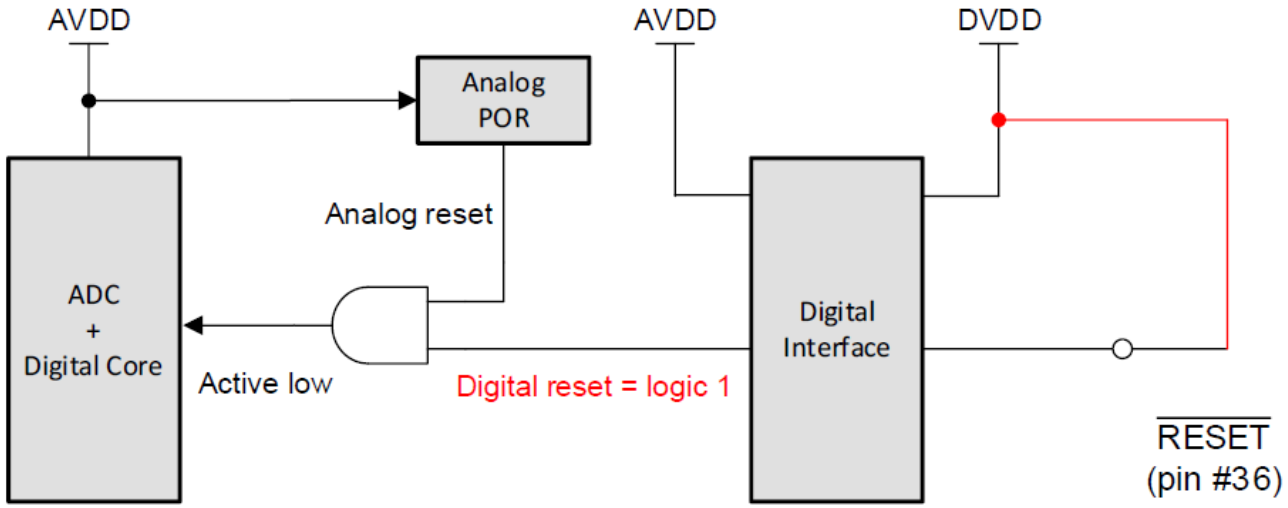

Figure 2. POR Circuit Functional Block Diagram

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