

Using matched N-JFETs for lead resistance cancellation in three-wire RTD measurements

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Three-wire sensing is a common approach to sensor interfaces where the sensor impedance is of similar magnitude to the leads connecting to the sensor. Resistance temperature detectors (RTDs) are a common example of such a sensor. A Pt100 RTD has a resistance of 100Ω at 0°C. Even 1Ω of lead resistance can contribute >2.5°C of error to the measured temperature. In a three-wire measurement, matched current sources are used to ensure that the voltage drop across the sensor connecting leads are equal and therefore can be removed from the measurement.

Figure 1 illustrates a three-wire, ratiometric, RTD measurement circuit that employs a monolithic, dual, N-channel JFET, the **JFE2325**, and two resistors as a simple, low-cost, approach to creating two matched current sources. This solution is also able to operate at relatively low supply voltages. The voltage drop across the JFET current source circuit only needs to be above the pinchoff voltage of the JFET, 1.08V in the case of the JFE2325, to operate properly.

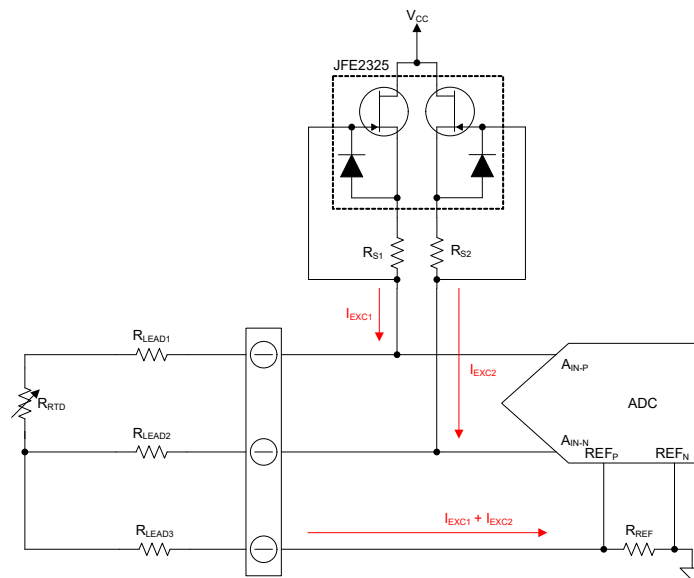


Figure 1. Three-wire, ratiometric RTD measurement using the JFE2325 dual JFET as matched current sources

To understand the benefit of the three-wire approach, we can derive the equations for the voltage at each input to the ADC:

$$V_{AIN-P} = I_{EXC1}(R_{LEAD1} + R_{RTD}) + (I_{EXC1} + I_{EXC2})(R_{LEAD3} + R_{REF}) \quad (1)$$

$$V_{AIN-N} = I_{EXC2}(R_{LEAD2}) + (I_{EXC1} + I_{EXC2})(R_{LEAD3} + R_{REF}) \quad (2)$$

If $R_{LEAD1} = R_{LEAD2} = R_{LEAD}$ and $I_{EXC1} = I_{EXC2} = I_{EXC}$, then the differential input voltage sensed by the ADC can be simplified to **Equation 3**:

$$V_{ADC} = V_{AIN-P} - V_{AIN-N} = I_{EXC}(R_{LEAD} + R_{RTD}) + 2I_{EXC}(R_{LEAD3} + R_{REF}) - I_{EXC}R_{LEAD} - 2I_{EXC}(R_{LEAD3} + R_{REF}) = I_{EXC}R_{RTD} \quad (3)$$

The voltage drop across the third lead and the reference resistor are common to both ADC inputs and are therefore removed.

Lastly, because the measurement is ratiometric, the absolute value of the excitation current and its stability over temperature is not as important as the matching between the two current sources. The ADC output only depends on the ratio of the RTD resistance to the reference resistance as shown in **Equation 4**:

$$\text{Output Code} = 2^n - 1 \times \frac{V_{RTD}}{V_{REF}} = 2^n - 1 \times \frac{I_{EXC}R_{RTD}}{2 \times I_{EXC}R_{REF}} = 2^{n-2} \times \frac{R_{RTD}}{R_{REF}} \quad (4)$$

Current source calculations

A very simple JFET current source is formed by placing a resistor in series with the source of an N-JFET and connecting the gate below the resistor as shown in **Figure 2**. As current flows through the source resistor R_S , the resistor raises the voltage at the JFET source with respect to its gate, further pinching off the JFET channel and regulating the drain-to-source current, I_{DS} , through negative feedback.

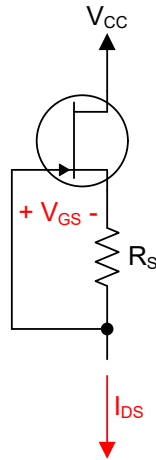


Figure 2. A simple JFET current source formed by connecting the gate below a source resistor

The simplest method to determine the output current of the JFET current source is to use the I_{DS} versus gate-to-source voltage (V_{GS}) curve from the JFET datasheet. This curve for the JFE2325 is reproduced in **Figure 3**.

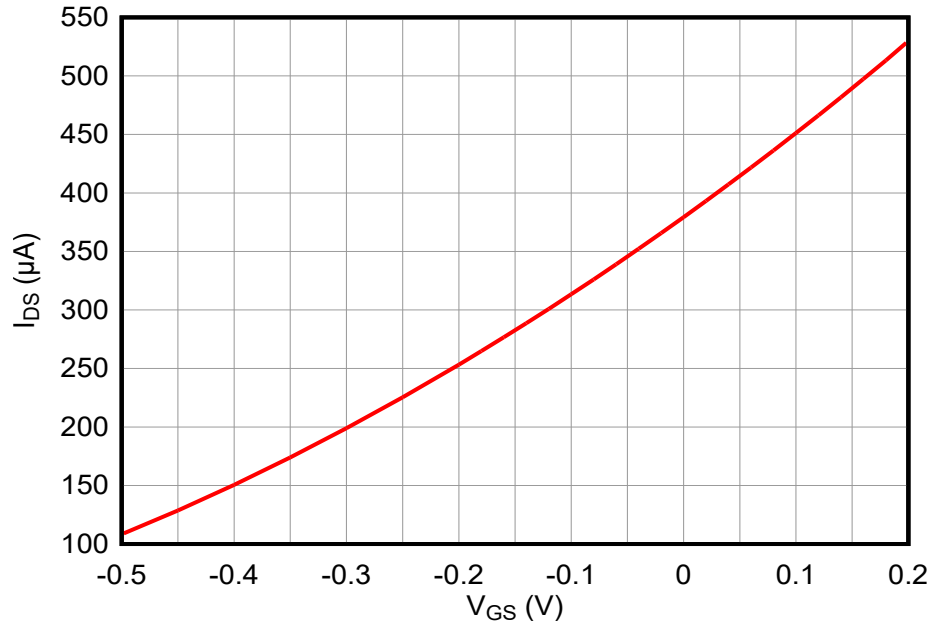


Figure 3. Drain-to-source current (I_{DS}) vs gate-to-source voltage (V_{GS}) for the JFE2325

Considering that the voltage drop across R_S is equivalent to the gate-to-source voltage but with opposite polarity, the value for R_S can be calculated for the necessary V_{GS} to produce the desired I_{DS} , shown in [Equation 5](#):

$$V_{GS} = -I_{DS}R_{DS} \rightarrow R_S = \frac{-V_{GS}}{I_{DS}} \quad (5)$$

From [Figure 3](#), we can see that for a drain current of $200\mu A$, the JFE2325 requires a V_{GS} of $-0.3V$. Inserting this value into [Equation 5](#), we solve for R_S in [Equation 6](#):

$$R_S = \frac{-V_{GS}}{I_D} = \frac{-(-0.3V)}{200\mu A} = 1.5k\Omega \quad (6)$$

I_{DS} can be directly calculated if the JFET pinchoff voltage, V_P , and drain-to-source saturation current, I_{DSS} , are known, from [Equation 7](#):

$$I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad (7)$$

Inserting [Equation 5](#) for V_{GS} gives [Equation 8](#):

$$I_{DS} = I_{DSS} \left(1 - \frac{-I_{DS}R_S}{V_P}\right)^2 = I_{DSS} \left(1 + \frac{I_{DS}R_S}{V_P}\right)^2 \quad (8)$$

[Equation 8](#) can be expanded and put into the standard quadratic form ($ax^2 + bx + c = 0$) and solved using the quadratic equation ([Equation 9](#) and [Equation 10](#)):

$$\left(\frac{I_{DSS}R_S^2}{V_P^2}\right)I_{DS}^2 + \left(\frac{2I_{DSS}R_S}{V_P} - 1\right)I_{DS} + I_{DSS} = 0 \quad (9)$$

$$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \quad (10)$$

Where a, b, and c are defined in [Equation 11](#), [Equation 12](#), and [Equation 13](#):

$$a = \left(\frac{I_{DSS} R_S^2}{V_P^2} \right) \quad (11)$$

$$b = \left(\frac{2I_{DSS} R_S}{V_P} - 1 \right) \quad (12)$$

$$c = I_{DSS} \quad (13)$$

This approach will give two roots, but only one of the two will be a valid value for output current from the current source. Using typical values for I_{DSS} and V_P for the JFE2325, 385 μ A and -1.079V, gives an I_{DS} of 200.4 μ A with a 1.5k Ω source resistor.

Estimating mismatch between the two current sources

Calculating mismatch between the two current sources requires investigating the impact of mismatch in the JFET parameters on the resulting output current. Discrete JFETs have extremely wide tolerances on their I_{DSS} and V_P values. However, because the two JFETs in the JFE2325 are built on the same die using modern IC layout techniques, the parameters of the two JFETs closely match each other. [Figure 4](#) is a production histogram of the I_{DSS} mismatch of the two JFETs in the JFE2325, taken from over 74,000 units. It can be seen from the histogram that the I_{DSS} of the two JFETs matches to 2% within three standard deviations of the mean. The maximum I_{DSS} mismatch, which indicates six standard deviations from the mean, is specified to 5% in the datasheet of the JFE2325.

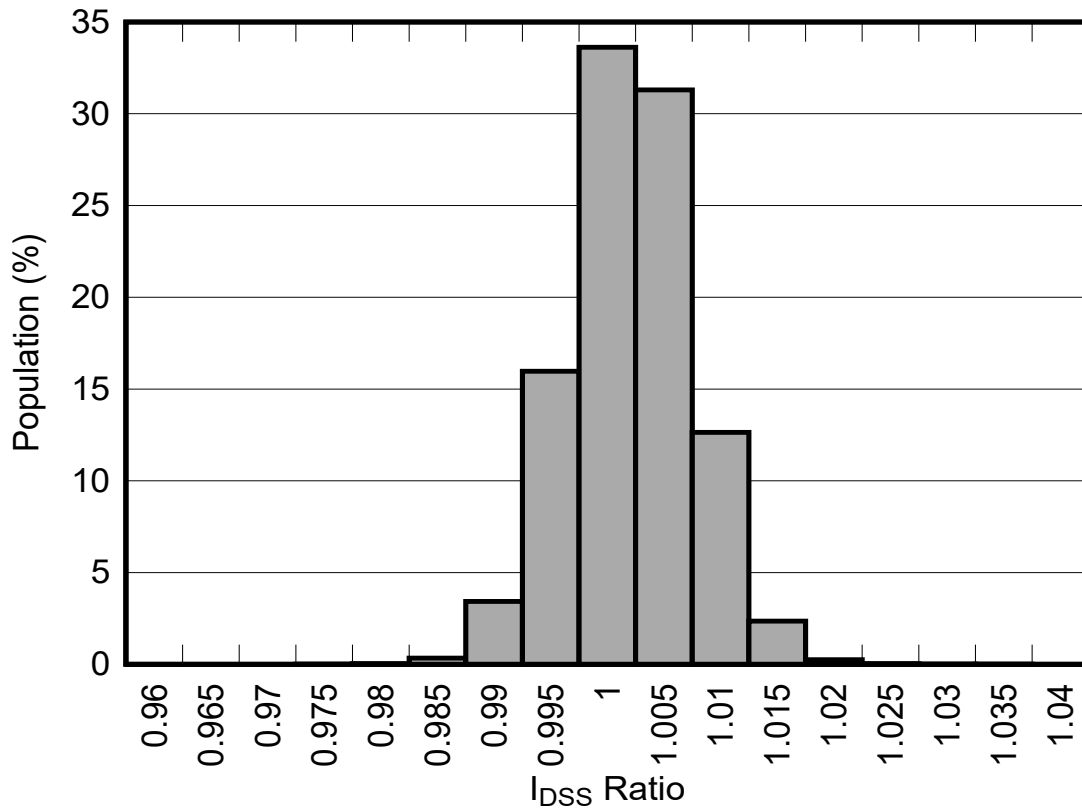


Figure 4. Production histogram of I_{DSS} mismatch between the two internal JFETs of the JFE2325

JFET I_{DSS} and V_P are not independent parameters. Rather, the two quantities are correlated such that any increase in I_{DSS} will result in a V_P further from zero. **Figure 5** shows this correlation between I_{DSS} and V_P (called gate-to-source cutoff voltage, V_{GSC} , in the plot) for the JFE2325.

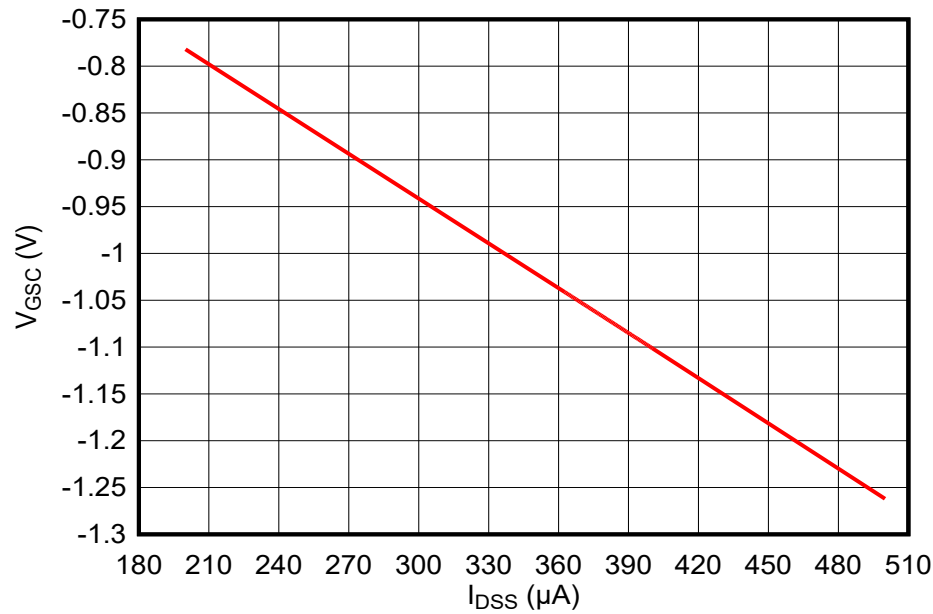


Figure 5. Pinchoff voltage, or gate-to-source cutoff voltage (V_{GSC}) vs I_{DSS} of the JFE2325

We can extract a linear equation from this plot to estimate the pinchoff voltage for a JFET given a certain I_{DSS} value, giving **Equation 14**:

$$V_P = -1592.6 \times I_{DSS} - 0.4656V \quad (14)$$

Table 1 shows the values for I_{DSS} and V_P for three possible JFETs in the JFE2325 along with the resulting I_{DS} . JFET1 is a nominal case for an internal JFET. JFET2 has a 2% mismatch in I_{DSS} compared to JFET1, which is equivalent to a unit three standard deviations from the mean. JFET3 has a 5% mismatch in I_{DSS} compared to JFET1, equivalent to a unit six standard deviations from the mean.

	I_{DSS}	V_P	I_{DS} ($R_S = 1.5k\Omega$)
JFET1 (Nominal)	385.0 μA	-1.079V	200.4 μA
JFET2 (2% Mismatch)	377.3 μA	-1.066V	197.1 μA
JFET3 (5% Mismatch)	365.8 μA	-1.048V	192.2 μA

Table 1. Possible parameters for mismatched JFETs in the JFE2325

The resulting I_{DS} for a current source built from each JFET is calculated by solving **Equation 9** with the respective values for I_{DSS} and V_P . The mismatch in current sources is calculated in **Equation 15** and **Equation 16**:

$$\text{Mismatch}(\pm 3\sigma, \%) = 100 \times \frac{|200.4\mu A - 197.1\mu A|}{200.4\mu A} = 1.647\% \quad (15)$$

$$\text{Mismatch}(\pm 6\sigma, \%) = 100 \times \frac{|200.4\mu A - 192.2\mu A|}{200.4\mu A} = 4.092\% \quad (16)$$

It can be instructional to also view the I_{DS} versus V_{GS} plot with a load line added for the source resistor R_S as shown in **Figure 6**. The I_{DS} value will be where the curve for the JFET and the load line for R_S intersect.

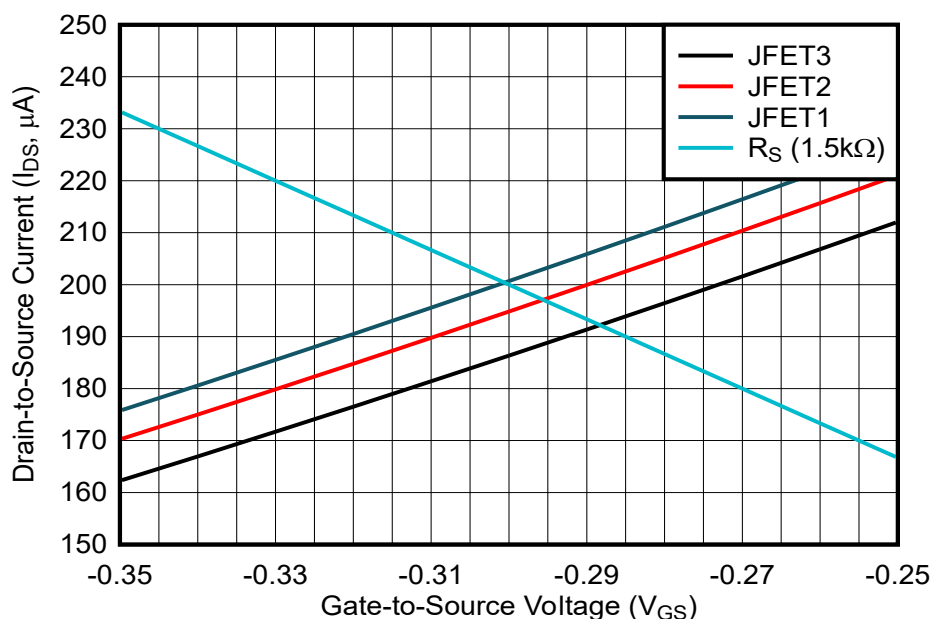


Figure 6. I_{DS} vs V_{GS} plot for the three JFETs given in Table 1 with a $1.5k\Omega$ load line

Notice that the lower I_{DSS} devices, JFET2 and JFET3, intersect the R_S load line at V_{GS} values closer to zero, effectively pinching off the JFET channel less. Conversely, if the JFET I_{DSS} were increased, R_S would force the V_{GS} further from 0V and pinch off the JFET channel more. This is why a 2% mismatch in I_{DSS} values of the JFETs does not result in a 2% mismatch in output current from the current sources. Increasing R_S will reduce the mismatch between the two current sources, but with the downside of decreasing the output current of the current source.

Conclusion

Three-wire configurations are a common and effective way to remove the errors introduced by lead resistance to RTD measurements. However, three-wire systems require a pair of well-matched current sources to effectively remove errors. A simple method to create these matched current sources is to use a monolithic pair of N-JFETs such as the JFE2325. The JFE2325 includes two, well-matched, JFET devices on the same die inside of an extremely small $0.8\text{mm} \times 1\text{mm}$ package. Because the two JFETs share the same silicon area, their parameters match each other far better than discrete single JFETs. Furthermore, adding a source resistor to the JFETs introduces negative feedback which reduces variation in the output current due to changes in the JFET parameters. This approach delivers two current sources with exceptional matching at a very low cost, small solution size, and able to operate over a wide range of power supply voltages.

References

1. Wu, Joseph, "[A Basic Guide to RTD Measurements](#)."
2. Texas Instruments, [JFE2325 Dual, Low-Power, N-Channel JFET for Electret Microphones](#).

About the author

John Caldwell is a technologist for the linear amplifiers BU where he works across all product lines to define the next generation of high performance signal conditioning amplifiers. John has more than 15 years of experience in linear amplifier development and precision, low noise, circuit design. John received his B.S. and M.S. in electrical engineering from Virginia Tech, holds 3 U.S. patents, and has published more than 30 articles.

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