Technical White Paper

MSPM33 MCU Advantages in Body Electronics and Lighting Applications

ABSTRACT

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Trademarks

1 Introduction

The global automotive industry is in a defining phase of a technological transformation, with body electronics and lighting emerging as a primary battleground for MCU innovation. Microcontroller units (MCUs) have transitioned from simple peripheral switches to the vital neural network powering next-generation vehicular comfort, style, and safety. Driven by the aggressive adoption of smart cockpits, dynamic LED matrix lighting, and zone-control architectures, body electronics now command a massive share of the semiconductor footprint of the vehicle. This strategic shift is fundamentally reshaping supply chains, demanding high-efficiency, multi-channel MCUs capable of managing complex cabin automation and adaptive lighting systems while providing localized supply security for global automakers.

2 The Three Entry Barriers for Automotive Chips

Unlike consumer electronics, automotive-grade semiconductors must clear three extreme thresholds:

1. Functional safety (ISO 26262): ASIL B is now the baseline for body and comfort controls. High-risk failures—like a malfunctioning window anti-pinch mechanism—demand ≥90% single-point fault coverage to prevent injury.
2. Reliability (AEC-Q100): chips undergo harsh testing, including 2,000 hours of high-temperature aging (125°C), 1,000 thermal cycles (-55°C to 150°C), and 50G mechanical vibration. The chips must deliver a 10+ year lifespan with a failure rate under 1 FIT.
3. Supply chain resilience: to match the 3 to 5 year vehicle development cycle, suppliers must dedicate independent production lines to help achieve 15+ years of stable supply longevity.

3 Advantages of MSPM33 in Automotive BEL Applications

Designed for ASIL B compliant automotive systems, the MSPM33 aims to improve the body electronics market by delivering the a synergy of safety, affordability, and streamlined development.

3.1 Hardware and Chip-Level Features

These advantages are physically designed into the silicon, manufactured on the wafer, and verified through component-level automotive qualification:

- Remarkable single-core self-test architecture
  - Targeted ASIL B functional safety through unique hardware-driven self-test mechanisms integrated directly into the single-core silicon layout, eliminating the need for traditional lockstep secondary cores.
- 40% hardware bill-of-materials (BOM) cost reduction
  - The single-core design drastically reduces die size and optimizes packaging, slashing hardware BOM costs by up to 40% compared to market competitors utilizing dual-core lockstep designs.
- AEC-Q100 Grade 1 automotive qualification
  - The physical chip is fully qualified for harsh automotive environments, providing electrical and mechanical stability across a wide operating temperature range from –40°C to 125°C.
- Automotive-grade zero-defect manufacturing
  - Manufactured in specialized fabrication and assembly sites under strict IATF 16949 and ISO 9001 quality management systems, fully audited by Bureau Veritas® (BV) to prevent physical and systematic faults.

3.2 Software and Ecosystem Support

This layer consists of the software stack running on top of the silicon and the comprehensive documentation provided to accelerate customer compliance and time-to-market:

- Production-ready Microcontroller Abstraction Layer (MCAL) software support
  - Includes the MCAL software out-of-the-box, delivering the essential core component defined within the standard AUTOSAR basic software layer.
- Third-party Automotive Open System Architecture (AUTOSAR®) ecosystem compatibility
  - Offers native compatibility with industry-standard third-party AUTOSAR development suites, such as Elektrobit (EB) Tresos®, significantly lowering software migration barriers.
- Streamlined design and reuse efficiency
  - Leverages a modular and layered software architecture to simplify client development cycles, enabling the creation of safe, highly efficient, and highly reusable automotive electronic systems.
- Audit-ready compliance and delivery documentation
  - Provided with comprehensive ISO 26262 functional safety packages; clients can also request and instantly download complete production part approval process (PPAP) documentation through ti.com.

3.3 MSP Edge AI Capability

The MSP Edge AI microcontroller delivers leading performance in low latency and power efficiency by integrating a dedicated hardware accelerator called the TinyEngine™ NPU. This cost-effective design supports a wide range of neural network layers and mixed data types (including 8-bit, 4-bit, and 2-bit weights), while featuring flexible CPU and DMA integration to seamlessly offload unsupported layers back to the main CPU.

The MSP microcontrollers support three primary machine learning modalities to process sensor data efficiently at the edge: classification, fault and anomaly detection, and regression.

- *Classification* aims to categorize unseen 1D, multi-dimensional, or 2D image data into predefined classes, such as identifying motion types from a 3-axis accelerometer or recognizing shapes.
- *Fault and anomaly detection* focuses on identifying abnormal system behaviors within 1D and multi-dimensional time-series data, enabling applications like ECG rhythm analysis, arc fault detection, and predictive maintenance for motors.
- Lastly, *regression* maps the sensor inputs—including PIR, audio, and voltage data—to a continuous scale rather than discrete categories, allowing systems to predict future continuous states based on real-time input data.

4 MSPM33C32 Overview

The first MSPM33C32xx-Q1 has been released to market:

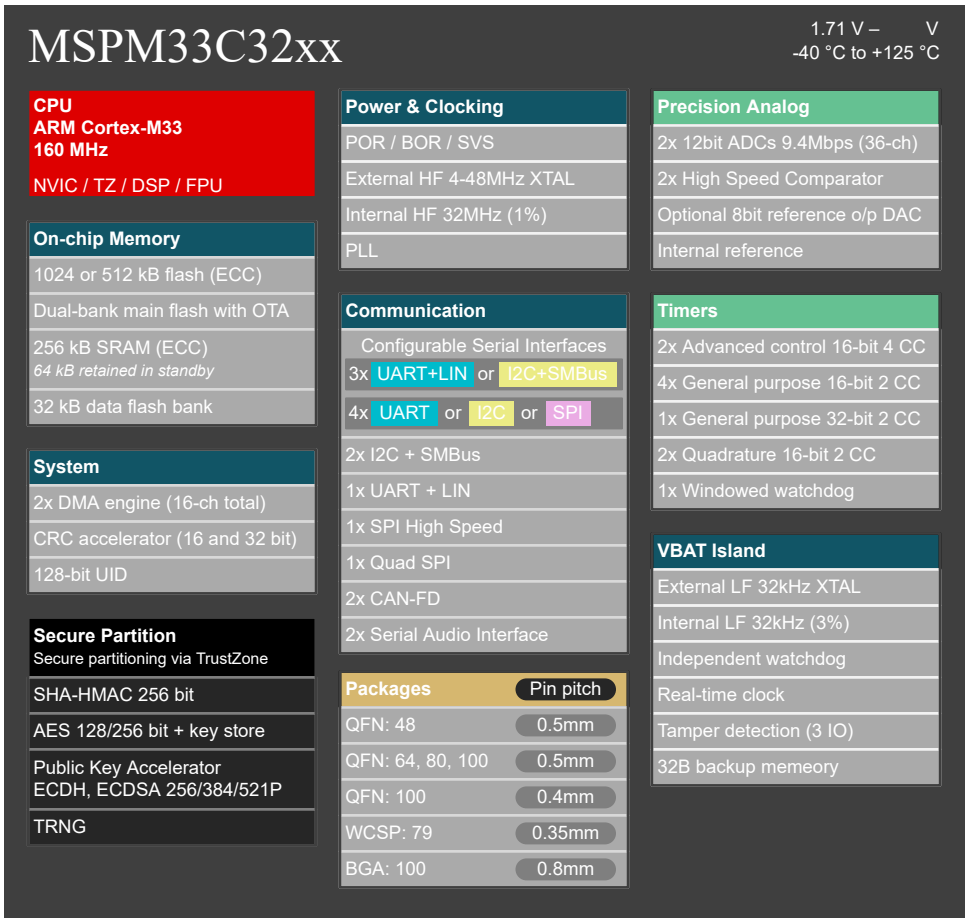

Figure 4-1. MSPM33C32xx-Q1 (ASIL B) is 160MHz M33C MCU With Up to 1MB Flash, Secure Boot, QSPI, and Audio-TDM MCU

- Advanced compute engine
  - Core: 160 MHz Arm® Cortex®-M33 CPU equipped with TrustZone®, floating point unit (FPU), and DSP extensions.
  - Memory architecture: integrated up to 1MB dual-bank main flash (enabling seamless OTA and address swap firmware updates) and 256KB SRAM. Both memories feature full hardware error correction code (ECC) protection.
  - Data storage: built-in 32KB data flash bank.
- Integrated high-performance analog
  - Dual SAR ADCs: two 12-bit SAR ADCs achieving high throughput up to 8Msps+, supporting up to 36 total channels.
  - Analog comparators: two high-speed, low-power analog comparators mapped with internal and optional 8-bit reference output DACs.
- Control timers and actuators
  - Motor control: advanced control timers that can drive up to four DC motors or two BLDC motors.
  - Timer suite: complete array of timers including two advanced control (16-bit 4 CC), four general purpose (16-bit 2 CC), one general purpose (32-bit 2 CC), and two quadrature (16-bit 2 CC).
- Robust connectivity interfaces

  - Dual CAN-FD: two CAN-FD controllers delivering high-speed automotive network throughput up to 5Mbit/s.
  - Quad SPI (QSPI): one QSPI interface delivering high-throughput data storage and display connectivity at 20MBps.
  - UNICOMM architecture: flexible, reconfigurable serial interfaces supporting up to eight UART, five SPI, or nine I²C instances.
  - Audio interfaces: two serial audio interfaces supporting up to 4 serial audio channels with I^2S and 16 TDM slots.
- Silicon security and systematic safety
  - Hardware trust root: Platform Security Architecture (PSA) Certified Level 2 using the Security Evaluation Standard for Internet of Things Platforms (SESIP) for the immutable root of trust (RoT) with secure boot and secure firmware installation.
  - Crypto accelerators: dedicated hardware execution units for AES-256, SHA-256, ECDH and ECDSA, and a 32-bit true random number generator (TRNG).
  - Fault management: dual DMA engines (16-channel total), CRC hardware accelerator (16-bit and 32-bit), 128-bit UID, along with windowed and independent watchdog timers (WDTs).
- VBAT isolated island
  - Features an isolated battery-backed domain embedding an independent watchdog, a real-time clock (RTC), external and internal LF 32kHz oscillators, 32B backup memory, and Tamper Detection (three IOs).
- Physical specifications
  - Temperature grade: AEC-Q100 Grade 1 qualified for harsh environments (–40°C to 125°C).
  - Supply voltage: wide operating range from 1.71V to 3.63V.
  - Packaging options: available in 48-pin VQFN (7mm x 7mm ，0.5mm pitch), 64-pin LQFP (12mm x 12mm, 0.5mm pitch), 80-pin LQFP (14mm x 14mm, 0.5mm pitch), 100-pin LQFP (16mm x 16mm, 0.5mm pitch), 100-pin LQFP (14mm x 14mm, 0.4mm pitch) and 100-pin nFBGA (9mm x 9mm, 0.8mm pitch).

5 Headlight Application

1. Rich tailored peripherals
   - 20x PWM channels: drives multiple LED strings, matrices, cooling fans, and stepper motors (light position).
   - 20x ADC channels: provides simultaneous multi-channel sampling for precise NTC temperature and voltage monitoring.
2. Dense communication matrix
   - Four CAN-FD: Enables high-speed backbone communication with the Body Control Module (BCM) or off-board networks.
   - Four SPI: an excellent choice for high-speed, multi-channel control of premium LED drivers (for example, TPS92682 and TPS92520).
   - Three UART and 2x I2C: Connects seamlessly with local DC/DC regulators and auxiliary sensors.
3. High performance and computation
   - 160MHz Cortex®-M33 with FPU: delivers plenty of math-heavy processing power needed for complex matrix LED/ADB pixel-level algorithms without latency.
4. Advanced security and memory
   - Arm TrustZone and Immutable RoT: secures firmware against hacking, providing secure boot and hardware-isolated partitions.
   - Large Memory with ECC: up to 1MB Flash and 256kB SRAM with error correction code (ECC) to prevent data corruption caused by harsh automotive EMI.
5. Seamless automotive ecosystem
   - AUTOSAR support: includes MCAL drivers to fast-track standard automotive software development.

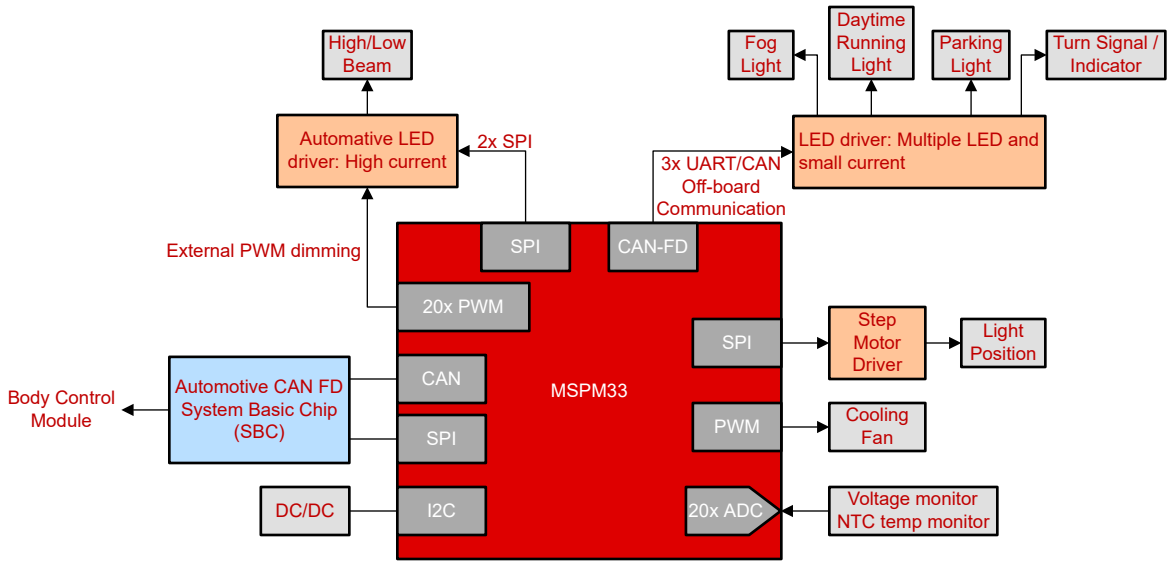

Figure 5-1. Headlight Application Block Diagram

6 Body Control Module Application

1. Robust domain gateway (communications)
   - CAN-FD and LIN integration: simultaneously manages high-speed backbone vehicle data (through SBC) and localized low-cost lighting and mirror networks.
   - Dual I2S interfaces: directly drives two Speaker Drivers to output welcome chimes, blind-spot alerts, or click sounds.
2. High-speed memory expansion (compute and memory)
   - XSPI: connects to high-speed external flash to store complex dynamic light image arrays (puddle lamps) and high-quality audio files.
3. Comprehensive input and output coordination
   - MSDI integration (through SPI): effortlessly aggregates dozens of physical switch statuses (windows, lock and unlock, child lock) from a multi-switch detection interface.
   - Motor control (through SPI or PWM): seamlessly controls smart gate drivers (DRV series) for heavy-load body motors like window lifts, soft close, and door handles.
   - Analog monitoring (ADC or I2C): gathers multi-channel inputs from ambient temperature and position sensors.

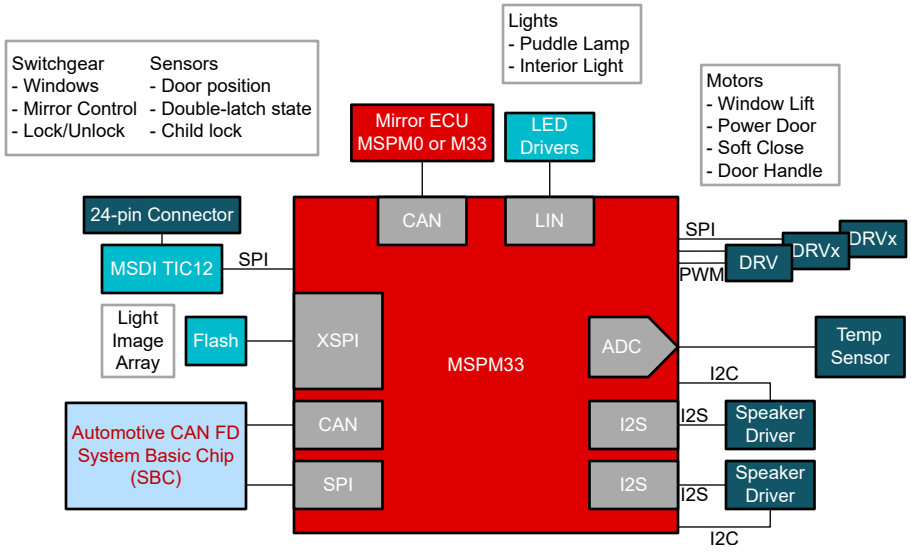

Figure 6-1. Body Control Module Application Block Diagram

7 Resources

Please ask the sales team for access to documents in mySecure to help develop your project.

- Texas Instruments, MSPM33C321A-Q1, product page.
- Texas Instruments, LP-MSPM33C321A, product page.
- Texas Instruments, Functional Safety, webpage.
- Texas Instruments, MCAL Access Link, MCAL (available upon request).
- Texas Instruments, EB Tools Access Link, EB Tools (available upon request).

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