

High-Speed Voltage-Controlled Current Source (VCCS) for Transient Load Testing and Laser Driver



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Abstract

As data-center computing demands higher-performance power management, the need for precise transient response testing becomes critical. This technical white paper presents a high-speed, high-current voltage-controlled current source (VCCS) optimized for applications such as electronic load, laser drivers. The design focuses on achieving a rapid rise-time (100ns) and high output current (up to 150A pulsed) while maintaining stability and voltage compliance. The paper details a comprehensive design procedure, covering critical component selection for power MOSFETs (focusing on saturation region operation, input capacitance, and safe operating area), sense resistor optimization to balance power dissipation and ESL-induced rise-time constraints, and opamp selection based on bandwidth, slew rate, and output current requirements. Additionally, the document evaluates various circuit architectures, including the use of damping resistor (R_{damp}) and dual-feedback topologies to suppress parasitic oscillations and optimize settling time for modern GPU and CPU power supply applications.

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1 Introduction

The rapid growth of data-center computing increases the demand for high-performance systems with efficient power management. A transient load tester is a circuit that creates rapid changes in load current to evaluate the transient response and stability of a power delivery system. Such testing helps assess how effectively a system handles sudden changes in power demand. A voltage-controlled current source (VCCS) provides a programmable load current for implementing a transient load tester. The output current is controlled by an input voltage using a closed-loop opamp, power FET, and precision sense resistor. This reference design presents VCCS implementations optimized for different requirements and high-speed operation. This design supports accurate power delivery testing for modern GPU and CPU power supply and data-center applications.

1.1 Design Summary

Table 1-1. Design — High-current, High-speed VCCS

Parameter	Goal
Output Current (Maximum)	150A (pulsed)
Rise Time (10%–90%)	100ns
Voltage Compliance (Min)	0.4V
Trans-conductance (I_{OUT}/V_{IN})	500A/V

2 Theory of Operation

2.1 Circuit Overview

Figure 2-1 shows the core topology of the VCCS implemented in this design. The circuit consists of an opamp driving the gate of a power FET, with a precision sense resistor placed in the source path of the FET. The voltage developed across the sense resistor is fed back to the inverting input of the opamp, completing the negative feedback loop. The governing transfer function is:

$$I_{OUT} = \frac{V_{IN}}{R_{sense}} \quad (1)$$

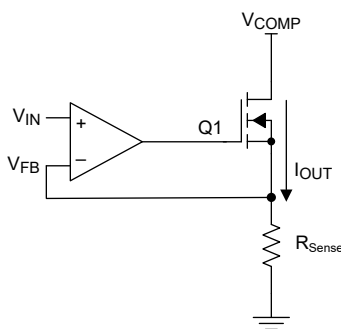


Figure 2-1. Opamp Controlled Constant Current Source

2.2 Closed-loop Operation

The loop operates as follows:

1. The input control voltage V_{IN} is applied to the non-inverting terminal of the opamp.
2. The opamp compares V_{IN} with the feedback voltage V_{FB} , which is the voltage developed across the sense resistor due to the drain-to-source current flowing through the FET.
3. Any difference between V_{IN} and V_{FB} (the error signal) is amplified by the opamp and used to drive the gate of the FET.
4. The FET responds to the gate drive by modulating channel conductance, thereby adjusting the current flowing through the sense resistor.
5. The loop reaches equilibrium when $V_{FB} = V_{IN}$

At this steady-state condition, the output current is precisely determined by the input voltage and the sense resistance, independent of the load impedance, which is the defining characteristic of an ideal current source as shown in [Equation 1](#)

2.3 FET Operation Region

In a voltage-to-current converter (V2I), the MOSFET must operate strictly in the saturation region to function as an ideal voltage-controlled current source. In saturation, the drain current I_D is governed solely by V_{GS} and is independent of V_{DS} , giving the FET a high and well-defined trans-conductance g_m . This makes sure that any step applied at the gate by the opamp is promptly and proportionally reflected at the source, allowing the feedback loop to settle quickly and accurately to the desired output current. However, if the FET is allowed to enter the ohmic (linear) region $\rightarrow$ where $V_{DS} < (V_{GS} - V_{th}) \rightarrow$ the device no longer behaves as a current source but instead transitions into a voltage-controlled resistor. In this region, the drain current becomes a function of both V_{GS} and V_{DS} , causing the effective trans-conductance g_m to collapse significantly. As a result, when the opamp applies a step change at the gate, only a very small fraction of that step is replicated at the source — the gate-to-source signal transfer is severely attenuated. The feedback loop technically remains closed, but operating with a drastically reduced effective gain. This reduced effective gain forces the opamp to drive the gate harder and harder in an attempt to correct the error, yet each correction yields only a weak response from the FET. The loop continues to iterate through this low-gain corrective process, causing the output to settle very slowly before finally reaching the intended current level.

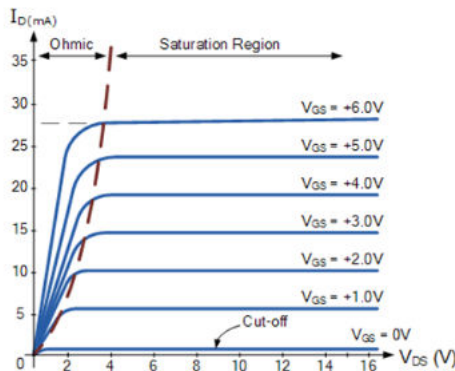


Figure 2-2. FET Characteristics Curve

3 Design Procedure

This section discusses the selection of FET, R_{sense} and opamp.

3.1 Choosing FET

The design process initiates with the selection of the FET, which is governed by three primary performance metrics:

1. Input Capacitance, C_{iss}
2. Compliance Voltage Range
3. Safe Operating Area, SOA

3.1.1 C_{iss}

In any practical gate drive circuit, parasitic inductance exists in the gate trace and bond-wire connections. The gate inductance, combined with the total effective capacitance at the gate node C_{eff} , including C_{iss} forms an LC tank circuit. An undamped LC rings at a natural resonant frequency when a fast step reaches the gate, causing oscillations in V_{GS} and consequently in the output current, severely degrades transient response. A damping resistor R_{damp} placed in series with the gate suppresses these oscillations by introducing sufficient resistance into the LC loop, critically damping the resonance and producing a clean, non-oscillatory gate-voltage transition.

The value of R_{damp} must satisfy a key condition: R_{damp} must be significantly larger than the output resistance R_o of both op amps and the FET's internal gate resistance R_g . Since both R_o and R_g are typically very small in high-speed designs, the combination becomes negligible compared with total series resistance at the gate node, making R_{damp} the dominant resistance in the gate drive path. A practical value of 5Ω is selected for R_{damp} satisfying the condition $R_{damp} \gg R_o$, and R_g , while keeping the gate-drive speed within the required range.

Since R_{damp} is the dominant resistance at the gate node, the RC network forms a first-order low-pass filter with C_{eff} , and the bandwidth of this RC network is given by $1 / (2\pi \times R_{damp} \times C_{eff})$. This pole governs how fast the gate voltage can respond to a step input from the opamp, effectively setting the rise-time of the entire system. Therefore, to meet the required rise-time specification, the bandwidth of the RC filter must be greater than or equal to the response bandwidth. $BW \geq 0.35 / T_{rise}$, (T_{rise} represents the desired rise-time). This condition directly constrains the maximum permissible value of C_{eff} and consequently C_{iss} of the selected FET.

Assuming a first-order system, the required bandwidth relates to the rise-time according to [Equation 2](#).

$$BW \geq \frac{0.35}{T_{rise}} \quad (2)$$

The bandwidth of the RC gate network is given by [Equation 3](#)

$$BW = \frac{1}{2\pi \times R_{damp} \times C_{eff}} \quad (3)$$

Equating these two expressions gives the fundamental C_{iss} constraint:

$$C_{eff} \leq \frac{T_{rise}}{(2\pi \times R_{damp} \times 0.35)} \quad (4)$$

This inequality defines the maximum allowable total effective gate capacitance that the selected FET must satisfy to meet the rise-time specification.

3.1.2 Compliance Voltage Range

To verify that the FET stays in saturation, the designer must consult two key curves from the datasheet. First, the I_D versus V_{GS} transfer characteristic determines the maximum gate-to-source voltage (V_{GS} , maximum) required to drive the full output current. This value is the V_{GS} at which I_D equals the target output current. Second, the I_D versus V_{DS} output characteristics are examined at that specific V_{GS} maximum to identify the knee-point voltage, which is the minimum V_{DS} at which I_D saturates and becomes independent of V_{DS} . This knee-point voltage represents the minimum headroom the FET requires to stay in saturation.

The minimum compliance voltage of the application must exceed the knee-point V_{DS} identified above by a sufficient margin. If the minimum compliance voltage is too close to or below the knee-point, the FET enters the ohmic region under worst-case conditions, and a different device with a lower V_{th} or a sharper saturation knee must be selected.

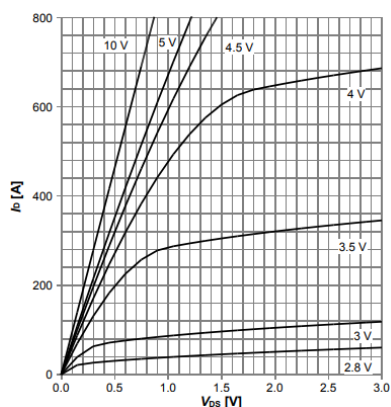


Figure 3-1. Typical Output Characteristics

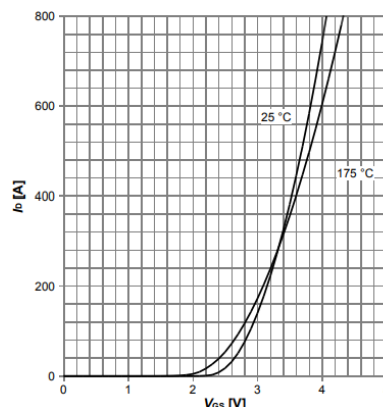


Figure 3-2. Typical Transfer Characteristics

As a worked example, the typical output and transfer characteristics of the FET, [IQE013N04LM6CGSC](#) are shown in [Figure 3-1](#) and [Figure 3-2](#). [Figure 3-1](#) shows the drain current variation with drain-to-source voltage for different gate-to-source voltages, where the drain current increases rapidly before entering the saturation region. [Figure 3-2](#) shows the transfer characteristics at 25°C and 175°C, indicating the variation of drain current with gate-to-source voltage and the effect of temperature on the device current. These characteristics are useful for determining the operating region and providing sufficient voltage margin during FET operation.

3.1.3 Safe Operating Area (SOA)

The safe operating area (SOA) curve is a critical checkpoint during FET selection because this curve defines the safe combinations of V_{DS} and I_D the device can handle without failure. For a V2I converter, the maximum output current specification directly determines where the operating point lands on the SOA plot. Importantly, the SOA curve provides maximum allowable on-time boundaries - for a given current level, the device can sustain higher power dissipation for shorter duration, but as the on-time increases, the allowable operating region shrinks due to thermal buildup in the die. Therefore, check the duty-cycle and pulse duration of the output current waveform against the appropriate pulsed SOA boundary. If the required on-time exceeds SOA permits at the target current, select a FET with a larger die area or better thermal characteristics.

Makes sure the opamp output swing range must comply with gate operating forward and reverse region.

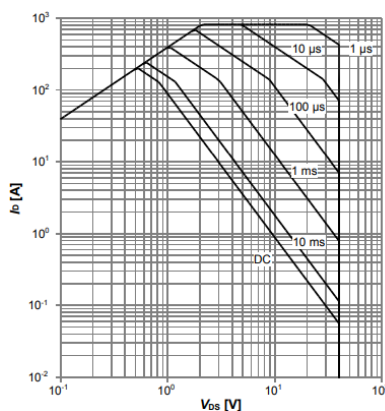


Figure 3-3. Safe Operating Area

3.2 R_{sense} Selection

The sense resistor (R_{sense}) plays a fundamental role in the V2I converter by converting the output current into a feedback voltage that the opamp can regulate against the input reference. However, choose the value of R_{sense} carefully to balance two competing concerns: sufficient voltage development for accurate sensing versus excessive power dissipation. For a high-current design, even a modest resistance can result in significant power loss. For example, at 50A, a 2mΩ resistor dissipates 5W, while a 0.1mΩ resistor dissipates only 0.25W. To keep

power dissipation at the sense resistor manageable, R_{sense} must be kept as low as possible, maintaining that the voltage drop across resistor R_{sense} remains small relative to the minimum compliance voltage while the power dissipation stays within acceptable limits. R_{sense} selection also depends on the acceptable output current error formed due to the opamp input offset voltage.

3.2.1 Effect of ESL

The parasitic ESL of the sense resistor forms an **L/R low-pass filter** with R_{sense} , since the feedback voltage V_{FB} is sensed directly across R_{sense} . During a current transient, the ESL opposes the rapid change in current, and the feedback voltage only settles to the true value after a time-constant of $\tau = \text{ESL} + L_{\text{Source}} / R_{\text{sense}}$, giving a rise-time of approximately:

$$T_{\text{rise}} = 2\tau = 2 \times \frac{(\text{ESL} + L_{\text{Source}})}{R_{\text{sense}}} \quad (5)$$

This creates a fundamental conflict, reducing R_{sense} minimizes power dissipation but directly increases the L/R time constant and slows down the feedback response, resulting in a rise-time beyond the required specification. Therefore, R_{sense} cannot be reduced arbitrarily, and the rise-time constraint sets a lower limit for R_{sense} .

3.3 Opamp Selection

3.3.1 Bandwidth

The opamp bandwidth is the first and most fundamental criterion in opamp selection because a slow opamp directly limits the rise time of the output current regardless of how well the rest of the circuit is optimized. Treating the system as a first-order approximation, the minimum required bandwidth of the opamp is given by [Equation 6](#).

$$\text{BW} = \frac{0.35}{T_{\text{rise}}} \quad (6)$$

where:

- T_{rise} is the target rise time specification

However, this value represents the minimum value at which the opamp alone is fast enough and leaves no margin for the additional bandwidth limiting introduced by the rest of the signal path.

In particular, the low-pass filter formed by R_{damp} and C_{gate} at the FET input already consumes a portion of the available bandwidth, meaning if the opamp is chosen at exactly the minimum BW, the cascaded system response falls short of the rise time target. To make sure the opamp does not become the bottleneck and that sufficient bandwidth remains after accounting for the $R_{\text{damp}} - C_{\text{gate}}$ pole, select an opamp with a bandwidth of 3× to 4× the calculated minimum, providing enough headroom for the overall closed-loop system to meet the rise time specification comfortably.

3.3.2 Slew Rate

When the V2I converter transitions from zero output current to the desired set point, the opamp must drive the FET gate from 0V to $V_{\text{GS(desired)}} - V_{\text{IN}}$ within the target rise-time T_{rise} . During this transition, the output must slew across the full gate-drive range in a single continuous transition, requiring maximum instantaneous rate of change. [Equation 7](#) calculates the required estimated slew rate.

$$\text{SR}_{\text{required}} = \frac{\Delta V_{\text{OUT}}}{T_{\text{rise}}} = \frac{V_{\text{GS(desired)}} - V_{\text{IN}}}{T_{\text{rise}}} \quad (7)$$

This is the only transition in normal operation where the opamp output must cover a large voltage swing in a short time. For all other current-level changes, transitioning from one set point to another requires only a small correction to V_{GS} , meaning the opamp output excursion remains small and the slew rate is not a limiting factor. Slew rate therefore becomes a critical constraint only during the zero-to-full-current transition.

$$SR_{\text{effective}} \approx \left(\frac{V_{ID}}{V_{\text{linear_range}}} \right) \times SR_{\text{max}}$$

Here V_{ID} represents the drain to source voltage. Since $V_{ID} \ll V_{\text{linear_range}}$ in a well-regulated loop, $SR_{\text{effective}}$ is a fraction of the datasheet SR_{max} . To make sure the opamp meets the rise-time requirement under this condition, select a device with a datasheet slew rate of $5 \times$ to $10 \times SR_{\text{required}}$, maintaining sufficient output rate-of-change even when the loop is operating in linear, small-signal region. To understand more about slew rate limitations for small signal, see [Ramping Up on Slew Rate](#)

3.3.3 Opamp Output Current

When the V2I converter transitions from zero output current to the desired set-point, the opamp must charge the FET gate capacitance from 0V up to V_{GS} (threshold). This is the only transition where a large amount of gate charge must be delivered in a short time. For all other current-level changes — stepping from one set-point to another — the change in gate charge ΔQ_G is very small, meaning the required gate current is also very small and opamp output current is not a limiting factor.

To determine the maximum opamp output current required gate charge at threshold, $Q_{G(\text{th})}$ is taken from the datasheet. This is the total charge, a opamp must deliver to bring the FET from fully off to the point where conduction begins, and represents the worst case charge demand on the opamp output.

The key timing constraint is that this charge $Q_{G(\text{th})}$ must be delivered within $0.25 \times T_{\text{rise}}$. The reasoning is straightforward, until $Q_{G(\text{th})}$ is fully transferred, the FET remains off and no output current flows. The design only tolerate the FET being off for a fraction of the target rise-time — any longer and the FET turn-on delay alone consumes a significant portion of T_{rise} , making the rise-time specification impossible. Budgeting $0.25 \times T_{\text{rise}}$ for this phase makes sure the remaining $0.75 \times T_{\text{rise}}$ available for the current to ramp to the final value. The required opamp output current is therefore:

$$I_{\text{OUT}(\text{min})} = \frac{Q_{G(\text{th})}}{(0.25 \times T_{\text{rise}})} \quad (8)$$

As with slew rate, this output current requirement is only critical during the zero-to-full transition. Once the FET is on and the loop is regulating, current-level changes require only incremental gate charge, and the opamp output current demand drops to a negligible level.

4 Design Based Component Selection

4.1 Design for $T_{\text{rise}} = 100\text{ns}$

4.1.1 FET Selection

Applying the same bandwidth-to-rise time relationship established earlier:

$$BW_{\text{required}} = \frac{0.35}{T_{\text{rise}}} = \frac{0.35}{100\text{ns}} = 3.5\text{MHz}$$

The $R_{\text{damp}}-C_{\text{eff}}$ low-pass filter pole must lie above this bandwidth:

$$f_{\text{pole}} = \frac{1}{2\pi \times R_{\text{damp}} \times C_{\text{eff}}} \geq 3.5\text{MHz}$$

solving for C_{eff} : $C_{\text{eff}} \leq 9.09\text{nF}$

So the FET's effective input capacitance must be below 9.09nF for this design.

1. Input capacitance, C_{iss}

We are supposed to look into the FETs with C_{iss} less than 9.1nF, and by also considering the g_m effect of capacitance variation we must chose FET's with C_{iss} less than 7.6nF.

From the C_{iss} criteria and our desired current specification we opted for [IQE013N04LM6CGSC](#) ($C_{\text{iss}} = 3.3\text{nF}$).

2. Compliance voltage

From the [IQE013N04LM6CGSC](#) datasheet the maximum current requirement drives $V_{GS(max)}$ to 3V. Mapping this requirement with the output characteristics of the FET shows that the FET operates in saturation for voltages above 0.5-0.6V. For our minimum compliance specification of 0.4V, the FET operates around the transition region from ohmic to saturation. Ramping up the compliance voltage to 0.7-0.8V keeps the FET in saturation.

3. SOA

This design targets 150A output current at a minimum compliance voltage of 0.5V, with a pulse duration of 100 μ s. Reading the SOA curve at $V_{DS} = 0.4V$ along the 100 μ s boundary, the [IQE013N04LM6CGSC](#) supports well over 100A operating point. The device operates entirely within the safe region with substantial margin, confirming SOA does not restrict the design.

4.1.2 R_{sense} Selection

For this design targeting 150A output current, the sense resistor value must be kept low to minimize power dissipation. However, the lower resistance produces a smaller sense voltage, which can affect sensing accuracy. Therefore, a 2m Ω resistor provides a balance between power dissipation and sense voltage, generating 300mV at 150A full scale, which is adequate for opamp regulation while keeping power dissipation within practical limits.

4.1.3 Opamp Selection

4.1.3.1 Bandwidth

The minimum required opamp bandwidth is set by the target rise-time:

$$BW_{min} = \frac{0.35}{T_{rise}} = \frac{0.35}{100ns} = 3.5MHz$$

Applying the 3 $\times$ to 4 $\times$ margin gives a recommended bandwidth of 5.95MHz – 7MHz. The OPA690 at 500MHz exceeds this amount by over 70 $\times$, making bandwidth a non-restrictive criterion for this design.

4.1.3.2 Slew Rate

The minimum slew rate required to swing the gate to $V_{GS(desired)}$ within the rise-time:

$$SR_{min} = \frac{V_{GS}}{T_{rise}} = \frac{3V}{100ns} = 30V/\mu s \quad (9)$$

Applying the 5 $\times$ to 10 $\times$ margin gives a recommended range from 150 to 300V/ μ s. The OPA690 provides 1,800V/ μ s, a 60 $\times$ margin over the minimum, well beyond the recommended range.

4.1.3.3 Output Current

$$I_{OUT(min)} = \frac{Q_{G(th)}}{0.25 \times T_{rise}} = \frac{5nC}{0.25 \times 100ns} = 200mA \quad (10)$$

The [OPA690](#) provides a maximum output current of 215mA. However given that the bandwidth and slew rate margins are extremely large, the opamp response is fast enough that the gate charging completes well within the 25% turn-on delay budget in practice. The OPA690 satisfies all three selection criteria for [Design for \$T_{rise} = 100ns\$](#) .

[OPA620](#) with low offset, slew rate of 190V/ μ s, 100MHz and peak current > 250mA is also a good fit.

Component Parameter	Derived Mathematical Requirement	Selected Component	Component Capability
Opamp BW requirement	Loop BW > 3.5MHz	OPA690 (opamp)	500MHz
BW limitation caused by C_{iss}	Max allowable $C_{iss} < 9090pF$	IQE013N04LM6CGSC	3300pF
Opamp output current	opamp > 200mA	OPA690 (opamp)	215mA
Slew rate limitation	Slew rate > 33V/ μ s	OPA690 (opamp)	1800V/ μ s

4.2 Architecture Selection (Quick Reference)

CFA's provide high-speed, and fast slew rates necessary for high-frequency and pulse-based signal chains. However, VFA's offer the precision, accuracy, and low noise required for DC and lower-frequency designs, making them the preferred choice for managing offset, drift, and CMRR and predictable frequency response. For a 100ns rise-time, the VFA design stands as an excellent choice.

Table 4-1. Amplifier Architecture Comparison

Parameter	Voltage Feedback Amplifier (VFA)	Current Feedback Amplifier (CFA)
1. Input Impedance	Symmetrical. Both input pins act like high resistance.	Asymmetrical. The non-inverting pin is high resistance, but the inverting pin is ultra-low resistance $Z_{in+} \approx \text{High}, Z_{in-} \approx 10 \text{ to } 50\Omega$
2. Bandwidth vs. Gain	Trade-off. Bandwidth is inversely proportional to the closed-loop gain (A_V) via the Gain-bandwidth Product limit. $BW = \frac{GBWP}{A_V}$	Independent. Bandwidth is dictated by the physical feedback resistor (R_F) and internal capacitance (C_C), ignoring gain. $BW \approx \frac{1}{2\pi \times R_F \times C_C}$
3. Slew Rate	Hard Speed Limit. Slew rate is capped by a fixed internal tail current I_{tail} charging the internal capacitor (C_C). $SR_{max} = \frac{I_{tail}}{C_C}$	Power on Demand. Generates internal error current (I_{error}) proportional to the input step size (V_{step}), driving massive dynamic slew rates. $SR = \frac{I_{error}}{C_C} \approx \frac{V_{step}}{R_F \times C_C}$
4. DC Offset	Highly Precise. Symmetrical input stages provide an excellent choice for matched bias currents (I_B) and ultra-low input offset voltages (V_{OS}).	Less Precise. The asymmetrical input stage inherently suffers from mismatched bias currents, creating a larger overall DC offset error.
5. Feedback Capacitor (C_F)	Standard Practice. Placing a capacitor directly across the feedback loop is the standard way to limit bandwidth or create a low-pass filter. $f_{-3dB} = \frac{1}{2\pi \times R_F \times C_F}$	Strictly Forbidden. Because the inverting pin is low impedance, an AC short circuit ($X_C \rightarrow 0$ at high frequencies) destroys loop stability and instantly causes violent oscillation.

5 Circuit Architecture Selection

5.1 Single Feedback Method

For small R_{damp} :

- Less phase lag in feedback loop
- Higher loop bandwidth
- Faster transient response

For $R_{damp} = 0$

- Ringing due to high Q factor of the resulting LC network
- Circuit can become unstable regardless of loop design

Equation 11 calculates the effective limits for R_{damp} .

$$2 \times \sqrt{\frac{C_{eff}}{L_{gate}}} < R_{damp} < \frac{1}{2\pi \times BW \times C_{eff}} \quad (11)$$

In this calculation, L_{gate} represents the parasitic inductance in the gate-drive path. Selecting R_{damp} as 5Ω is a good enough to measure as there is no under damping and oscillations in the gate path and all the calculations

of C_{eff} are done with respect to $R_{damp} = 5\Omega$. For this design choosing R_{damp} as 5Ω is a good measure. Based on validation and simulation, R_{sense} can be tuned further.

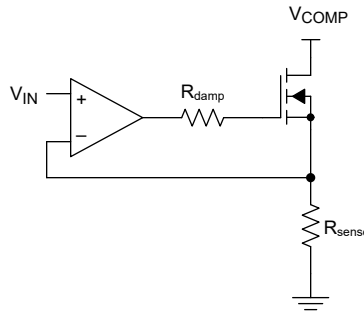


Figure 5-1. VCCS With Damp Resistor

5.2 Dual Feedback Method

As detailed in the [Operational Amplifier Stability Theory and Compensation Methods](#), maintaining loop integrity in dual feedback architectures requires precise management of the FB1 and FB2 feedback paths.

- FB1 → Feedback through R_{damp} (dominates at low-frequency, C_F is open)
- FB2 → Feedback through C_F (dominates at high-frequency, C_F is short)

The [Figure 5-2](#) shows dual feedback circuit with R_{damp} and R_F . To maintain stability, the design must satisfy the condition $R_F \gg R_{damp}$, make sure the feedback resistance is significantly larger than damp resistance. This relationship is governed by the following mathematical criteria, see also [Operational Amplifier Stability Theory and Compensation Methods](#)

$$F_{fb1} = \frac{1}{2\pi \times R_{damp} \times C_{eff}} \quad (12)$$

$$F_{fb2} = \frac{1}{2\pi \times R_F \times C_F} \quad (13)$$

$$f_{CFB1} > f_{CFB2} \quad (14)$$

$$\frac{1}{2\pi \times R_{damp} \times C_{eff}} > \frac{1}{2\pi \times R_F \times C_F} \quad (15)$$

$$C_F > \frac{(R_{damp} \times C_{eff})}{R_F} \quad (16)$$

Effective implementation relies on careful component selection to balance these feedback impedance against the necessary damping requirements.

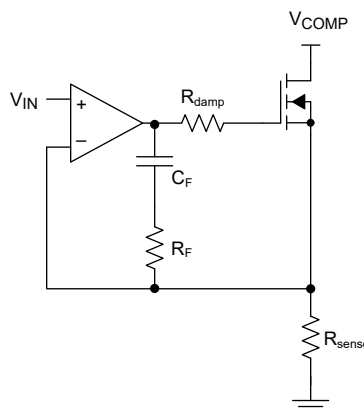


Figure 5-2. VCCS With Dual Feedback

5.3 Enhanced Dual Feedback Method

R_{FX} is an additional resistor added in series with C_F in the dual-feedback path as shown in Figure 5-3. The main purpose of R_{FX} is to increase the high-frequency noise gain. This configuration allows the system to remain stable with a smaller C_F , while also providing faster feedback response and quicker settling for input and load transients. The trade-off is increased output noise at high frequencies.

R_{FX} also provides an optional enhancement to the dual-feedback circuit. Setting R_{FX} to 0Ω reverts the circuit to the standard R_{damp} dual-feedback topology, which provides good stability. R_F cannot be zero in the R_{damp} dual-feedback topology because R_{FX} serves as the fundamental DC feedback resistor that senses the output voltage at low frequencies. Without R_{FX} the circuit loses the DC feedback path completely, and the opamp output becomes uncontrolled. Therefore, R_F serves as a performance optimization rather than a necessity.

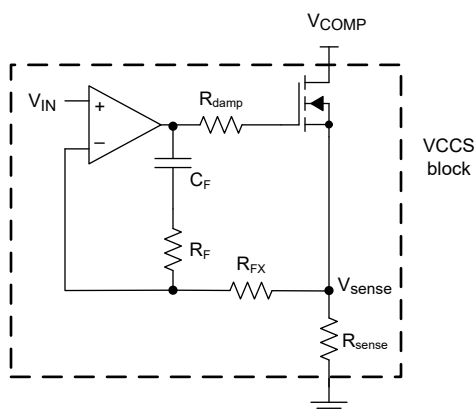


Figure 5-3. VCCS with Enhanced Dual Feedback

6 Results

The VCCS design is validated through simulation and hardware testing to validate compliance with the target specifications. Figure 6-1 demonstrates the transient response for a 100ns input ramp, resulting in a 50A pulsed output current. With an R_{sense} of $2m\Omega$, the steady-state voltage across the sense resistor settles accurately at 100mV.

The high-speed performance is further detailed in Figure 6-2, which provides a zoomed-in view of the rise time. The waveform exhibits minimal overshoot and rapid settling, confirming the effectiveness of the damping resistor R_{damp} and the dual-feedback architecture in suppressing parasitic oscillations. Additionally, the circuit's high-frequency capability is verified in Figure 6-3, which shows the output current tracking a continuous 20MHz sine-wave input, demonstrating the low-distortion performance of the high-bandwidth op amp in a dynamic load environment.

Results



Figure 6-1. Transient Output Current Response $T_{rise} = 100ns$ and $I_{OUT} = 50A$



Figure 6-2. Detailed View of Transient Rise Time and Settling Behavior

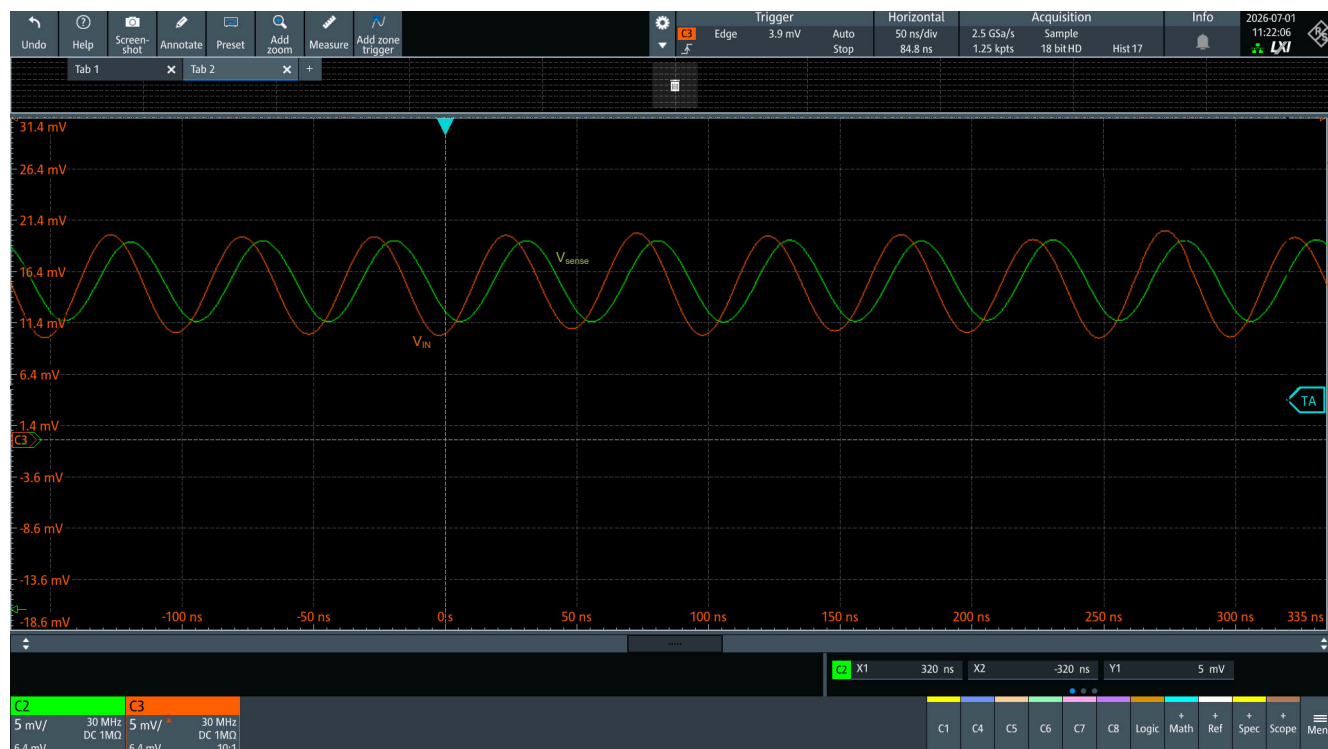


Figure 6-3. High-Frequency Output Current Response (20MHz Sine Wave)

To achieve output currents exceeding 50A while maintaining a fast rise time $T_{\text{rise}} = 100\text{ns}$ and a 0.5V compliance voltage, multiple VCCS blocks as shown in [Figure 5-3](#) can be connected in parallel. For applications requiring higher currents with relaxed transient requirements $T_{\text{rise}} > 100\text{ns}$ or higher compliance voltages, current levels above 50A can be achieved using a single VCCS block by increasing the V_{IN} voltage.

7 Related Documentation

- Texas Instruments, [OPA690 Wideband, Voltage-Feedback Operational Amplifier With Disable](#) datasheet.
- Texas Instruments, [OPAx620 250MHz, Precision, Rail-to-Rail I/O, CMOS Operational Amplifier](#) datasheet.
- Texas Instruments, [Operational Amplifier Stability Theory and Compensation Methods](#) technical white paper.
- Texas Instruments, [Ramping Up on Slew Rate](#) application note.

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