

Technical White Paper

Ethernet PHY Selection Guide for Radar Applications



Abstract

Automotive radar systems are evolving toward higher sensor density and tighter sensor fusion, requiring Ethernet networking that scales to support long-range ADAS radar to compact near-field radar. The required Ethernet data rate depends on where the signal processing occurs—from a few Mbps for edge-processed object lists to several Gbps for raw-data streaming to central compute. This white paper guides selection across TI's automotive Ethernet PHY portfolio (10BASE-T1S, 100BASE-T1, 1000BASE-T1), covering key features—TC10 low-power sleep, IEEE 802.1AS time synchronization, and IEEE 802.1AE MACsec security—offered in footprint-compatible packages. The document also maps TI PHYs to specific AWR and AWRL radar SoCs, helping designers pair PHYs based on interface, data rate, and feature requirements.

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1 Introduction

New-generation automotive architectures often consist of using five or more external radars for 360-degree coverage and specialized in-cabin radar for driver monitoring and occupancy detection. These two use cases have two distinct technological paths: high-performance ADAS radar and near-field or in-cabin radar.

Table 1-1. Two Distinct Use Cases

High-Performance ADAS Radar	Near-Field/In-Cabin Radar
<ul style="list-style-type: none"> Designed for long-range detection and high-resolution imaging Supports tighter radar-camera-LiDAR fusion algorithms Requires high object discrimination and high data throughput to stream data to a central computer 	<ul style="list-style-type: none"> Driven by evolving safety standards such as Euro NCAP Sensors focus on short-range applications like occupancy monitoring, intrusion detection, and parking assistance The priority for these sensors is high classification accuracy, low-power consumption, and cost-effective compact integration

Texas Instruments offers a family of Ethernet PHYs designed to meet the diverse requirements for both external and in-cabin radar. This whitepaper describes the key PHY-level features that influence radar system designs, maps the features to the TI PHY portfolio, and provides a selection guide for pairing TI PHYs with automotive radar SoCs.

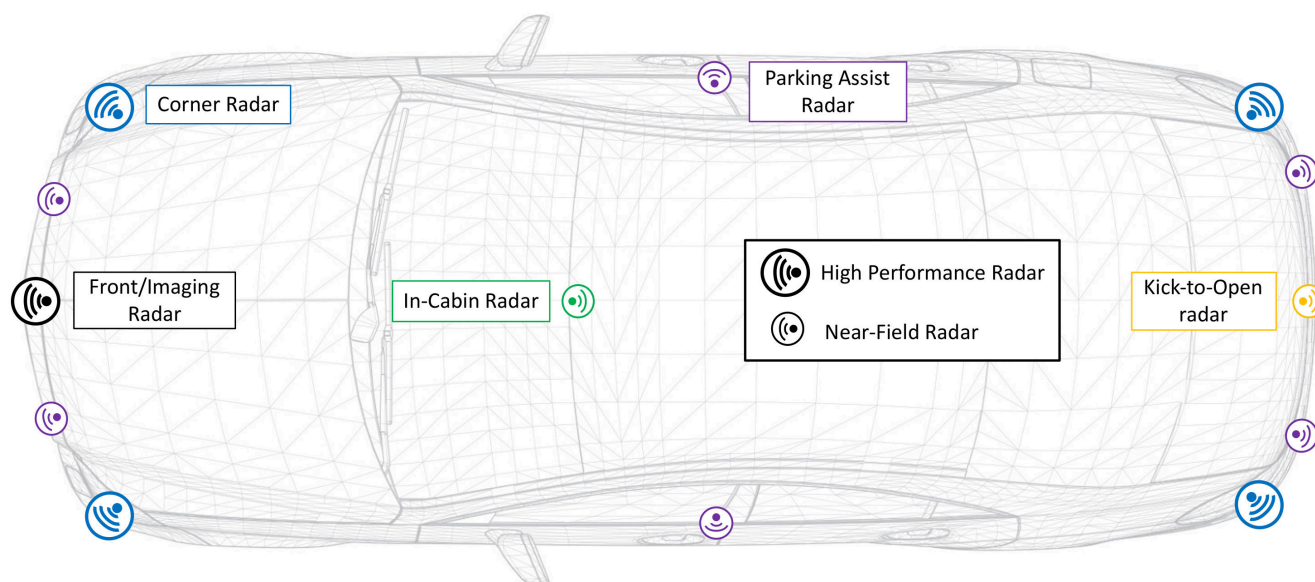


Figure 1-1. Common Automotive Radar Architecture

2 PHY Data Rate Selection and Radar Processing

Radar data processing is generally split into the signal processing and detection stage. The point at which each stage performs determines the Ethernet bandwidth the system requires.

The signal processing stage consists of performing various FFTs on the raw radar data to recover a list of objects with range, velocity, and angle (imaging radars can also have an additional elevation measurement). Each of these FFT steps result in a reduction of the sensor data sent back to ADAS compute. For example, after the range FFT, bins that do not contain targets can be discarded, reducing the amount of data that must be processed further.

The detection stage compresses the stream further by generating a concise object list (ID, range, velocity, angle, and so forth), which transmits to the central compute.

If all processing is performed on the radar SoC (edge), only the compact object list leaves the sensor, and the required link speed is on the order of a few Mbps. When processing is split, the edge can stop after the early FFTs and stream the intermediate data to a central ADAS ECU; in this case, the link must support tens to

hundreds of Mbps. Finally, if the central computer is responsible for all processing, the radar must transmit raw samples streamed at several Gbps.

Implications for PHY choice:

- **10BASE-T1s (10Mbps)** – Radar SoC performs all radar processing on the edge.
 - Use [DP83TD555](#) or [DP83TD535](#)
- **100BASE-T1 (100Mbps)** – Radar SoC performs some edge processing; intermediate spectrum data is sent to central compute for additional processing and higher-level fusion.
 - Use [DP83TC815](#) or [DP83TC817](#)
- **1000BASE-T1 (1Gbps)** – Radar SoC performs only early-stage processing. The bulk of the data streams to the central compute for further FFTs, detection, and sensor-fusion algorithms.
 - Use [DP83TG721](#)

TI Ethernet PHYs are available in all three speed classes. System designers can select the PHY to match the selected split-processing architecture.

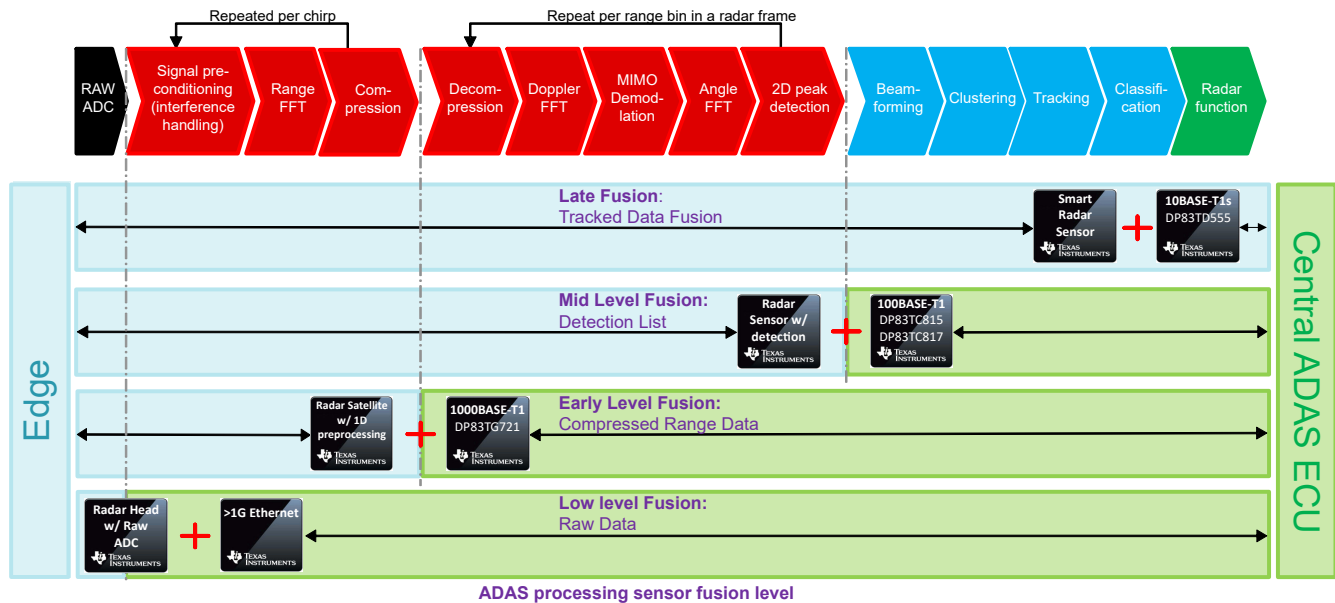


Figure 2-1. Distribution of Processing Edge and ADAS Compute

3 Additional PHY Level Features

3.1 Low-Power Sleep (TC10)

TC10 is an Open Alliance defined standard for sleeping and waking automotive Ethernet networks. TI PHYs that support TC10 can enter a low-power sleep state, significantly reducing PHY current draw while remaining able to respond to system wake commands. The PHY can also be connected to control the power rails of the radar module, enabling it to manage the sleep and wake states of the entire radar module. More information can be found in [System Implementation of Open Alliance TC10 Sleep/Wake-up](#).

3.2 Time Sensitive Networking (IEEE 802.1AS)

TSN allows for the synchronization of multiple PHYs in a vehicle network to the same wall clock. Events, like a radar chip, can trigger on all radar modules synchronously. The PHY has mechanisms to present the wall clock to the radar SoC, aligning the timing of the SoC to the network.

Additionally, TI's 100M PHYs with TSN support have a fixed latency feature to compensate for the larger latency variation caused by the lower clock speeds at 100M.

3.3 MACsec (IEEE 802.1AE)

MACsec is a PHY-level security standard that encrypts and authenticates each Ethernet frame. Only trusted devices with the correct MACsec keys can read traffic, preventing tampering and eavesdropping. The radar SoC must also implement the MACsec key agreement (MKA) service for authentication and key management.

For more details, see [TSN and MACsec in Automotive Radar Applications](#).

4 TI Ethernet PHY Family and Selection

TI's single-pair automotive Ethernet PHYs are available in a range of feature tiers, as described in [Section 3](#), from basic PHYs to those supporting MACsec. These feature sets are cumulative—so a PHY with MACsec support also includes 802.1AS and TC10. System designers can select the TI PHY that supports the required subset of features, potentially without incurring additional cost or complexity. Additionally, all 100BASE-T1 and 1000BASE-T1 PHYs are footprint compatible with a common schematic. This *drop-in* compatibility helps future-proof radar modules for evolving vehicle-network requirements.

TI PHY	Basic	+ TC10	+ 802.1AS	+ MACsec
1000BASE-T1	DP83TG720	N/A	DP83TG721	N/A
100BASE-T1	DP83TC814	DP83TC812 DP83TC813 (Small form factor)	DP83TC815	DP83TC817
10-BASE-T1S	N/A	DP83TD535 DP83TD530	DP83TD555 (SPI)	N/A

For the most up-to-date Ethernet PHY portfolio, visit the [TI Ethernet PHY product page](#).

4.1 10BASE-T1S Multidrop Ethernet PHYs

TI's 10Mbps Ethernet PHYs implement the IEEE 802.3cg multidrop bus. A minimum of eight nodes can share a single twisted pair cable with 10Mbps bandwidth. 10BASE-T1S has support for PLCA (physical layer collision avoidance), allowing for bounded latency and equal access across the nodes.

For automotive radar, 10BASE-T1S is advantageous because low-speed peripheral radars can all be connected on one 10BASE-T1S bus instead of using separate point-to-point links and multiple switch ports, simplifying wiring and potentially reducing BOM cost.

TI offers three 10BASE-T1S parts that cover the typical radar SoC interfaces:

- **DP83TD530** and **DP83TD535** exposes an OA3p interface and relies on the radar SoC to provide the Ethernet MAC and PLCA logic
- **DP83TD555** integrates MAC and PHY with a SPI bus for radars with SPI to seamlessly connect to 10BASE-T1S network.

All three devices can be mixed on the same 10BASE-T1S bus. This flexibility allows designers to select the preferred part based on the existing interface of the radar, and still benefit from the multidrop topology, TC-10 low-power sleep, and optional TSN time synchronization that the 10BASE-T1S family provides.

4.2 TI Ethernet PHY Pairing With TI AWR High-Performance Radar SoCs

TI's high-performance automotive radar SoCs expose three main communication interfaces:

- **CSI-2**: High-speed serial interface for raw sensor data.
- **Ethernet MAC**: The MAC side of the standard IEEE 802.3 Ethernet link (TI radar SoCs support MII, RMII or RGMII configurations).
- **CAN-FD**: Flexible data rate CAN interface for control and diagnostics.

Since the MAC conforms to IEEE 802.3, any TI Ethernet PHY can be used with the radar SoC if the data-rate class of the PHY matches the rate supported by the SoC (100BASE-T1 or 1000BASE-T1). When selecting a PHY, the system designer must verify that the select part supports the same speed tier that the radar SoC requires. The listed radar SoC Ethernet speeds are maximum capabilities. For example, the AWR2x44P can be configured for 100M or 10M Ethernet if more edge processing is used on the radar SoC.

Table 4-1. Ethernet Interface Options Available on the AWR Radar SoC Family

Device	PHY
AWR2188	CSI-2 (primary) With edge processing MCU: DP83TG721 DP83TC815 DP83TC817
AWR2x44P	DP83TG721
AWR2544	DP83TG721
AWR2x44-ECO	DP83TC815 DP83TC817

4.3 TI Ethernet PHY Pairing With TI AWRL In-Cabin, Near Field Radar SoCs

TI's near-field and in-cabin automotive radar SoCs mainly expose SPI and CAN-FD data interfaces because the on-SoC processing and classification reduce the output data rate. For these devices, the preferred Ethernet PHY pairing is the DP83TD555, which integrates a full MAC and SPI, eliminating the need for an external MAC controller and providing a compact design that fits the low throughput requirements of the AWRL radars.

Table 4-2. Interface Options Available on the AWRL Radar SoC Family

Device	Communication Interface
AWRL6888	DP83TD555
AWRL6844	
AWRL6432	
AWRL1432	
AWR1843AOP	
AWR2944LC	DP83TC815 DP83TC817

5 Conclusion

Ethernet links must meet the demands of delivering 10Mbps, 100Mbps, or 1Gbps with deterministic latency, time synchronization, and robust security due to shifts to five plus radars per vehicle, tighter sensor-fusion algorithms, and the increased use of near-field radar. TI's automotive PHY portfolio provides these speed classes, multidrop capability, and optional TC-10 low-power, TSN, and MACsec features in interchangeable, footprint-compatible packages.

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Last updated 10/2025