Errata

CC274xx-Q1 SimpleLink™ Wireless MCU Device Revision E and F

ABSTRACT

This document describes the known exceptions to functional specifications (advisories) of the CC274xx-Q1 SimpleLink™ device.

This document supports the following devices:

- CC2745R74E0WRHARQ1
- CC2745R10E0WRHARQ1
- CC2745R10E1WRHARQ1
- CC2745P10E0WRHARQ1
- CC2744R74E0WRHARQ1

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Trademarks

1 Advisories Matrix

Table 1-1 lists all advisories, modules affected, and the applicable silicon revisions.

Table 1-1. Advisories Matrix

MODULE	DESCRIPTION	SILICON REVISIONS AFFECTED	
		E	F
ADC	Advisory ADC_08—ADC BUSY bit not cleared in repeat single, sequence, and repeat sequence conversion modes	Yes	Yes
ADC	Advisory ADC_09—ADC can have random conversion errors.	Yes	Yes
BATMON	Advisory BATMON_01—Incorrect temperature measurement	Yes	Yes
BATMON	Advisory BATMON_02—Spurious temperature update interrupts from BATMON in standby	Yes	Yes
SYS	Advisory SYS_204—SysTimer may not always generate a compare event when previously programmed with a value	Yes	Yes
SYS	Advisory SYS_206—The RF phase jumps during HFXT amplitude compensation and HFXT amplitude control	Yes	Yes
SYS	Advisory SYS_207—Standby entry may not be gated if FLTSETTLED bit is read too soon	Yes	Yes
SYS	Advisory SYS_211—Some concurrent high bandwidth operations require resource coordination framework	Yes	Yes
APU	Advisory APU_201—APU Data memory write operation fails	Yes	Yes
HSM	Advisory HSM_01—Updated retry mechanism for RNG health check initialization	Yes	Yes
UDMA	Advisory UDMA_01—µDMA write response to a peripheral's single request can be missed	Yes	Yes
RADIO	Advisory RADIO_05—Radio write operation fails	Yes	Yes
SYSROM	Advisory SYSROM_01—Power Loss Vulnerability in System ROM Firmware Update Process	Yes	No

2 Nomenclature, Package Symbolization, and Revision Identification

2.1 Device and Development Support—Tool Nomenclature

To designate the stages in the product development cycle, Texas Instruments™ assigns prefixes to the part numbers of all devices and support tools. Devices are assigned one of two prefixes: X or P, to indicate non-production versions of the silicon die (for example, XCC2745P10-Q1). Fully qualified production versions carry no prefix. Texas Instruments recommends two possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (X/TMDX) through fully qualified production devices/tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

no prefix Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Prototype devices (marked with X or P) have a greater failure rate than fully qualified production devices. Texas Instruments advises against their use in production systems, as their long-term reliability has not been fully characterized. Only fully qualified production devices should be used in end products.

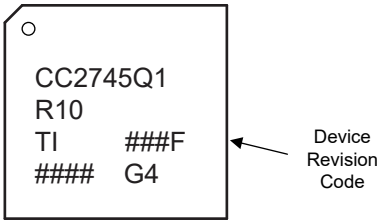
2.2 Devices Supported

This document supports the following devices:

- CC2745R74E0WRHARQ1
- CC2745R10E0WRHARQ1
- CC2745R10E1WRHARQ1
- CC2745P10E0WRHARQ1
- CC2744R74E0WRHARQ1

2.3 Package Symbolization and Revision Identification

Package Symbolization and Table 2-1 describe package symbolization and the device revision code.



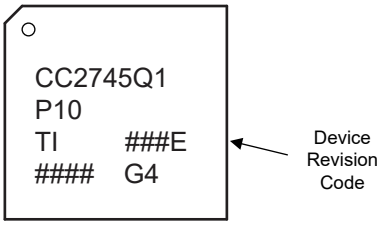


Figure 2-1. Package Symbolization

Table 2-1. Revision Identification

Device Revision Code	Silicon Revision
E	PG2.0
F	PG2.1

3 Advisories

ADC_08 *ADC BUSY bit not cleared in repeat single, sequence, and repeat sequence conversion modes*

Revisions Affected

C

Description

When the ADC is configured in repeat single, sequence, or repeat sequence conversion modes with trigger policy as trigger next in the MEMCTLx register, software attempting to stop the conversion sequence by clearing the ENC bit does not clear the BUSY bit in the STATUS register. In the case of sequence conversion mode with trigger next policy, the BUSY bit is cleared at the end of the conversion sequence.

Workaround

To stop the conversions and to clear the BUSY bit in the above-mentioned ADC operating scenario, the following software sequence can be followed.

1. Write CTL0.ENC = 0
2. Change CTL1.TRIGSRC to SOFTWARE
3. Write CTL1.SC=1

ADC_09 *ADC can have random conversion errors*

Revisions Affected

C

Description

ADC can have errors at a rate as high as 1 in 400 million ADC conversions. When a conversion error occurs, the error results in a jump in the digital output of the ADC without a corresponding change in the ADC input voltage, otherwise known as a ‘sparkle code’. The magnitude of the jump is 64 LSBs higher or lower than the expected ADC output when the ADC is used in 12-bit resolution setting. The magnitude of the jump decreases to ±16 LSBs for 10-bit resolution and ±4 LSBs when set to 8-bit resolution.

Workaround

The error rate can be reduced to 1 error in 100 billion ADC conversions by setting ADC.DEBUG1:CTRL[10:9] bits high.

Other software workarounds, like a best-out-of-three, where out of three consecutive samples the one with the highest standard deviation is discarded and the other two averaged to generate the ADC output, can also be considered.

ADC_09 (continued) ***ADC can have random conversion errors***

Software averaging of 16 consecutive ADC outputs decreases the deviation of the ADC output to ±4 LSBs when set to 12-bit resolution.

These workarounds would be incorporated into future releases of SimpleLink™ Low Power F3 software development kit (SDK).

BATMON_01 *Incorrect temperature measurement*

Revisions Affected

C

Description

BATMON can report incorrect temperatures when hysteresis is enabled. To prevent potential incorrect temperature reports, the user must always disable BATMON hysteresis.

Workaround

Hysteresis is controlled by the PMUD.CLT[2] HYST_EN bit.

Hysteresis is enabled by default (reset value = 1) and, therefore, must actively be disabled during boot.

Hysteresis can be disabled by clearing the PMUD.CLT[2] HYST_EN bit using the following command:

HWREG(PMUD_BASE + PMUD_O_CTL) = (PMUD_CTL_CALC_EN | PMUD_CTL_MEAS_EN)

This workaround is incorporated into the SimpleLink™ Low Power F3 software development kit (SDK) version 8.10 and newer.

BATMON_02 *Spurious temperature update interrupts from BATMON in standby*

Revisions Affected

C

Description

BATMON can issue spurious temperature update interrupts when PMUD.EVENT.TEMP_UPDATE is used as a wake-up source from standby.

Workaround

Instead of using PMUD.EVENT.TEMP_UPDATE as the wake-up source, PMUD.EVENT.TEMP_OVER_UL (current temperature over a set upper limit) or PMUD.EVENT.TEMP_BELOW_LL (current temperature below a set lower limit) shall be considered.

When using PMUD.EVENT.TEMP_OVER_UL or PMUD.EVENT.TEMP_BELOW_LL as wake-up interrupts, these are the other settings that have to be enabled:

- Select GLDO as the source for VDDR regulation by setting PMCTL.VDDRCTL.SELECT to 0x0.

Note

This causes a slight increase in standby power consumption. Please check the ‘Power Consumption – Power Modes’ section of the data sheet for exact details.

- Set SYS0.TMUTE4.RECHCOMPREFLVL to 0x2
- Set SYS0.TMUTE5.GLDOISSET to 0x1E

This workaround would be incorporated into future releases of SimpleLink™ Low Power F3 software development kit (SDK).

SYS_204	***SysTimer may not always generate a compare event when previously programmed with a value.***
Revisions Affected	E and F
Description	SysTimer does not always generate a compare event during the initialization/sync up phase, when SysTimer has previously been programmed with a value.
Workaround	Wait to program SysTimer until SYSTIM.STATUS.SYNCUP is cleared. This workaround is incorporated into the SimpleLink™ Low Power F3 software development kit (SDK) version 8.10 and newer.

SYS_206	***The RF phase jumps during HFXT amplitude compensation and HFXT amplitude control.***
Revisions Affected	E and F
Description	The RF phase jumps during HFXT amplitude compensation and HFXT amplitude control. This issue only applies after start-up of the device is complete, and then later programmatically adjusting the cap array values while using HFXT. If the cap array values are set during startup, this issue is not seen.
Workaround	The setting or modification of cap array steps should only be done during start-up and before any RF operations. Do not modify the cap array steps dynamically during run-time after that point. The Q1 and Q2 cap array steps can be modified in SysConfig.

SYS_207 *Standby entry may not be gated if FLTSETTLED bit is read too soon.*

Revisions Affected

E and F

Description

Standby entry may not be gated if attempted before LFINC filter settles and is read too soon. This issue is not seen when using LFXT.

Workaround

In order to workaround this, when using LFOSC:

1. Clear both the interrupts.
2. Check for CKMD.RIS.HFXTGOOD.
3. Check for CKMD.RIS.LFTICK.
4. Check for FLTSETTLED.

Standby entry should be triggered only when the LFINC filter has settled which can be confirmed by reading the memory masked register (MMR) CKMD.LFCLKSTAT.FLTSETTLED bit.

Alternatively, LFXT can be used and this can be avoided. This workaround is incorporated into the SimpleLink™ Low Power F3 software development kit (SDK) version 8.40 and newer.

SYS_211	***Some concurrent high bandwidth operations require resource coordination framework.***
Revisions Affected	E and F
Details	*Concurrent high bandwidth operations involving CAN, APU peripherals, and multiple bus initiators (DMA, I2S or HSM) require resource coordination framework.*
Workaround	Use DMA as the only bus initiator for CAN registers and APU memory accesses. This workaround is incorporated into the SimpleLink™ Low Power F3 software development kit (SDK) version 9.14 and newer. Users are recommended to update to the HSM firmware included in the 9.14 SDK. Additionally, users are recommended to read the "Upgrade and Compatibility Information" section of the SDK release notes to understand API implications of this change.

APU_201	*APU Data memory write operation fails.*
Revisions Affected	E and F
Description	APU Data memory write operation fails if two write operations occur back-to-back.
Workaround	Customers must always use the TI APU driver to access APU data memory. This workaround is incorporated into the SimpleLink™ Low Power F3 software development kit (SDK) version 8.40 and newer.

HSM_01 *Updated retry mechanism for RNG health check initialization*

Revisions Affected

E and F

Details

On CC27XX devices using CRNG, a firmware limitation could cause the device to halt during RNG configuration or HUK token provisioning when CRNG encountered a transient low-entropy condition. CRNG entropy is influenced by system activity and may temporarily require additional time to accumulate. Since previous versions of the SimpleLink Low Power F3 SDK's HSM firmware support were initially built without accounting for this, it would halt on the first health check failure rather than waiting for entropy to stabilize.

Workaround

HSM firmware version 3.4.5 and higher provides a firmware-oriented approach to reviving device entropy generation levels when encountering transient low-entropy conditions. This is achieved with a retry mechanism targeting the initial seed of the DRBG engine.

This workaround is incorporated into the SimpleLink™ Low Power F3 software development kit (SDK) 9.14.04, 9.20.01, and newer. This HSM firmware is backwards compatible with older versions of the SDK.

UDMA_01 *µDMA write response to a peripheral's single request can be missed.*

Revisions Affected

E and F

Details

µDMA responds to single and burst requests from peripherals. In case the write access(es) from µDMA is(are) intercepted by the interconnect write buffers due to arbitration loss, the peripheral can raise a second spurious single or burst request. Since the µDMA responds to the second request after the peripheral's FIFO gets full with earlier write buffer contents, the second write(s) is(are) ignored by the peripheral and get(s) missed. This issue is seen only during data transfers via µDMA TX channels. This issue is not seen on the µDMA RX channels, since the read path through the interconnect does not include write buffers.

Workaround

µDMA SETBURST is configured to use BURST requests.

µDMA arbitration size is 2.

TX FIFO level trigger is set to ≤ 1/4 empty.

This workaround is to be incorporated into future releases of SimpleLink™ Low Power F3 software development kit (SDK).

RADIO_05 *Radio write operation fails*

Revisions Affected

E and F

Details

Radio write operation fails if two write operations occur back-to-back.

Workaround

The RCL (Radio Control Layer) must always be used to interface with the radio.

This workaround is incorporated into the SimpleLink™ Low Power F3 software development kit (SDK) version 8.40 and newer.

SYSROM_01	*Power Loss Vulnerability in System ROM Firmware Update Process*
Revisions Affected	E
Details	The firmware update process, including HSM, Secondary Bootloader, and application updates, executed by the System ROM may be unexpectedly interrupted if a power loss occurs during operation. Since the ROMAPI register is not retained across power cycles, the System ROM is unable to resume and complete the firmware update process.
Workaround	None. The permanent fix is to use Silicon Revision PG2.1 (Rev F).

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 31, 2025 to August 30, 2026 (from Revision B (December 2025) to Revision C (August 2026)) **Page**

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