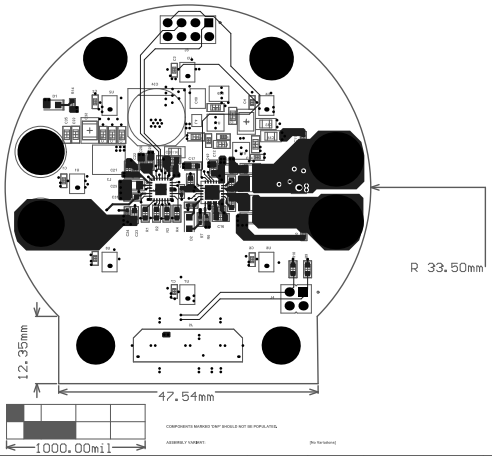
221 Board sized to silkscreened box after final mask. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

JUSTIFICATION: BE TOP CLOCKWISE "PIN1" SCREAM ENTERPRISES

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = L1_TOP

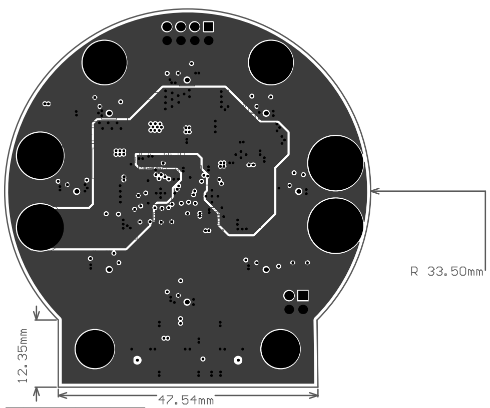
BOARD #: Robotics Design REV: A SVN REV: Not in version control

DID #: TIDA-060054

GENERATED : 5/20/2026 10:15:04 AM

TEXAS INSTRUMENTS

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED , PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc
ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

ALL ARTWORK VIEWED FROM TOP SIDE
BOARD #: Robotics Design
REV: A
SVN REV: Not in version control
LAYER NAME = [illegible]
TID #: TIDA-060054
PLOT NAME = L2-GND1
GENERATED : 5/20/2026 10:18:06 AM
TEXAS INSTRUMENTS

221 ■ Board sized to silkscreened size after final route. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

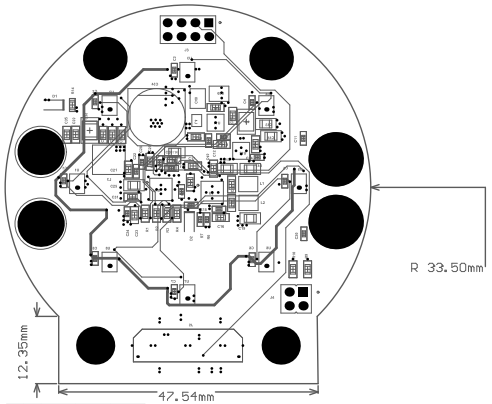
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = L3_Signal

BOARD #: Robotics_Design REV: A SVN REV: Not in version control

STD #: TIDA-060054

GENERATED : 5/20/2026 10:15:07 AM TEXAS INSTRUMENTS

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

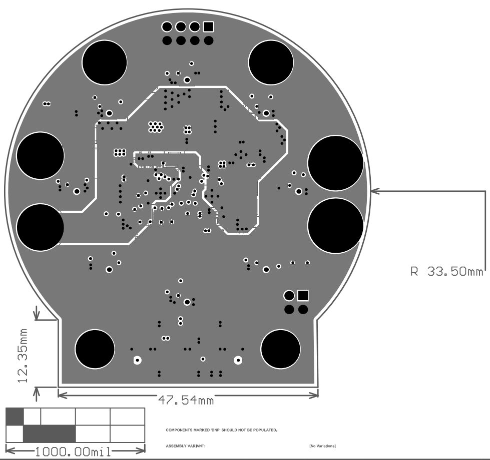
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER [X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE [ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc
ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE		BOARD #: Robotics Design	REV: A	SVN REV: Not in version control	
LAYER NAME =		TID #: TIDA-060054			
PLOT NAME = L4_GND2		GENERATED : 5/20/2026 10:18:09 AM		TEXAS INSTRUMENTS	

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

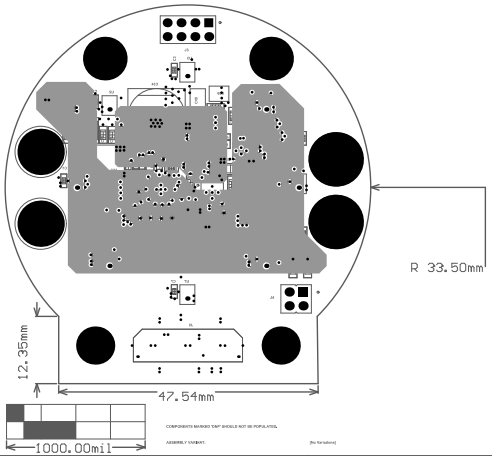
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = L6_PWR
BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 5/20/2026 10:18:10 AM TEXAS INSTRUMENTS

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

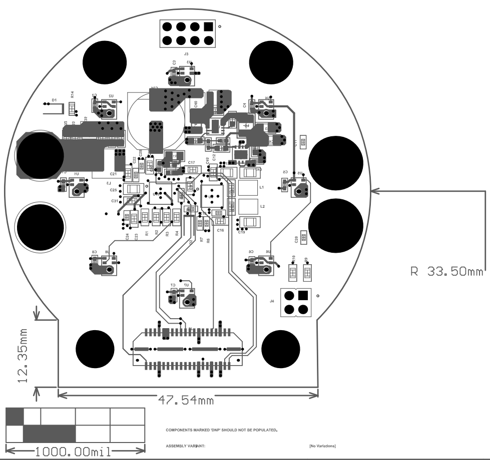
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER [X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE [ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE		BOARD #: Robotics Design	REV: A	SVN REV: Not in version control	
LAYER NAME = [illegible]		TID #: TIDA-060054			
PLOT NAME = L6_Bottom		GENERATED : 5/20/2026	10:18:12 AM	TEXAS INSTRUMENTS	

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

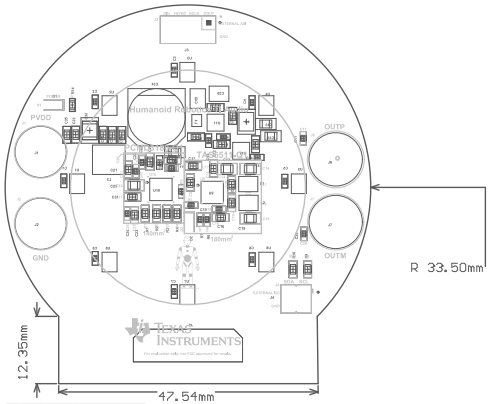
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [illegible]
PLOT NAME = Top Silkscreen Overlay

BOARD #: Robotics Design REV: A SVN REV: Not in version control
IID #: TIDA-060054
GENERATED : 5/20/2026 10:15:14 AM
TEXAS INSTRUMENTS

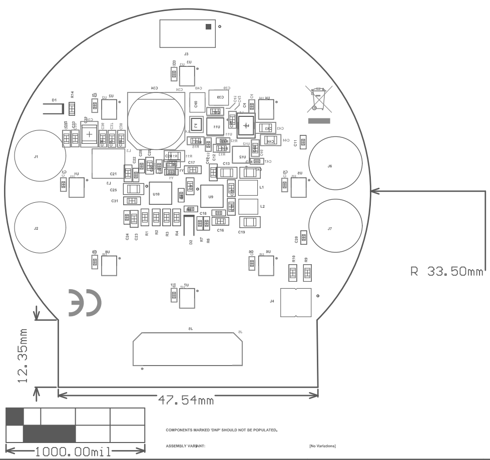
ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER [X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE [ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

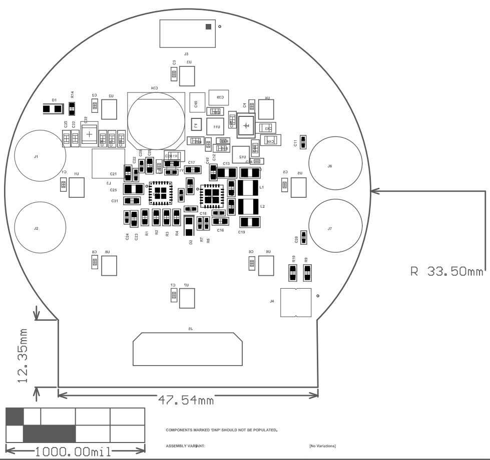
LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE		BOARD #: Robotics Design	REV: A	SVN REV: Not in version control	
LAYER NAME = [illegible]		TID #: TIDA-060054			
PLOT NAME = Bottom Silkscreen Overlay		GENERATED : 5/20/2026	10:18:15 AM	TEXAS INSTRUMENTS	

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
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4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

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DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
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ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc
ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

ALL ARTWORK VIEWED FROM TOP SIDE		BOARD #:	Robotics Design	REV:	A
LAYER NAME =	Top Paste	TID #:	TIDA-060054		
PLOT NAME =	Top Paste Mask Print	GENERATED :	5/20/2026 10:18:17 AM		TEXAS INSTRUMENTS

SVN REV: Not in version control

221 Bevel sized to silkscreened text after final mask. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
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	Dielectric 3	FR-4	39.20mil	4	
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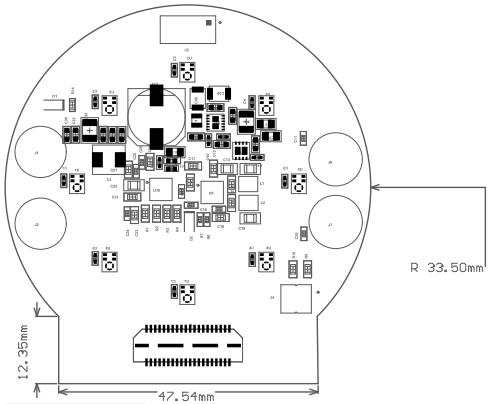
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = Bottom

PLOT NAME = Bottom Paste Mask Print

BOARD #: Robotics Design REV: A SVN REV: Not in version control

SID #: TIDA-060054

GENERATED : 5/20/2026 10:18:19 AM

TEXAS INSTRUMENTS

1	2	3	4	5	6

221 ■ Bevel sized to silkscreen text after final mask. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

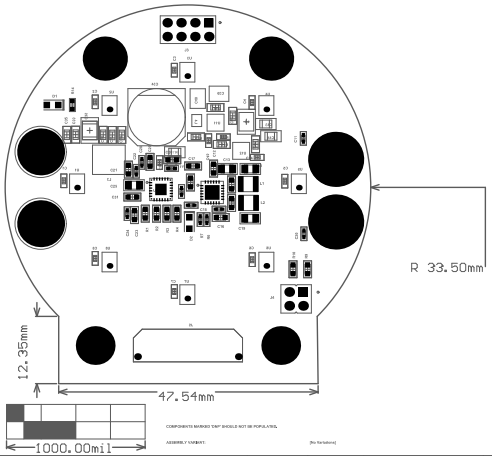
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = Top Solder, Mask, Print, Bottom
PLOT NAME = Top Solder Mask Print

BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 5/20/2026 10:31:20 AM
TEXAS INSTRUMENTS

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

1	2	3	4	5	6

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

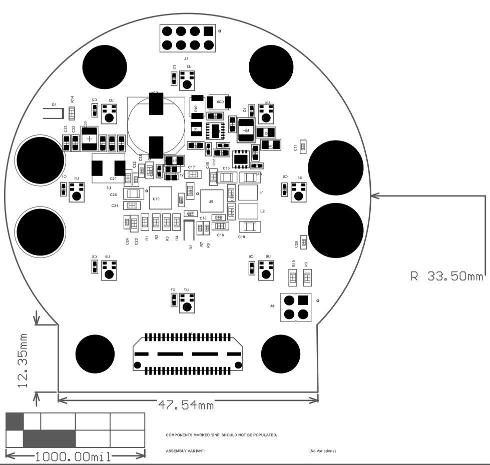
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER ______
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- ______
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- ______

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER ______

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER ______
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER ______
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER ______

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc
ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: Robotics Design	REV: A	SVN REV: Not in version control
LAYER NAME = Bottom Solder	TID #: TIDA-060054		
PLOT NAME = Bottom Solder Mask Print	GENERATED : 5/20/2026 10:18:22 AM		TEXAS INSTRUMENTS

221 ■ Install shield to silkscreened box after final wash. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

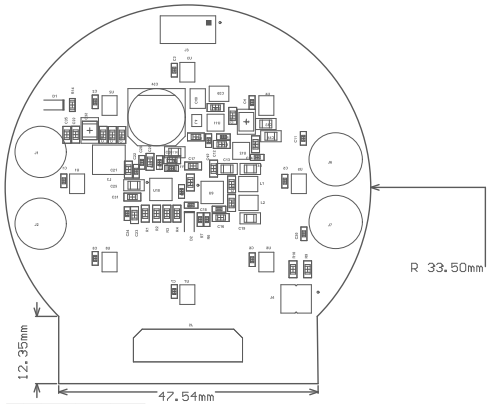
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

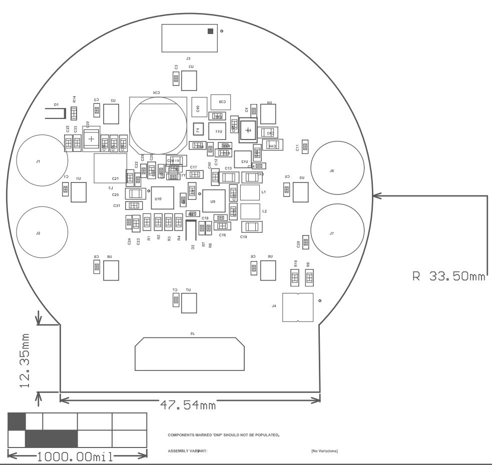
PLOT NAME = M1 Board Outline

BOARD #: Robotics Design REV: A SVN REV: Not in version control

DID #: TIDA-060054

GENERATED : 5/20/2026 10:15:23 AM TEXAS INSTRUMENTS

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: Robotics Design	REV: A	SVN REV: Not in version control
LAYER NAME = [illegible]	TID #: TIDA-060054		
PLOT NAME = M2 Board Dimensions	GENERATED : 5/20/2026	10:18:25 AM	TEXAS INSTRUMENTS

ENGINEER: Garret Godfrey	LAYOUT BY: Tessolve
SCALE: 0.72	ALTIUM DESIGNER VERSION: 23.1.1.15

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

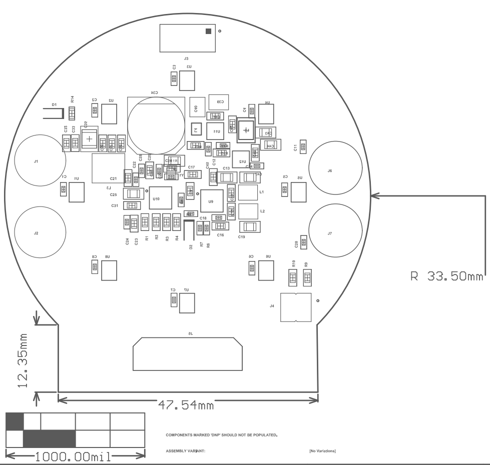
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1. THIS IS IMPEDANCE CONTROLLED BOARD.
2. ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED, PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.
4. 7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES. MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE		BOARD #:	Robotics Design	REV:	A	SVN REV: Not in version control
LAYER NAME =	[illegible]	TID #:	TIDA-060054			
PLOT NAME =	M3 3D STEP Top	GENERATED :	5/20/2026	10:18:26 AM		TEXAS INSTRUMENTS

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

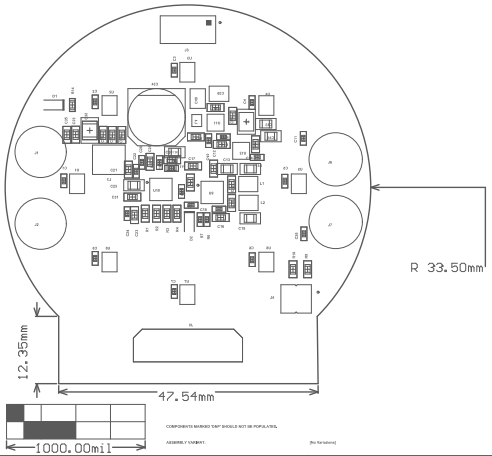
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M4 3D STEP Bottom

BOARD #: Robotics Design REV: A
SWN REV: Not in version control
SID #: TIDA-060054
GENERATED : 5/20/2026 10:15:28 AM
TEXAS INSTRUMENTS

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

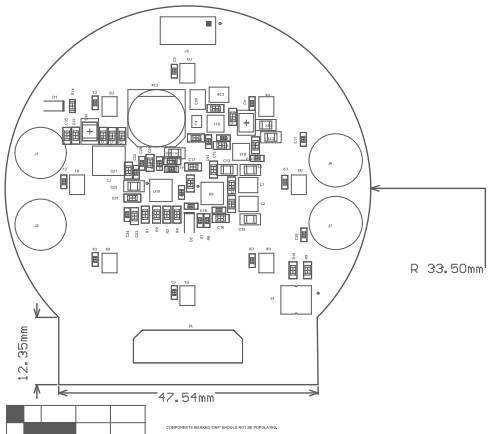
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

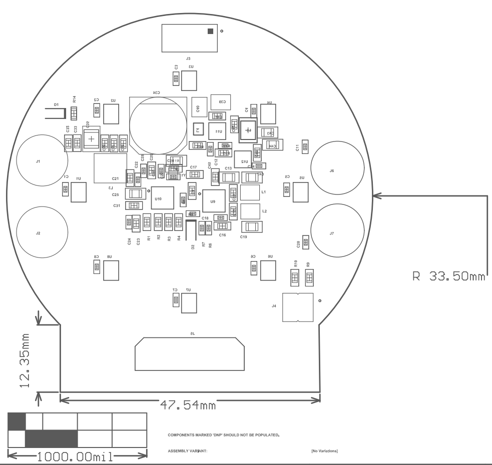
PLOT NAME = M5 Assembly Top

BOARD #: Robotics Design REV: A SVN REV: Not in version control

TID #: TIDA-060054

GENERATED : 5/20/2026 10:15:30 AM TEXAS INSTRUMENTS

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER ______
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- ______
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- ______

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER ______

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER ______
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER ______
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER ______

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SVN REV:	Not in version control
LAYER NAME = [illegible]	TID #:	TIDA-060054				
PLOT NAME = M6 Assembly Bottom	GENERATED :	5/20/2026	10:18:31 AM		TEXAS INSTRUMENTS	

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Board sized to silkscreened box after final mods. Test shall be 0 pt here. Test shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

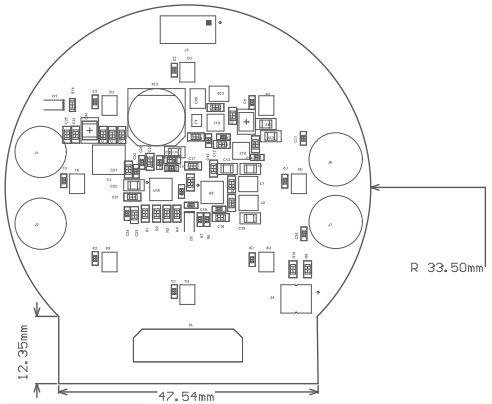
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = Mb.Title Sheet

BOARD #: Robotics_Design REV: A SVN REV: Not in version control
IID #: TIDA-060054
GENERATED : 5/20/2026 10:15:33 AM TEXAS INSTRUMENTS

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Install shield to silkscreened box after final wash. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

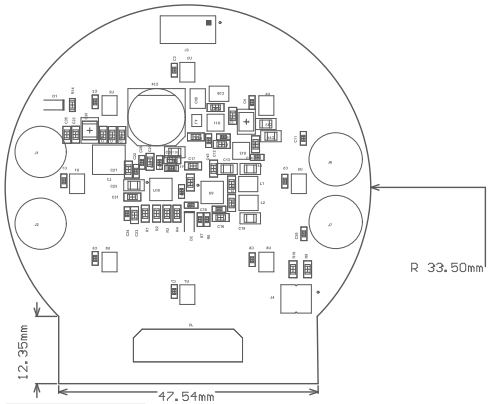
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

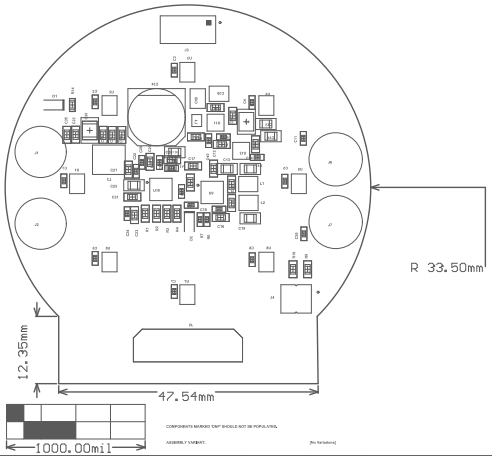
PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M10 Fab Notes

BOARD #: Robotics_Design REV: A SVN REV: Not in version control
3RD #: TIDA-060054
GENERATED : 5/20/2026 10:15:34 AM TEXAS INSTRUMENTS

221	Install shield to silkscreened box after final wash. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.
222	These assemblies are ESD sensitive, ESD precautions shall be observed.
223	These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224	These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = Mid_GerberInformation

BOARD #: Robotics_Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 5/20/2026 10:15:36 AM
TEXAS INSTRUMENTS

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

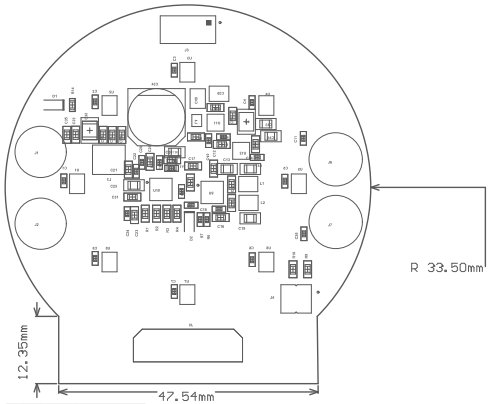
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M12 Stackup
BOARD #: Robotics Design REV: A SVN REV: Not in version control
IID #: TIDA-060054
GENERATED : 5/20/2026 10:15:37 AM TEXAS INSTRUMENTS

221 Bevel sized to silkscreened box after final mask. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

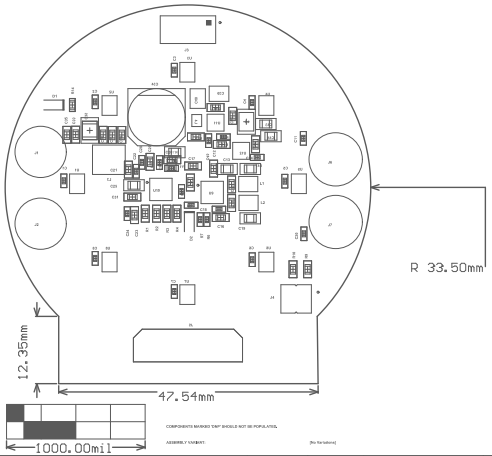
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = M13 Component Bodies Top

BOARD #: Robotics Design REV: A SVN REV: Not in version control

DID #: TIDA-060054

GENERATED : 5/20/2026 10:15:39 AM

TEXAS INSTRUMENTS

221 ■ Board sized to silkscreened size after final mask. Test shall be 0 pt here. Test shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

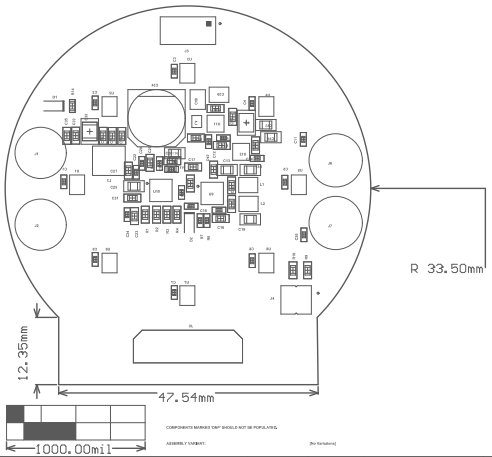
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = M14 Component Bodies Bottom

BOARD #: Robotics Design REV: A SVN REV: Not in version control

TID #: TIDA-060054

GENERATED : 5/20/2026

10:15:40 AM

TEXAS INSTRUMENTS

221 ■ Install shield to silkscreened box after final wash. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

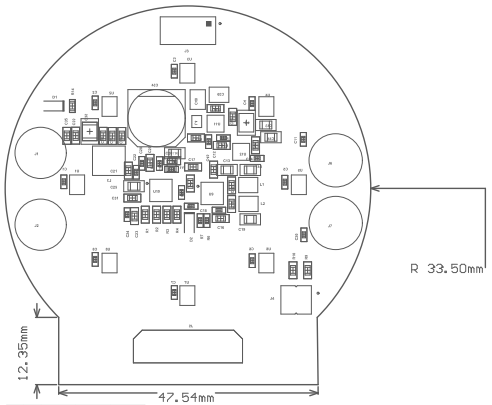
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = M&S Courtyards Top

BOARD #: Robotics Design REV: A SVN REV: Not in version control

DID #: TIDA-060054

GENERATED : 5/20/2026 10:18:42 AM TEXAS INSTRUMENTS

221 ■ Install stand-to-attachment boss after final wash. Test shall be 5 pt hex. Test shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

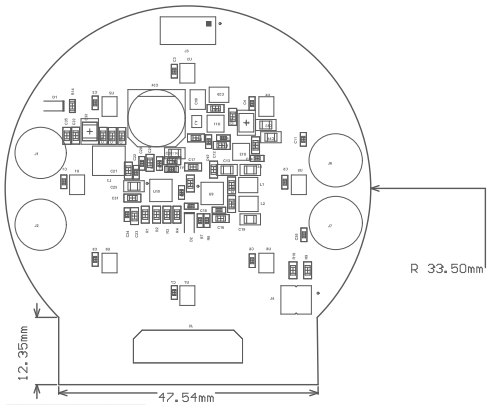
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = M16 Courtyards Bottom

BOARD #: Robotics Design REV: A SVN REV: Not in version control

DID #: TIDA-060054

GENERATED : 5/20/2026 10:15:43 AM

TEXAS INSTRUMENTS

221 ■ Board sized to silkscreened box after final mask. Test shall be 0 pt box. Test shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

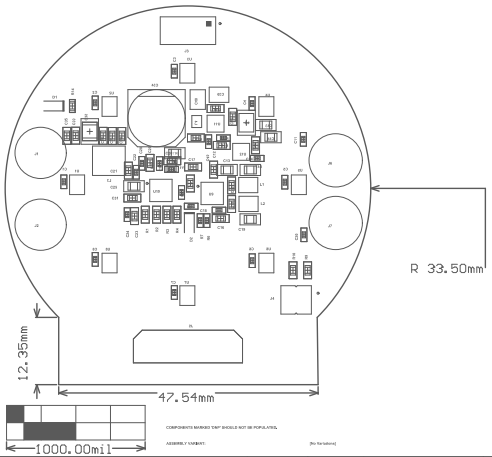
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = M17 Embedded Cavity

BOARD #: Robotics Design REV: A SVN REV: Not in version control

DID #: TIDA-060054

GENERATED : 5/20/2026 10:15:45 AM TEXAS INSTRUMENTS

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

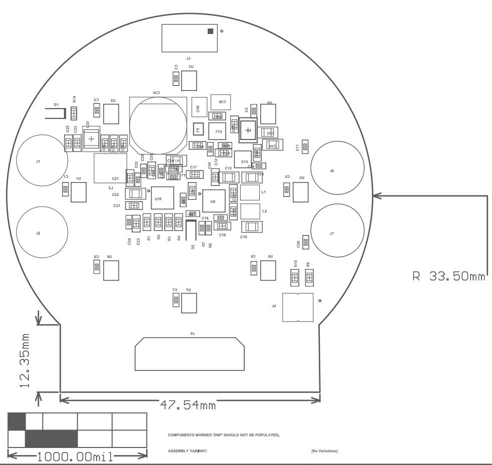
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
- [X] FR-4 [ ] FR-4 High Tg [ ] OTHER ____

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 / [ ] OTHER +/- ____

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 / [ ] OTHER +/- ____

DRILLING:
- REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
- PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER ____

BOARD FINISH:
- SILKSCREEN: [X] TOP [X] BOTTOM
- SILKSCREEN COLOR: [X] WHITE [ ] OTHER ____
- SOLDER RESIST COLOR: [X] GREEN [ ] OTHER ____ / [X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG / [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER ____

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE / [ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
- [X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
- [X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
- MICROSECTION: [ ] YES
- BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
- [ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
- [ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
- [ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
- [ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design	
DESIGNED FOR: TI Internal	
FILE NAME: Robotics_Design.PcbDoc	
ENGINEER: Garret Godfrey	LAYOUT BY: Tessolve
SCALE: 0.72	ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE		BOARD #:	Robotics Design	REV:	A
LAYER NAME =	[illegible]	TID #:	TIDA-060054	SVN REV:	Not in version control
PLOT NAME =	M18 Embedded Assembly	GENERATED :	5/20/2026	10:18:46 AM	TEXAS INSTRUMENTS

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

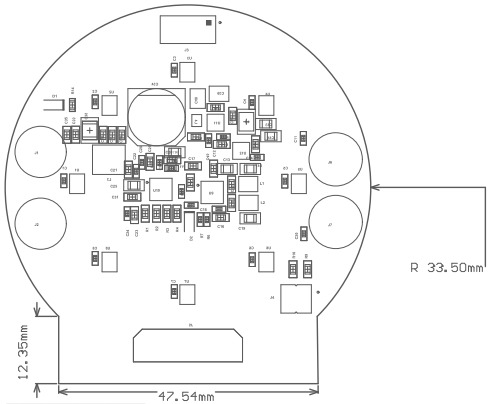
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M40 Embedded Keepout

BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 5/20/2026 10:15:48 AM
TEXAS INSTRUMENTS

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Install shield to silkscreened box after final wash. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

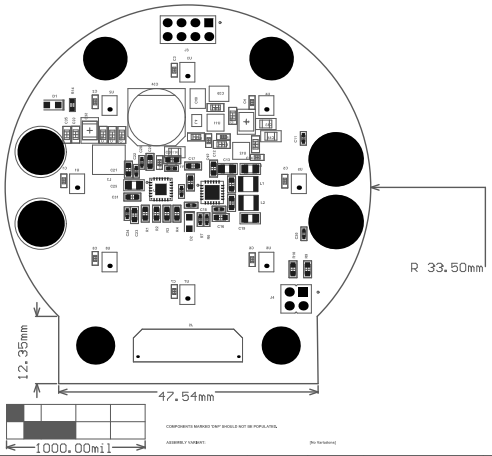
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = Top Pad Master
BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 5/20/2026
10:15:49 AM
TEXAS INSTRUMENTS

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

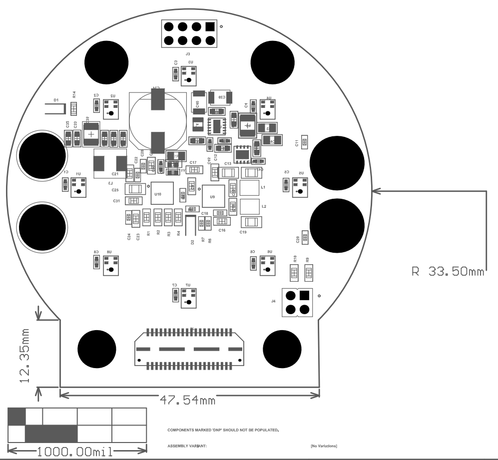
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER [X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE [ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

ALL ARTWORK VIEWED FROM TOP SIDE		BOARD #:	Robotics Design	REV:	A
SVN REV:	Not in version control				
LAYER NAME =	[illegible]Bottom	TID #:	TIDA-060054		
PLOT NAME =	Bottom Pad Master	GENERATED :	5/20/2026	10:18:51 AM	TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Board sized to silkscreened box after final mods. Test shall be 8 pt box. Test shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

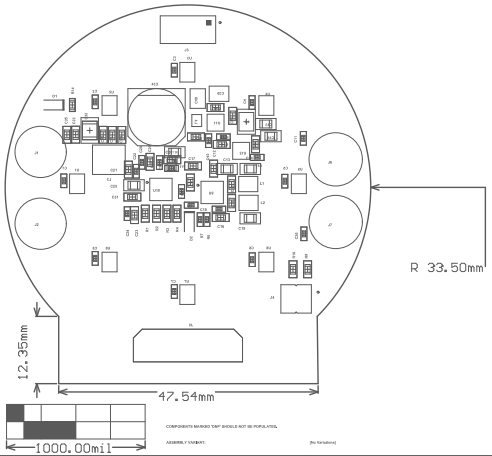
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
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4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = Keep Out Layer
BOARD #: Robotics Design REV: A SVN REV: Not in version control
STD #: TIDA-060054
GENERATED : 5/20/2026 10:15:53 AM TEXAS INSTRUMENTS

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

DRILL TABLE

Symbol	Count	Hole Size	Plated	Hole Type
⌘	13	7.87mil (0.200mm)	PTH	Round
▼	227	10.00mil (0.254mm)	PTH	Round
□	8	31.50mil (0.800mm)	NPTH	Round
⊕	2	39.37mil (1.000mm)	NPTH	Round
○	8	40.00mil (1.016mm)	PTH	Round
✡	4	47.24mil (1.200mm)	PTH	Round
⊠	2	126.00mil (3.200mm)	PTH	Round
◇	2	129.92mil (3.300mm)	PTH	Round
▣	2	144.00mil (3.658mm)	PTH	Round
▽	2	214.57mil (5.450mm)	PTH	Round
	270 Total			

FOR 7.87 MIL DRILL +0/-7.87MIL
FOR 10 MIL DRILL +0/-10 MIL
FOR NPTH +/- 2MIL
FOR PTH +/- 3MIL

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
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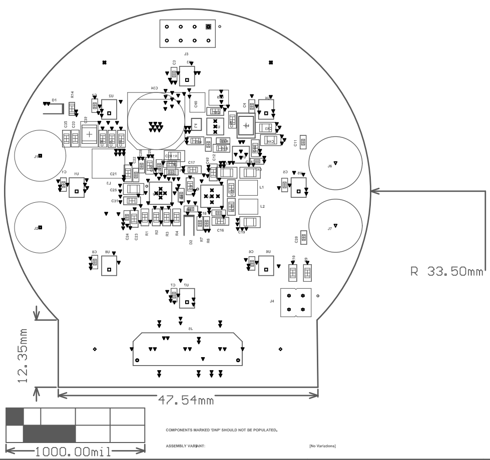


COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER [X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE [ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc
ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE		BOARD #: Robotics Design	REV: A	SVN REV: Not in version control
LAYER NAME = Drill Drawing		TID #: TIDA-060054	
PLOT NAME = Drill Drawing For (L1_TOP - L6_Bottom)		GENERATED : 5/20/2026 10:18:54 AM	TEXAS INSTRUMENTS

221 ■ Board sized to silkscreened box after final mask. Test shall be 0 pt here. Test shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

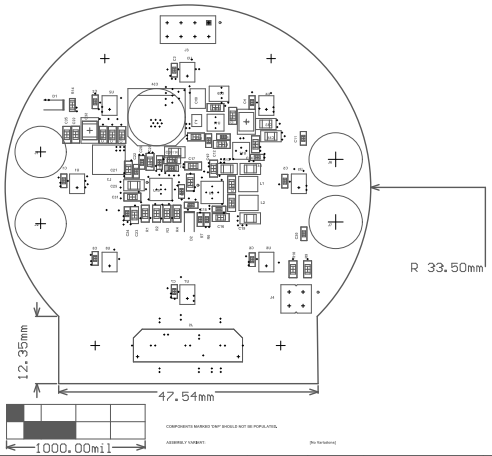
IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%



FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = Drill Guide For (L1_TOP - L6_Bottom)

BOARD #: Robotics Design REV: A SVN REV: Not in version control

TID #: TIDA-060054

GENERATED : 5/20/2026 10:15:56 AM

TEXAS INSTRUMENTS

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