

- 011  Drill used in fabrication was 100% fresh. You must use 20 Year Old drill for the Lead holes in the PCB substrate.
- 012  Use acceptable and RIGID materials for the solder.
- 013  Use acceptable and RIGID materials for the solder.
- 014  Use acceptable and RIGID materials for the solder.
- 015  Use acceptable and RIGID materials for the solder.

IMPEDANCE TABLE:

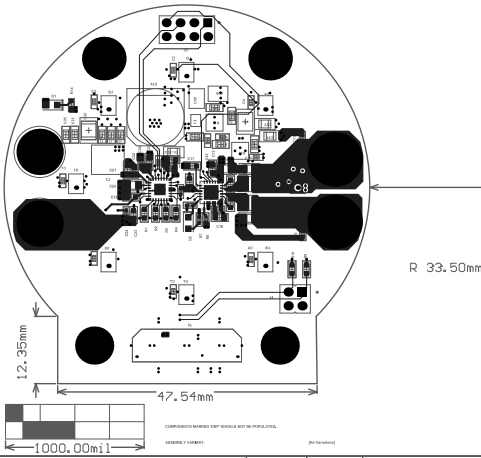
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:			68.00mil		+/-10%

FAB NOTES

- 1. THIS IS IMPROVED CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENCING" COVERING REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS: +/-0.001" ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  V. SCORE  
 N.C. ROUTE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS 2  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL1549 REQUIREMENTS.  
 PCB MUST BEAR THE UL1549-UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



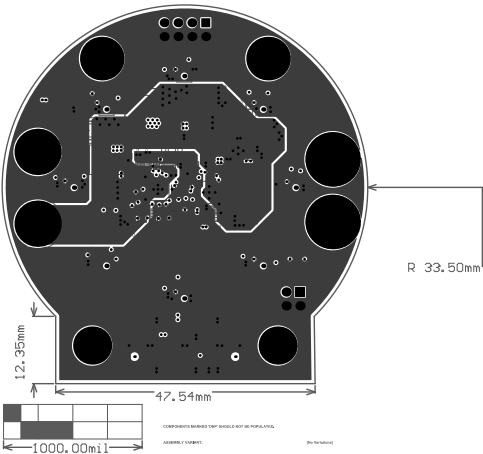
PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL WORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SWN REV:	MOLAS VERSION CONTROL	TEXAS INSTRUMENTS (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	BOARD #:	3DA-26054	REV:		DATE:	06/16/24	TEXAS INSTRUMENTS
PLQ NAME =	GENERATED:	06/28/2025	DATE:	06/16/24	TIME:	06:16:04 AM	TEXAS INSTRUMENTS

- 001  Mask used is alternative to other mask sets. You must use 2.5 Mic. You must use the Lead Frame for the PCB substrate.
- 002  Mask assembly on 400 umhole size (not for solder).
- 003  Mask assembly on 400 umhole size (not for solder).
- 004  Mask assembly on 400 umhole size (not for solder).
- 005  Mask assembly on 400 umhole size (not for solder).



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR-4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR-4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR-4	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR-4	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	FR-4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:			68.00mil		+/-10%

FAB NOTES

1. THIS IS IMPEDANCE CONTROLLED BOARD.
2. ALL VIAS ARE TENTED IN BOTH SIZES UNLESS OTHERWISE MASK OPENED IN GERBER.
3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
4. 0.75mm VIAS VMS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/4958N AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS +/-0.0002(0.01") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER \_\_\_\_\_  
 THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER Refer stack up

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRELLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

ARRAY/PANEL:  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs  
 TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS 1  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL1549 REQUIREMENTS.  
 PCB MUST BEAR THE UL1549-4 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES  
 MICROSECTION:  YES  NONE  REQUIRED  PER ORDER

BARE BOARD ELEC. TEST:  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE:  
Robotics Design

DESIGNED FOR:  
TI Internal

FILE NAME:  
Robotics\_Design.PcbDoc

ENGINEER:  
Garret Godfrey

LAYOUT BY:  
Tessadve

SCALE: 0.72

ALTIM DESIGNER VERSION:  
23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE		BOARD #:	Robotics Design	REV#:	A	SWN-REV:	MOLAS version control	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	
LAYER NAME =	XXXXXXXXXXXXXXXXXXXX	IPC #:	IPC-A-6005A	DATE:	6/28/2025	TIME:	10:18:06 AM	TEKAS INSTRUMENTS	
PLQ NAME =	L2MINDA	GENERATED:	6/28/2025	DATE:	6/28/2025	TIME:	10:18:06 AM	TEKAS INSTRUMENTS	

- 001  Drill used in fabrication was finer than used. You will be 2-3 hrs. You need to use the Lead table for the PCB materials.
- 002  Trace accuracy on 400 um/min. 400 um/min. (not for design).
- 003  Trace accuracy on 400 um/min. 400 um/min. (not for design).
- 004  Trace accuracy on 400 um/min. 400 um/min. (not for design).
- 005  Trace accuracy on 400 um/min. 400 um/min. (not for design).

IMPEDANCE TABLE:

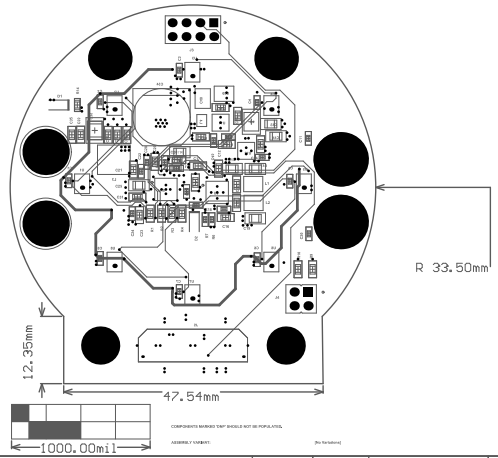
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_SIGNAL	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_BOTTOM	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.00mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIZES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS +/-0.001mm ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  V. SCORE  
 N.C. ROUTE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 1  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SWM REV:	MOLAS/ANISH/CONTROL	TEXAS INSTRUMENTS (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	IPC #:	2DA-00054	DATE:	6/28/2025	06:16:07 AM	TEKAS INSTRUMENTS	ENGINEER: Garrett Godfrey LAYOUT BY: Tessadve
PLQ NAME =	GENERATED:	6/28/2025	06:16:07 AM	TEKAS INSTRUMENTS	SCALE: 0.72	ALTRUM DESKMAN VERSION: 23.1.1.15	

- 001  Drill used & dimensions are per hole size. The drill is 2.5mm. The hole is per the Lead Table in the BOM extension.
- 002  Hole locations are 400 microns (0.0157 inches) offset from center.
- 003  Hole locations are 400 microns (0.0157 inches) offset from center. The hole is per the Lead Table in the BOM extension.
- 004  Hole locations are 400 microns (0.0157 inches) offset from center. The hole is per the Lead Table in the BOM extension.
- 005  Hole locations are 400 microns (0.0157 inches) offset from center. The hole is per the Lead Table in the BOM extension.

IMPEDANCE TABLE:

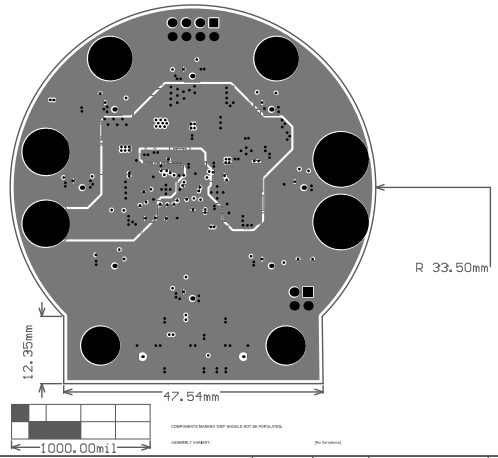
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR4	4.00mil	4	
3	LL_SIGNAL	Copper	1.83mil		
	Dielectric 3	FR4	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR4	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	FR4	4.00mil	4	
6	LL_BOTTOM	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:			68.00mil		+/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIZES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS +/-0.001mm ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/-

**DRELLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENIG  
 IMM. TIN/SILVER OR EQUIV  OTHER

ARRAY/PANEL:  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS 2  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER  
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

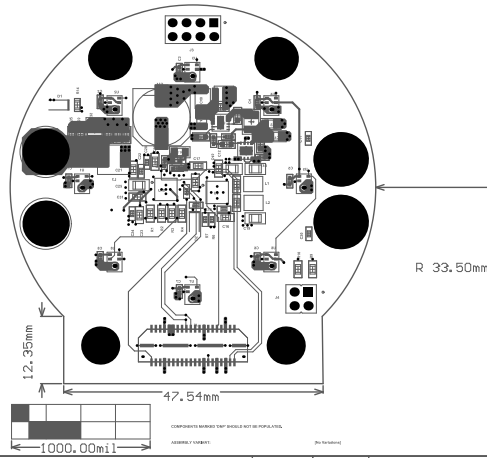
DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL PARTWORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	DATE:	06/18/2025	TIME:	08:18:09 AM	DESIGNER:	Garret Godfrey	ENGINEER:	Garret Godfrey	LAYOUT BY:	Tessadve	ALTRUM DESIGNER VERSION:	23.1.1.15
LAYER NAME =	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221	IPC-2221
PLQ NAME =	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2	LL_GND2



- 011  Drill used to determine via hole sizes. You will be 2.5x. You need to use the Drill table in the PTH software.
- 012  Use accuracy on 400 micron. 400 micron does not fit.
- 013  Use accuracy on 400 micron. 400 micron does not fit.
- 014  Use accuracy on 400 micron. 400 micron does not fit.
- 015  Use accuracy on 400 micron. 400 micron does not fit.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL	REFERENCE
	+/- 10% Tolerance	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_Pwr	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Bottom	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:			68.00mil		+/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCES FOLLOWED: 0.020mm (0.001") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  V. SCORE  
 N.C. ROUTE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS 2  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**BARE BOARD ELEC. TEST:**  NONE  REQUIRED  PER ORDER

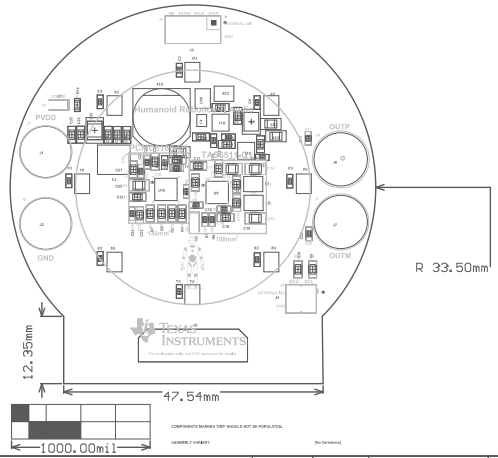
XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design  
 DESIGNED FOR: TI Internal  
 FILE NAME: Robotics\_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SWN REV:	Molias version control	TEXAS INSTRUMENTS (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	IPC #:	2DA-00054	DATE:	6/28/2025	TIME:	06:16:12 AM	TEXAS INSTRUMENTS
PLQ NAME =	GENERATED:	6/28/2025	DATE:	06/16/12 AM	TIME:		TEXAS INSTRUMENTS

- 001:  Must meet 6-ounce minimum copper thickness. This must be 2-ounce for Lead-Free for the FR-4 substrate.
- 002:  Must meet 2-ounce minimum copper thickness for the copper.
- 003:  Must meet 2-ounce minimum copper thickness for the copper.
- 004:  Must meet 2-ounce minimum copper thickness for the copper.
- 005:  Must meet 2-ounce minimum copper thickness for the copper.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR-4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR-4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR-4	39.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR-4	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	FR-4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.00mil

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE FOLLOWED IS +/-0.0025(0.101") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER  Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM  OTHER

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 1  1  2  3  RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL RIGHTS RESERVED	BOARD #:	Robotics Design	REV:	A	DATE REV:	06/16/2020	DESIGNED BY:	Garret Godfrey	DESIGNED FOR:	TI Internal	
LAYER NAME =	TOP SHEET OVERLAY	BOARD #:	RODA-00054	REV:	A	DATE REV:	06/16/2020	DESIGNED BY:	Garret Godfrey	DESIGNED FOR:	TI Internal
PLQID NAME =	Top Sheet Overlay	GENERATED:	06/20/2020	06/16/14 AM	TEKAS INSTRUMENTS						

ENGINEER:	Garret Godfrey	LAYOUT BY:	Tessalve
SCALE:	0.72	ALTRUM DESIGNER VERSION:	23.1.1.15

- 001  Drill used to determine hole field sizes. The drill bit is 2.5mm. The hole size per the Lot# table in the POP instructions.
- 002  Laser assisted on 400 um pitch 400 um diameter hole size.
- 003  Laser assisted on 400 um pitch 400 um diameter hole size.
- 004  Laser assisted on 400 um pitch 400 um diameter hole size.
- 005  Laser assisted on 400 um pitch 400 um diameter hole size.

IMPEDANCE TABLE:

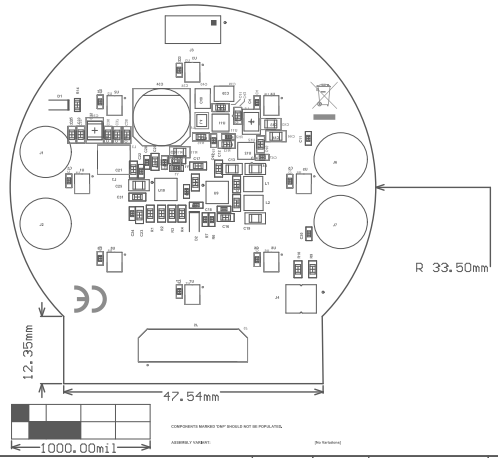
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack	
	Top Overlay					
	Top Solder	Solder Resist	1.25um	3.5		
1	LL_TOP	Copper	1.83um			
	Dielectric 1	FR4	4.07um	4		
2	LL_GND1	Copper	1.83um			
	Dielectric 2	FR4	4.07um	4		
3	LL_Signal	Copper	1.83um			
	Dielectric 3	FR4	39.20um	4		
4	LL_GND2	Copper	1.83um			
	Dielectric 4	FR4	4.07um	4		
5	LL_PWR	Copper	1.83um			
	Dielectric 5	FR4	4.07um	4		
6	LL_Solder	Copper	1.83um			
	Bottom Solder	Solder Resist	1.25um	3.5		
	Bottom Overlay					
Total board thickness:					69.00um	+/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIZES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.51) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE FOLLOWANCE IS +/-0.0025(0.1017) ON TOP SIDES. MINIMUM ANNULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNULAR RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR4  FR-4 High Tg  OTHER  Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERPIS

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 3  RoHS  1  2  3  PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design  
 DESIGNED FOR: TI Internal  
 FILE NAME: Robotics\_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	DATE REV:	MoJa version control	TEXAS INSTRUMENTS (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = Bottom_SilkScreen Overlay	JOB #:	13DA-00054	DATE:	6/28/2025	TIME:	06:16:15 AM	TEXAS INSTRUMENTS
PLQI.NAME =	GENERATED:	6/28/2025	DATE:	06/16/15 AM	TIME:		TEXAS INSTRUMENTS

- 001  Mask used is dimensions are not fixed, they will be 2.0mm. You need to use the Lead table in the POP software.
- 002  Mask resolution is 400 microns. All dimensions that are shown.
- 003  Mask resolution is 400 microns. All dimensions that are shown.
- 004  Mask resolution is 400 microns. All dimensions that are shown.
- 005  Mask resolution is 400 microns. All dimensions that are shown.

IMPEDANCE TABLE:

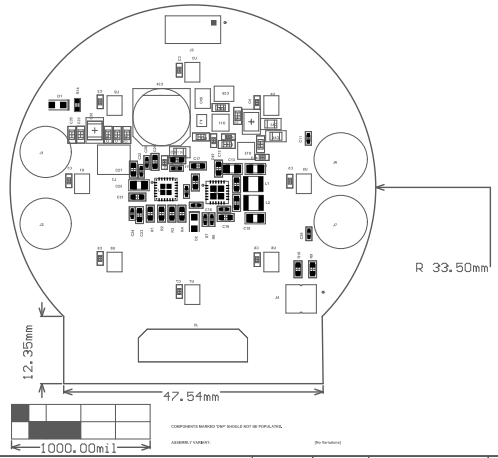
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR-4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR-4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR-4	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR-4	4.00mil	4	
5	LL_Pwr	Copper	1.83mil		
	Dielectric 5	FR-4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.00mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIZES UNLESS OTHERWISE MASK OPENED IN GERBERS.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "QA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS +/-0.0025(0.10") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER  Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM  OTHER

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  V. SCORE

N.C. ROUTE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 2  1  2  3

RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  NONE  REQUIRED  PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



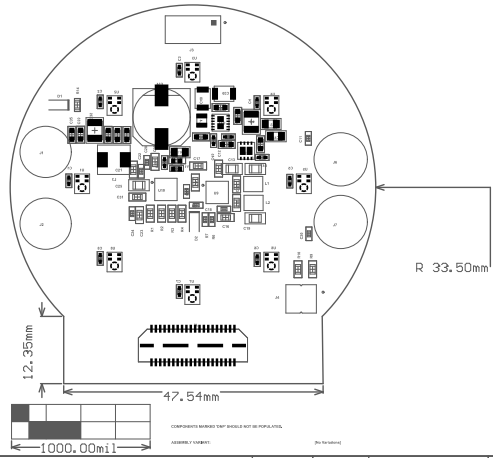
PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL RIGHTS RESERVED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SWN-REV:	MOLAS version control	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = TopMask.Mask Print	ID #:	3DA-00054	DATE:	6/28/2025	TIME:	10:16:17 AM	TEKAS INSTRUMENTS
ENGINEER:	Garret Godfrey	LAYOUT BY:	Tessadve	ALTRUM DESKMAN VERSION:	23.1.1.15		
SCALE:	0.72						

- 001  Mask used is different than other Mask sets. You will be 2-4 hrs. You need to use the Lead table in the POP software.
- 002  Mask resolution is 400 microns. 400 microns shall be used.
- 003  Mask resolution is 400 microns. 400 microns shall be used.
- 004  Mask resolution is 400 microns. 400 microns shall be used.
- 005  Mask resolution is 400 microns. 400 microns shall be used.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR4	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR4	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	FR4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:			68.20mil		+/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIZES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS +/-0.001mm ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS ARE WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  V. SCORE  
 N.C. ROUTE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 2  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**BARE BOARD ELEC. TEST:**  NONE  REQUIRED  PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



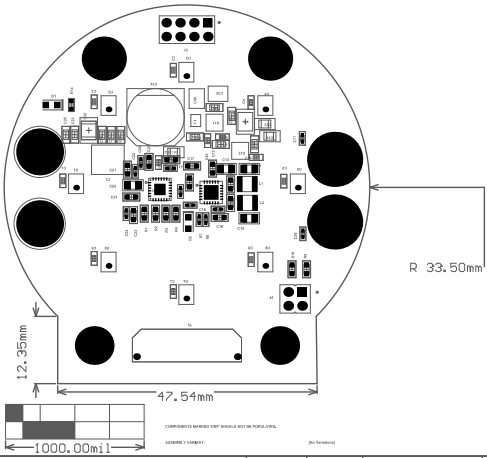
PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL-ARTWORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV#:	A	DATE REV:	MoJa version control	TEXAS INSTRUMENTS
LAYER NAME = BottomBase Mask Print	JOB #:	EDA-00054	DATE:	6/28/2025	TIME:	10:16:19 AM	TEXAS INSTRUMENTS
ENGINEER:	DESIGNED BY:	Garret Godfrey	DESIGNED BY:	Tessadve	DATE:	6/28/2025	SCALE: 0.72
LAYOUT BY:	ALTRUM DESIGNER VERSION:	Tessadve	ALTRUM DESIGNER VERSION:	23.1.1.15			

- 001  Mask used is alternative non-ferrous mask. The mask is 2.5um. The mask is per the Lead rule in the ERP software.
- 002  Mask resolution is 400 um/min. 400 um/min does not fit data.
- 003  Mask resolution is 400 um/min and the mask is 2.5um. The mask is per the Lead rule in the ERP software.
- 004  Mask resolution is 400 um/min and the mask is 2.5um. The mask is per the Lead rule in the ERP software.
- 005  Mask resolution is 400 um/min and the mask is 2.5um. The mask is per the Lead rule in the ERP software.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL	REFERENCE
	+/- 10% Tolerance	
TRACE WIDTH		
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25um	3.5	
1	LL_TOP	Copper	1.83um		
	Dielectric 1	Fiberglass	4.00um	4	
2	LL_GND1	Copper	1.83um		
	Dielectric 2	Fiberglass	4.00um	4	
3	LL_Signal	Copper	1.83um		
	Dielectric 3	Fiberglass	35.20um	4	
4	LL_GND2	Copper	1.83um		
	Dielectric 4	Fiberglass	4.00um	4	
5	LL_PWR	Copper	1.83um		
	Dielectric 5	Fiberglass	4.00um	4	
6	LL_Solder	Copper	1.83um		
	Bottom Solder	Solder Resist	1.25um	3.5	
	Bottom Overlay				
Total board thickness:			60.00um		+/-10%

FAB NOTES

1. THIS IS IMPEDANCE CONTROLLED BOARD.
2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS +/-0.001mm ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 1  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

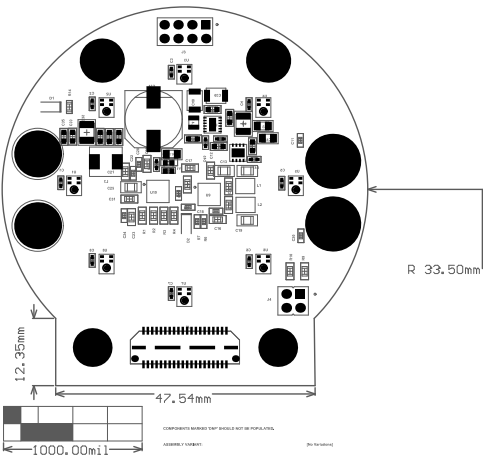
FILE NAME: Robotics\_Design\_PcbDoc

ENGINEER: Garrett Godfrey LAYOUT BY: Tessa Ivo

SCALE: 0.72 ALTRUIX DESKMAN VERSION: 23.1.1.15

ALL RIGHTS RESERVED	BOARD #:	Robotics Design	REV:	A	SWM REV:	Major version control	TEXAS INSTRUMENTS (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = TopSolderMask.PcbDoc	SD #:	3DA-00054	DATE:	6/28/2025	08:16:20 AM	TEKAS INSTRUMENTS	
PLQ NAME = TopSolderMask.PcbDoc	GENERATED:	6/28/2025	08:16:20 AM	TEKAS INSTRUMENTS			

- 001  Mask used to determine via fill hole size. The mask is 2.0mm. The hole is per the Lead Table in the BOM extension.
- 002  Mask used to determine via fill hole size. The mask is 2.0mm. The hole is per the Lead Table in the BOM extension.
- 003  Mask used to determine via fill hole size. The mask is 2.0mm. The hole is per the Lead Table in the BOM extension.
- 004  Mask used to determine via fill hole size. The mask is 2.0mm. The hole is per the Lead Table in the BOM extension.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR-4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR-4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR-4	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR-4	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	FR-4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1. THIS IS IMPEDANCE CONTROLLED BOARD.
2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/4958N AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS +/-0.0002(0.01") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER  Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 1  1  2  3  RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**BARE BOARD ELEC. TEST:**  NONE  REQUIRED  PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ENGINEER: Garrett Godfrey LAYOUT BY: Tessa Ivo

SCALE: 0.72 ALTRUIX DESKMAN VERSION: 23.1.1.15

ALL RIGHTS RESERVED. VIEWED FROM TOP SIDE.	BOARD #:	Robotics Design	REV:	A	SWM REV:	MOLAS: version control	TEXAS INSTRUMENTS (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = BottomSolderMask.PcbDoc	3D #:	3DA-00054	DATE:	6/28/2026	08:18:22 AM	TEXAS INSTRUMENTS	
PLQ NAME = BottomSolderMask.PcbDoc	GENERATED:	6/28/2026	DATE:	08:18:22 AM	08:18:22 AM	TEXAS INSTRUMENTS	

- 001  Drill used to determine hole/through hole. The drill bit is 2.0mm. The hole is per the Lead Table in the POP reference.
- 002  Hole accuracy on 400 micron. 400 micron does not fit.
- 003  Hole accuracy on 400 micron. 400 micron does not fit.
- 004  Hole accuracy on 400 micron. 400 micron does not fit.
- 005  Hole accuracy on 400 micron. 400 micron does not fit.

IMPEDANCE TABLE:

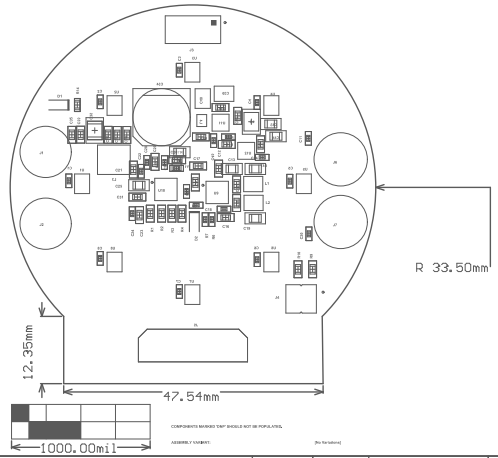
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR-4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR-4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR-4	39.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR-4	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	FR-4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.00mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/4958N AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE FOLLOWANCE IS +/-0.0025(0.10") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER  Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENIG

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  V. SCORE

N.C. ROUTE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 1  1  2  3

RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	DATE REV:	MoJas.walsh@ti.com	TEXAS INSTRUMENTS (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	BOARD #:	3DA-00054	REV:		DATE REV:		
PLOT NAME =	GENERATED:	6/28/2025	DATE REV:	06/18/23 AM	DATE REV:		TEXAS INSTRUMENTS

- 001  Drill used is dimensioned on the Drill List. The drill bit is 2.0mm. The drill bit is used for the Lead Pad in the PCB.
- 002  The assembly is on 400 micron 400 microns drill bit.
- 003  The assembly is on 400 micron 400 microns drill bit.
- 004  The assembly is on 400 micron 400 microns drill bit.
- 005  The assembly is on 400 micron 400 microns drill bit.

IMPEDANCE TABLE:

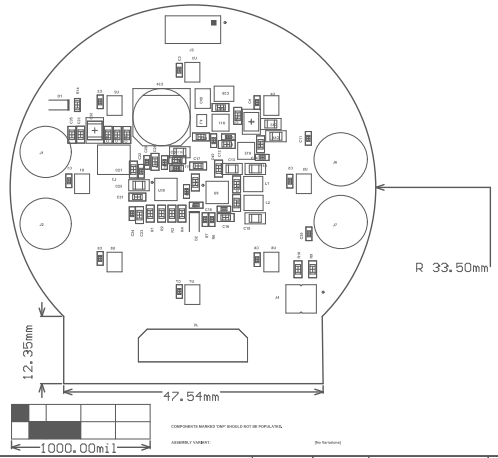
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.00mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE FOLLOWED IS +/-0.0025(0.10") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER  Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM  OTHER

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  V. SCORE

N.C. ROUTE  N.C. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 3 >  1  2  3

RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**BARE BOARD ELEC. TEST:**  NONE  REQUIRED  PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL RIGHTS RESERVED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	DATE REV:	MoJas.walsh@ti.com	TEXAS INSTRUMENTS (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	3D #:	3DA-00054	DATE:	6/28/2025	08:16:25 AM	TEXAS INSTRUMENTS	ENGINEER: Garrett Godfrey
PLOT NAME =	GENERATED:	6/28/2025	08:16:25 AM	TEXAS INSTRUMENTS	LAYOUT BY: Tessalve	ALTRUM DESKMAN VERSION: 23.1.1.15	SCALE: 0.72

- 001  Drill used is dimensioned on the Drill Note. The drill bit is 2.0mm. The drill bit is used for the Lead Pad in the PCB substrate.
- 002  Drill used is dimensioned on the Drill Note. The drill bit is 2.0mm. The drill bit is used for the Lead Pad in the PCB substrate.
- 003  Drill used is dimensioned on the Drill Note. The drill bit is 2.0mm. The drill bit is used for the Lead Pad in the PCB substrate.
- 004  Drill used is dimensioned on the Drill Note. The drill bit is 2.0mm. The drill bit is used for the Lead Pad in the PCB substrate.

IMPEDANCE TABLE:

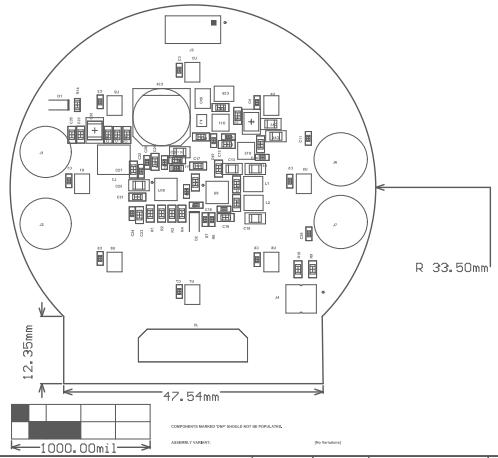
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.00mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENCING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCES FOLLOWED: DRILL: +/-0.0025mm ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS ARE WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  V. SCORE

N.C. ROUTE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 2  1  2  3

RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL RIGHTS RESERVED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	OWN REV:	MOLAS: version control	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	BOARD #:	3DA-00054	REV:				
PLOT NAME =	GENERATED:	6/28/2025	08:16:26 AM	TEXAS INSTRUMENTS			

- 001  Drill used in fabrication was 100% fresh. The drill bit is 2.0mm. The drill bit was the Lead Drill bit for the PCB substrate.
- 002  The assembly was done in a clean room.
- 003  The assembly was done in a clean room with the use of a clean room.
- 004  The assembly was done in a clean room with the use of a clean room.

IMPEDANCE TABLE:

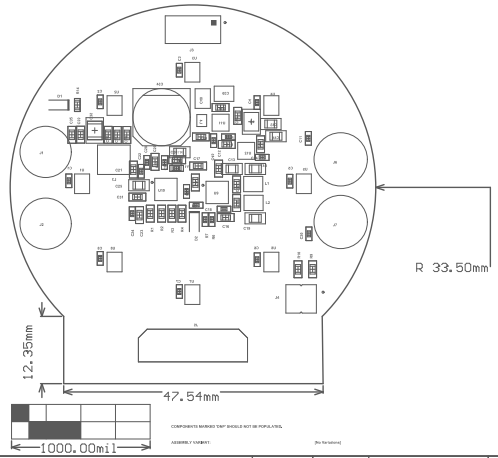
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR-4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR-4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR-4	39.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR-4	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	FR-4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					69.20mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5)
- AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED.
- PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/485IN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE IS +/-0.0025(0.10") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER \_\_\_\_\_

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER Refer stack up

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_

SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERPIS  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS >  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

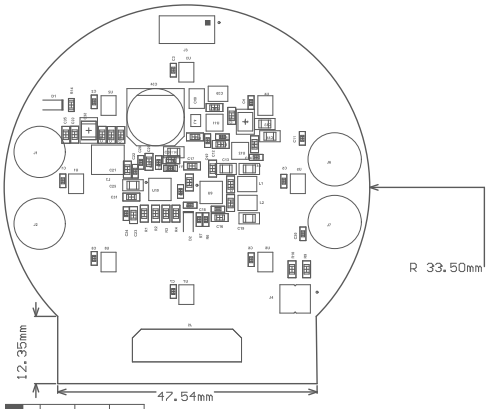
**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design  
 DESIGNED FOR: TI Internal  
 FILE NAME: Robotics\_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	OWN REV:	MOLAS/ANISH/CONTROL	TEXAS INSTRUMENTS (TI) and/or its Escrowers do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its Escrowers do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its Escrowers do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	IPC #:	IPC-A-6005A	DATE:	6/28/2025	08:16:28 AM	TEXAS INSTRUMENTS	ENGINEER: Garrett Godfrey LAYOUT BY: Tessadve ALTRUM DESIGNER VERSION: 23.1.1.15
PLOT NAME =	GENERATED:	6/28/2025	08:16:28 AM	TEXAS INSTRUMENTS	SCALE: 0.72		

- 001  All board and dimensions are in millimeters. The unit is in feet. The unit is in feet for the Lead table in the BOM tables.
- 002  All dimensions are in millimeters. All dimensions are in millimeters.
- 003  All dimensions are in millimeters. All dimensions are in millimeters. All dimensions are in millimeters.
- 004  All dimensions are in millimeters. All dimensions are in millimeters. All dimensions are in millimeters.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL	REFERENCE
	+/- 10% Tolerance	
TRACE WIDTH		
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR-4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR-4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR-4	39.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR-4	4.00mil	4	
5	LL_Pwr	Copper	1.83mil		
	Dielectric 5	FR-4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.00mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TIENTED IN BOTH SIZES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5)
- AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED.
- PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TIENTING / COVERING" REQUIREMENTS.
- 4. 0.75MM VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/485N AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS +/-0.0025(0.10") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER  Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENIG

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  V. SCORE

N.C. ROUTE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 1  1  2  3

RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  PER ORDER

XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

LAYER 2 & 3 (INNER LAYERS) XX MIL VIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ENGINEER: Garrett Godfrey LAYOUT BY: Tessadve

ALTRUM DESKMAN VERSION: 23.1.1.15

SCALE: 0.72

ALL RIGHTS RESERVED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SWM REV:	M01A version control	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	TOP	TOP	TOP	TOP	TOP	TOP	
PLOT NAME =	M01Assembly Top	GENERATED :	6/28/2025	08:16:30 AM	TEXAS INSTRUMENTS		



- 001 ■ Lead used is 63/37 eutectic solder. The lead is 2.0mm. The lead is not to be used for the Lead in the PCB substrate.
- 002 ■ Lead used is 63/37 eutectic solder. The lead is 2.0mm. The lead is not to be used for the Lead in the PCB substrate.
- 003 ■ Lead used is 63/37 eutectic solder. The lead is 2.0mm. The lead is not to be used for the Lead in the PCB substrate.
- 004 ■ Lead used is 63/37 eutectic solder. The lead is 2.0mm. The lead is not to be used for the Lead in the PCB substrate.

IMPEDANCE TABLE:

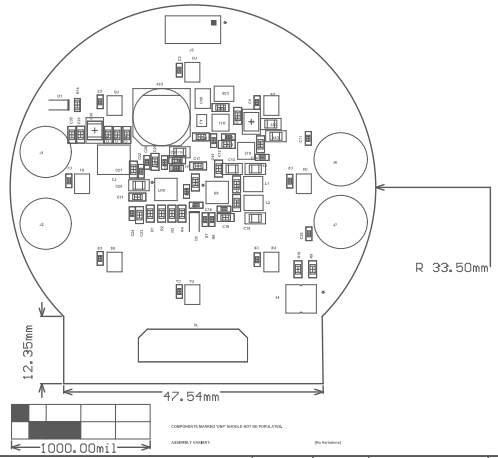
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR-4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR-4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR-4	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR-4	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	FR-4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.20mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBERS.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/4958N AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS +/-0.002(0.001") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS ARE WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER \_\_\_\_\_

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER \_\_\_\_\_ Refer stack up

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

ARRAY/PANEL:  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs  
 TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS 3 >  1  2  3  
 RoHS  OTHER \_\_\_\_\_ PER ORDER

ALL BOARDS MUST MEET OR EXCEED ILS4V9 REQUIREMENTS.  
 PCB MUST BEAR THE ILS4V-4 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES  
**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER  
**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL VIDE, XX MIL SPACE  
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



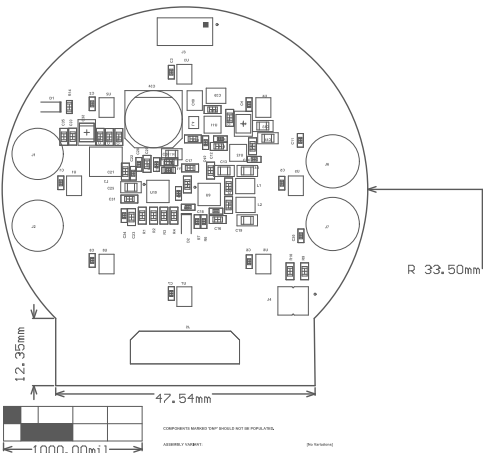
PRODUCT TITLE:  
Robotics Design

DESIGNED FOR:  
TI Internal

FILE NAME:  
Robotics\_Design.PcbDoc

ALL RIGHTS RESERVED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SWN-REV:	M01.00000000 control	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	BOARD #:	3DA-00054	REV:		GENERATED:	6/28/2026	08:16:33 AM
PLOT NAME =	GENERATED:	6/28/2026	08:16:33 AM	TEKAS REQUIREMENTS	SCALE:	0.72	LAYOUT BY: Tessadve
							ALTRUM DESIGNER VERSION: 23.1.1.15

- 001  All board and dimensions are in millimeters. The unit is in feet. The unit is in feet. The unit is in feet. The unit is in feet.
- 002  All dimensions are in millimeters. All dimensions are in millimeters.
- 003  All dimensions are in millimeters. All dimensions are in millimeters.
- 004  All dimensions are in millimeters. All dimensions are in millimeters.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL	REFERENCE
	+/- 10% Tolerance	
TRACE WIDTH		
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR-4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR-4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR-4	39.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR-4	4.00mil	4	
5	LL_Pwr	Copper	1.83mil		
	Dielectric 5	FR-4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBERS.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/4958N AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE FOLLOWED IS +/-0.0025(0.10") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER  Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENIG

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 2  1  2  3  RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**BARE BOARD ELEC. TEST:**  NONE  REQUIRED  PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ENGINEER: Garrett Godfrey LAYOUT BY: Tessadve

ALTRUM DESIGNER VERSION: 23.1.1.15

SCALE: 0.72

ALL-ARTWORK VIEWED FROM TOP SIDE: <input type="checkbox"/>	BOARD #: Robotics Design	REV#: A	DATE: 6/28/2025	TIME: 10:16:34 AM	DESIGNER: GARRETT GODFREY	DATE: 6/28/2025	TIME: 10:16:34 AM	FILE: Robotics_Design.PcbDoc
LAYER NAME =	IPC #:	DATE:	TIME:	FILE:	DATE:	TIME:	FILE:	
PLOT NAME = M10-646-Notes	GENERATED: 6/28/2025	DATE:	TIME:	FILE:	DATE:	TIME:	FILE:	

- 001  Drill used to fabricate non-plated holes. The drill bit is 2.0mm. The hole is per the Lead Table in the BOM information.
- 002  Drill used to fabricate plated through holes. The drill bit is 2.0mm. The hole is per the Lead Table in the BOM information.
- 003  Drill used to fabricate through holes. The drill bit is 2.0mm. The hole is per the Lead Table in the BOM information.
- 004  Drill used to fabricate through holes. The drill bit is 2.0mm. The hole is per the Lead Table in the BOM information.
- 005  Drill used to fabricate through holes. The drill bit is 2.0mm. The hole is per the Lead Table in the BOM information.

IMPEDANCE TABLE:

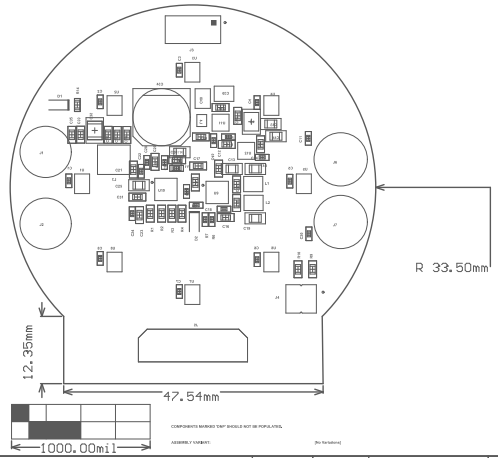
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:			60.00mil		+/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE FOLLOWED IS +/-0.0025(0.10") ON TOP SIDES. MINIMUM ANNUAL RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENIG

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 2  1  2  3  RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL RIGHTS RESERVED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	DATE/REV:	06/16/2024	DESIGNED BY:	Garret Godfrey	DESIGNED FOR:	TI Internal
LAYER NAME =	IPC-2753	IPC-2753	IPC-2753	IPC-2753	IPC-2753	IPC-2753	IPC-2753	IPC-2753	IPC-2753	IPC-2753
PLOT NAME =	Mkt/Gen/Inf/Information	GENERATED :	06/20/2025	06/16/2024	06/16/2024	06/16/2024	06/16/2024	06/16/2024	06/16/2024	06/16/2024

- 001  Drill used to determine via hole sizes. The drill bit is 2.5mm. The hole size per the Lot# 1 table in the DRG indicates.
- 002  Laser assisted in 400 micron 400 micron hole size.
- 003  Laser assisted in 400 micron hole size for 400 micron hole size for 400 micron hole size.
- 004  Laser assisted in 400 micron hole size for 400 micron hole size for 400 micron hole size.

IMPEDANCE TABLE:

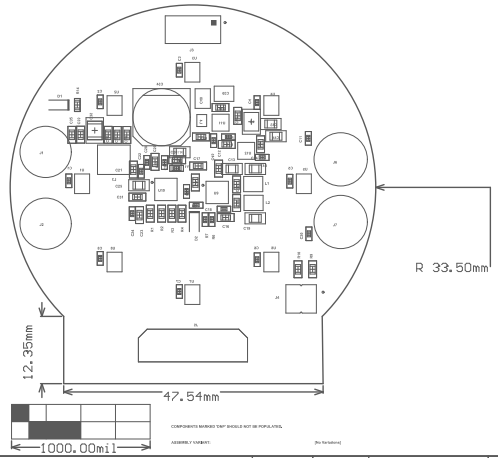
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR-4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR-4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR-4	39.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR-4	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	FR-4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.00mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS: 0.000-0.001" ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER \_\_\_\_\_

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER Refer stack up

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_

SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERPIS  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

ARRAY/PANEL:  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCB'S  
 TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS 2  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



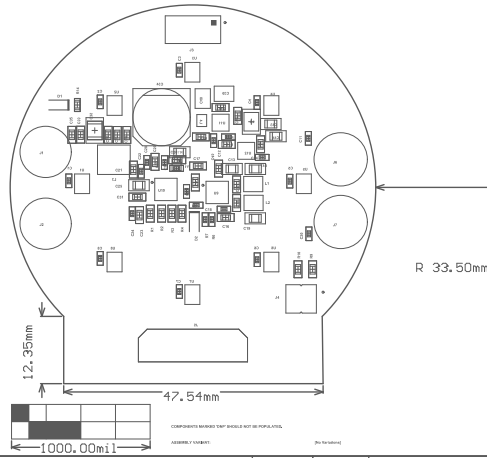
PRODUCT TITLE:  
Robotics Design

DESIGNED FOR:  
TI Internal

FILE NAME:  
Robotics\_Design.PcbDoc

ALL-ARTWORK VIEWED FROM TOP SIDE: <input type="checkbox"/>	BOARD #: Robotics Design	REV: A	DATE: 6/28/2025	TIME: 08:16:37 AM	DESIGNER: Garret Godfrey	DATE: 6/28/2025	TIME: 08:16:37 AM	FILE NAME: Robotics_Design.PcbDoc
LAYER NAME =	BOARD # =	REV =	DATE =	TIME =	DESIGNER =	DATE =	TIME =	FILE NAME =
PLOT NAME =	GENERATED =	DATE =	TIME =	FILE NAME =	SCALE =	0.72	23.1, 1.15	

- 001  All board and dimensions are in millimeters. The unit is in feet. The unit is in feet. The unit is in feet. The unit is in feet.
- 002  All dimensions are in millimeters. All dimensions are in millimeters.
- 003  All dimensions are in millimeters. All dimensions are in millimeters.
- 004  All dimensions are in millimeters. All dimensions are in millimeters.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL	REFERENCE
	+/- 10% Tolerance	
TRACE WIDTH		
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.00mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENCING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE FOLLOWED IS +/-0.0025(0.10") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS ARE WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENIG

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 2  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



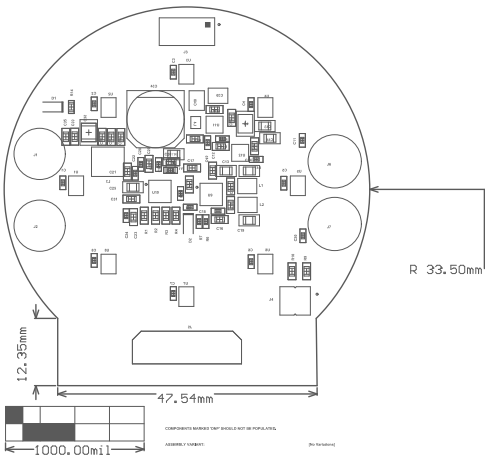
PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL RIGHTS RESERVED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	OWN REV:	MOLAS	DATE:	06/16/2025	DESIGNED BY:	Garret Godfrey	DESIGNED FOR:	TI Internal
LAYER NAME =	PCB #:	3DA-00054	REV:		OWN REV:		DATE:		DESIGNED BY:	Garret Godfrey	DESIGNED FOR:	TI Internal
PLOT NAME =	GENERATED:	06/20/2025	06:16:39 AM	TEKAS INSTRUMENTS					LAYOUT BY:	Tessadve	ALTRUM DESKMAN VERSION:	23.1.1.15

- 001  All board and dimensions are in millimeters. The unit is in feet. You need to use the Unit table in the PDP software.
- 002  All dimensions are in millimeters. All dimensions are in millimeters.
- 003  All dimensions are in millimeters. All dimensions are in millimeters.
- 004  All dimensions are in millimeters. All dimensions are in millimeters.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL	REFERENCE
	+/- 10% Tolerance	
TRACE WIDTH		
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				

Total board thickness: 68.20mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE FOLLOWED IS +/-0.0025" ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENIG

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  V. SCORE  
 N.C. ROUTE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 2  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design	DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc	ENGINEER: Garret Godfrey
LAYOUT BY: Tessadve	ALTRUM DESIGNER VERSION: 23.1.1.15
SCALE: 0.72	

ALL PARTS WORK VIEWED FROM TOP SIDE	BOARD #: Robotics Design	REV: A	DATE: 6/28/2025	TIME: 10:16:40 AM	DESIGNER: Garret Godfrey	DATE: 6/28/2025	TIME: 10:16:40 AM	COMPANY: TEXAS INSTRUMENTS
LAYER NAME =	BOARD # =	REV =	DATE =	TIME =	DESIGNER =	DATE =	TIME =	COMPANY =
PLOT NAME =	GENERATED =	DATE =	TIME =	COMPANY =				

- 001  Drill used to determine via hole sizes. The drill bit is 2.5mm. The hole size per the Lot# 1 table in the POP notebook.
- 002  Trace accuracy on 400 um pitch. 400 um resolution used for tolerances.
- 003  Trace accuracy on 200 um pitch. 200 um resolution used for tolerances.
- 004  Trace accuracy on 100 um pitch. 100 um resolution used for tolerances.
- 005  Trace accuracy on 50 um pitch. 50 um resolution used for tolerances.

IMPEDANCE TABLE:

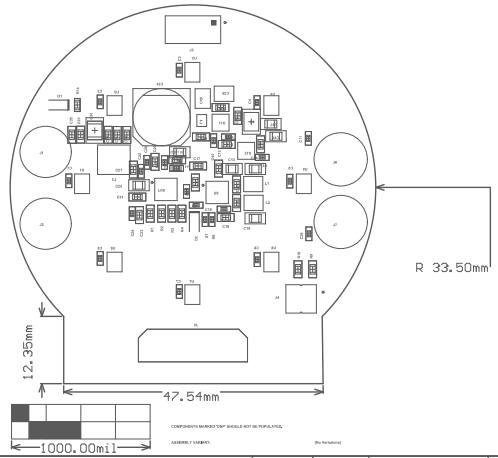
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR4	4.00mil	4	
3	LL_SIGNAL	Copper	1.83mil		
	Dielectric 3	FR4	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR4	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	FR4	4.00mil	4	
6	LL_SOLDER	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.20mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS +/-0.001mm ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR4  FR-4 High Tg  OTHER  Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 2  1  2  3  RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES  NONE  REQUIRED  PER ORDER

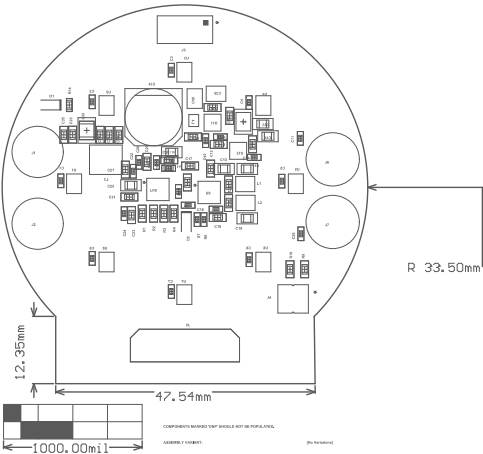
**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design  
 DESIGNED FOR: TI Internal  
 FILE NAME: Robotics\_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SWN REV:	MOLAS version control	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	BOARD #:	3DA-00054	REV:		GENERATED:	6/28/2025	6:16:42 AM
PLOT NAME =	GENERATED:	6/28/2025	6:16:42 AM	TEKAS INSTRUMENTS	SCALE:	0.72	LAYOUT BY: TessaDve ALTRUM DESKMAN VERSION: 23.1.1.15

- 001  Drill used to dimension via hole sizes. The drill bit is 2.5mm. The drill bit is used for the Lead Pad to the PCB substrate.
- 002  Drill used to dimension the 50 Ohm signal. The drill bit is 2.5mm. The drill bit is used for the Lead Pad to the PCB substrate.
- 003  Drill used to dimension the 50 Ohm signal. The drill bit is 2.5mm. The drill bit is used for the Lead Pad to the PCB substrate.
- 004  Drill used to dimension the 50 Ohm signal. The drill bit is 2.5mm. The drill bit is used for the Lead Pad to the PCB substrate.
- 005  Drill used to dimension the 50 Ohm signal. The drill bit is 2.5mm. The drill bit is used for the Lead Pad to the PCB substrate.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.20mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TUNED IN BOTH SIZES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TUNING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE DIMENSIONS ARE +/-0.0025" ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER \_\_\_\_\_

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER Refer stack up

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENIG  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs  
 TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS 3  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES  
**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER  
**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL VIDE, XX MIL SPACE  
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

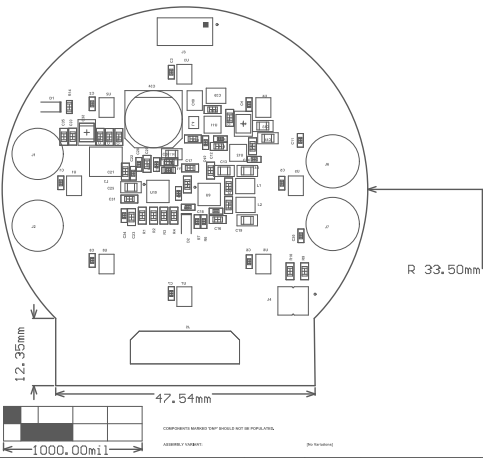
FILE NAME: Robotics\_Design.PcbDoc

ENGINEER: Garrett Godfrey LAYOUT BY: Tessadve

SCALE: 0.72 ALTRUM DESKMAN VERSION: 23.1.1.15

ALL RIGHTS RESERVED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SWN REV:	MoJas version control	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	BOARD #:	3DA-00054	REV:		GENERATED:	6/28/2026	6:16:43 AM
PLOT NAME =	GENERATED:	6/28/2026	6:16:43 AM	TEKAS INSTRUMENTS			

- 001  All board is fabricated on one half only. The other half is a mirror image of the first half.
- 002  All components are placed on the top side of the board.
- 003  All components are placed on the bottom side of the board.
- 004  All components are placed on both sides of the board.
- 005  All components are placed on the top side of the board.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				

Total board thickness: 68.20mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.51) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE FOLLOWED IS +/-0.0025(0.10") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENIG

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 2  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design	DESIGNED FOR: TI Internal	FILE NAME: Robotics_Design.PcbDoc
ENGINEER: Garret Godfrey	LAYOUT BY: Tessadve	ALTRUM DESIGNER VERSION: 23.1.1.15
SCALE: 0.72		

ALL RIGHTS RESERVED. VIEWED FROM TOP SIDE.	BOARD #: Robotics Design	REV: A	DATE: 06/28/2025	TIME: 08:16:45 AM	USER: TEKAS INSTRUMENTS	TEKAS INSTRUMENTS (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	BOARD # =	REV # =	DATE =	TIME =	USER =	
PLOT NAME =	GENERATED =	DATE =	TIME =	USER =		

- 001  Drill used is dimensioned on the Drill List. The drill bit is 2.0mm. The drill bit is used for the Lead Pad in the PCB.
- 002  The assembly is 400 microns. All dimensions are in millimeters.
- 003  The assembly is 400 microns. All dimensions are in millimeters.
- 004  The assembly is 400 microns. All dimensions are in millimeters.
- 005  The assembly is 400 microns. All dimensions are in millimeters.

IMPEDANCE TABLE:

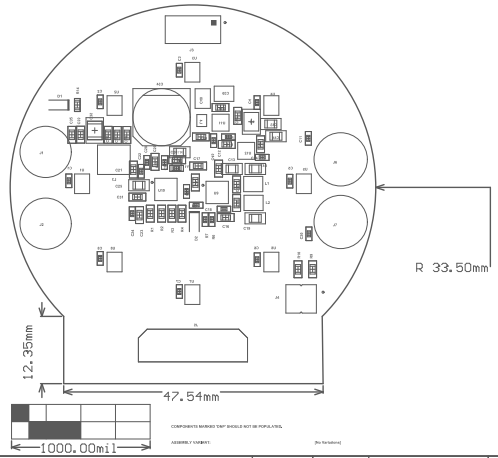
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.20mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TIENTED IN BOTH SIZES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TIENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE FOLLOWANCE IS +/-0.0025(0.10") ON TOP SIDES. MINIMUM ANNUAL RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER \_\_\_\_\_

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER Refer stack up

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_

SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERPIS  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

ARRAY/PANEL:  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs  
 TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS 1  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER  
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL VIDE, XX MIL SPACE  
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE:  
Robotics Design

DESIGNED FOR:  
TI Internal

FILE NAME:  
Robotics\_Design.PcbDoc

ALL RIGHTS RESERVED	REV: A	BOARD #:	Robotics Design	REV: A	DATE: 02/20/2025	TIME: 08:46 AM	DESIGNED BY: GARRET GODFREY	DESIGNED FOR: TI INTERNAL	FILE NAME: ROBOTICS_DESIGN.PCBDOC	ENGINEER: GARRET GODFREY	LAYOUT BY: TESSADVE
LAYER NAME =	DESIGNED BY =	DESIGNED FOR =	FILE NAME =	ENGINEER =	LAYOUT BY =	SCALE = 0.72					
PLOT NAME =	GENERATED =	DATE =	TIME =								

- 001  Drill used in fabrication was 100% fresh. The drill bit is 2.0mm. The drill bit was used for the Lead Holes in the PCB substrate.
- 002  The assembly was done in a clean room (ISO class 1000) and the solder was 100% fresh.
- 003  The assembly was done in a clean room (ISO class 1000) and the solder was 100% fresh. The assembly was done in a clean room (ISO class 1000).
- 004  The assembly was done in a clean room (ISO class 1000) and the solder was 100% fresh. The assembly was done in a clean room (ISO class 1000).

IMPEDANCE TABLE:

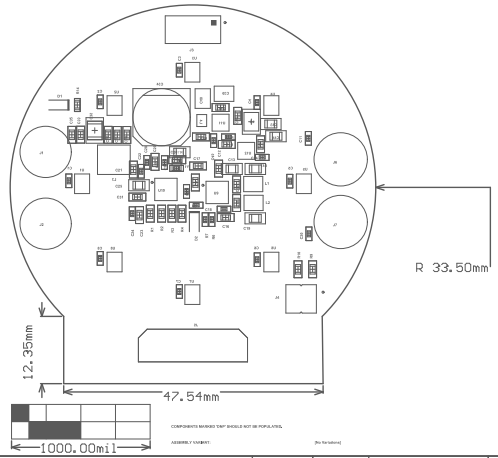
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:					60.00mil +/-10%

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE FOLLOWED IS +/-0.0025(0.10") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER \_\_\_\_\_

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER \_\_\_\_\_ Refer stack up

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_

SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERPIS  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs  
 TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS 3  1  2  3  
 RoHS  OTHER \_\_\_\_\_ PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  NONE  REQUIRED  PER ORDER  
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL RIGHTS RESERVED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SWN REV:	MoLab version control	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	BOARD #:	3DA-00054	REV:				
PLOT NAME =	GENERATED:	6/28/2025	08:16:48 AM			TEXASINSTRUMENTS	

- 001  Must meet 6-ohm maximum via hole impedance. This must be 2-ohm for Lead Pad on the PCB substrate.
- 002  Must meet 6-ohm maximum via hole impedance. This must be 2-ohm for Lead Pad on the PCB substrate.
- 003  Must meet 6-ohm maximum via hole impedance. This must be 2-ohm for Lead Pad on the PCB substrate.
- 004  Must meet 6-ohm maximum via hole impedance. This must be 2-ohm for Lead Pad on the PCB substrate.
- 005  Must meet 6-ohm maximum via hole impedance. This must be 2-ohm for Lead Pad on the PCB substrate.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

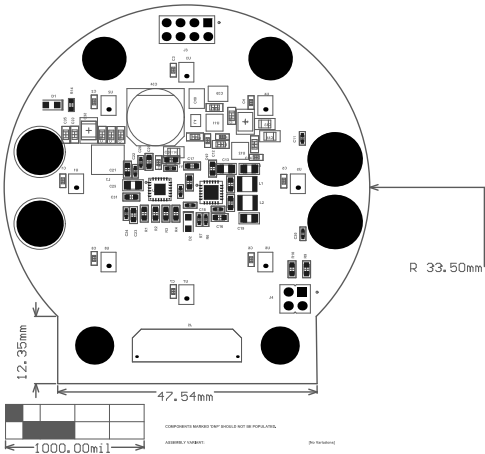
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	Fiberglass	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1. THIS IS IMPEDANCE CONTROLLED BOARD.
2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS: ±0.001±0.001" ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/-

**DRELLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENIG

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS 2  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

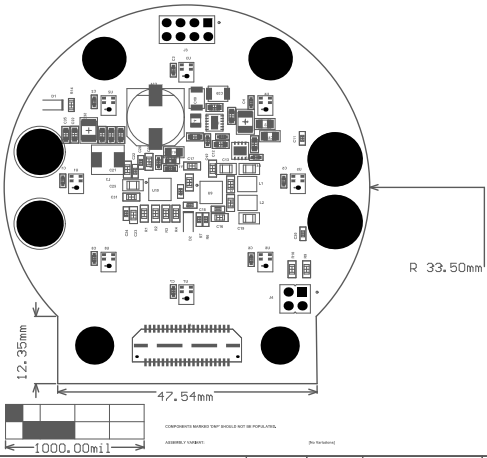
ENGINEER: Garrett Godfrey LAYOUT BY: Tessadve

ALTRUM DESIGNER VERSION: 23.1.1.15

SCALE: 0.72

ALL-REV WORK VIEWED FROM TOP SIDE: [REDACTED]	BOARD #: Robotics Design	REV#: A	SWM-REV: Molias version control	TEKAS INSTRUMENTS (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = [REDACTED]	3D #: 3DA-00054	GENERATED: 6/28/2025	6/16/24 AM	TEKAS INSTRUMENTS

- 001  Drill used & dimensions are per the files. The drill is 2.0mm. The drill is per the Lot# 1 file in the ZIP subfolder.
- 002  The assembly is in 400 umits. All dimensions are in 400 umits.
- 003  The assembly is in 400 umits. All dimensions are in 400 umits.
- 004  The assembly is in 400 umits. All dimensions are in 400 umits.
- 005  The assembly is in 400 umits. All dimensions are in 400 umits.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L3&4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25um	3.5	
1	LL_TOP	Copper	1.83um		
	Dielectric 1	Fiberglass	4.00um	4	
2	LL_GND1	Copper	1.83um		
	Dielectric 2	Fiberglass	4.00um	4	
3	LL_Signal	Copper	1.83um		
	Dielectric 3	Fiberglass	35.20um	4	
4	LL_GND2	Copper	1.83um		
	Dielectric 4	Fiberglass	4.00um	4	
5	LL_PWR	Copper	1.83um		
	Dielectric 5	Fiberglass	4.00um	4	
6	LL_Solder	Copper	1.83um		
	Bottom Solder	Solder Resist	1.25um	3.5	
	Bottom Overlay				
Total board thickness:					60.00um

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TUNED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TUNING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCES: 0.020mm (0.001") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENIG

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  V. SCORE  
 N.C. ROUTE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 2  1  2  3

RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**BARE BOARD ELEC. TEST:**  NONE  REQUIRED  PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL PARTS VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SWN.REV:	MoJas.walsh@ti.com	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	BOARD #:	3DA-00054	REV:		SWN.REV:		
PLOT NAME =	GENERATED:	6/28/2025	DATE:	06/18/25 AM	COMPANY:	TEXAS INSTRUMENTS	

- 001  Keep used to determine the final hole size. The drill bit is 2.5mm. The hole size is per the Lead Frame for the PCB substrate.
- 002  Keep according to the 400 um hole size.
- 003  Keep according to the 400 um hole size for the 400 um hole size.
- 004  Keep according to the 400 um hole size for the 400 um hole size.
- 005  Keep according to the 400 um hole size for the 400 um hole size.

IMPEDANCE TABLE:

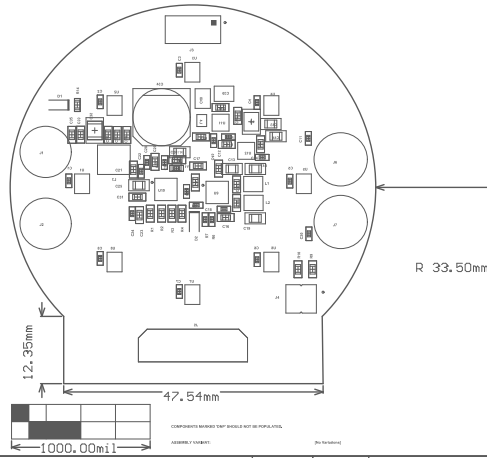
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25um	3.5	
1	LL_TOP	Copper	1.83um		
	Dielectric 1	FR-4	4.07mm	4	
2	LL_GND1	Copper	1.83um		
	Dielectric 2	FR-4	4.07mm	4	
3	LL_Signal	Copper	1.83um		
	Dielectric 3	FR-4	39.20um	4	
4	LL_GND2	Copper	1.83um		
	Dielectric 4	FR-4	4.07mm	4	
5	LL_PWR	Copper	1.83um		
	Dielectric 5	FR-4	4.07mm	4	
6	LL_Solder	Copper	1.83um		
	Bottom Solder	Solder Resist	1.25um	3.5	
	Bottom Overlay				
Total board thickness:					60.20um

FAB NOTES

- 1. THIS IS IMPEDANCE CONTROLLED BOARD.
- 2. ALL VIAS ARE TENTED IN BOTH SIDES UNLESS OTHERWISE MASK OPENED IN GERBER.
- 3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
- 4. 0.75mm VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. TOLERANCE IS +/-0.0025mm ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER \_\_\_\_\_

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER Refer stack up

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_

SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs  
 TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 3 >  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES

**MICROSECTION:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE:  
Robotics Design

DESIGNED FOR:  
TI Internal

FILE NAME:  
Robotics\_Design\_PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV:	A	SWM REV:	MoJas version control	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	SD #:	EDA-00054	DATE:	6/28/2025	06:18:03 AM	TEKAS INSTRUMENTS	ENGINEER: Garret Godfrey
PLOT NAME =	GENERATED:	6/28/2025	06:18:03 AM	TEKAS INSTRUMENTS	LAYOUT BY: Tessadve	ALTRUM DESKMAN VERSION: 23.1.1.15	SCALE: 0.72

DRILL TABLE

Symbol	Count	Hole Size	Plated	Hole Type
✕	13	7.87mil (0.200mm)	PTH	Round
▼	327	10.00mil (0.254mm)	PTH	Round
□	8	31.50mil (0.800mm)	NPTH	Round
⊗	2	39.37mil (1.000mm)	NPTH	Round
○	8	40.00mil (1.016mm)	PTH	Round
⊛	4	47.24mil (1.200mm)	PTH	Round
⊞	2	126.00mil (3.200mm)	PTH	Round
◇	2	129.92mil (3.300mm)	PTH	Round
■	2	144.00mil (3.658mm)	PTH	Round
▽	2	214.57mil (5.450mm)	PTH	Round
	270 Total			

FOR 7.87 MIL DRILL -10% TOL  
 FOR 10 MIL DRILL -10% TOL  
 FOR NPTH +/-2MIL  
 FOR PTH +/-3MIL

IMPEDANCE TABLE

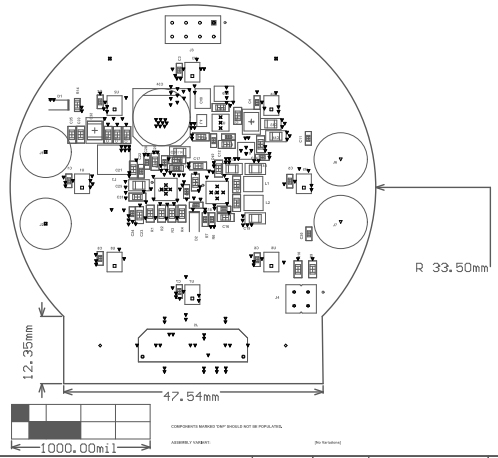
LAYERS	50 OHM SIGNAL	REFERENCE
	+/- 10% Tolerance	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.80mil		
	Dielectric 1	Fiberglass	4.00mil	4	
2	LL_GND1	Copper	1.80mil		
	Dielectric 2	Fiberglass	4.00mil	4	
3	LL_SIGNAL	Copper	1.80mil		
	Dielectric 3	Fiberglass	39.20mil	4	
4	LL_GND2	Copper	1.80mil		
	Dielectric 4	Fiberglass	4.00mil	4	
5	LL_PWR	Copper	1.80mil		
	Dielectric 5	Fiberglass	4.00mil	4	
6	LL_BOTTOM	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:			69.00mil		+/-10%

FAB NOTES

- THIS IS IMPEDANCE CONTROLLED BOARD.
- ALL LAMINATE ARE TIGHT IN BOTH SIZES UNLESS OTHERWISE MASK OPENED IN GERBER.
- VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT CAPABILITIES EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TIGHTENING / COVERING" REQUIREMENTS.
- 0.75MM VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLATING THICKNESS: 0.200-0.300" ON TOP SIDES. MINIMUM ANNUAL RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR-4  FR-4 High Tg  OTHER   
 THICKNESS: 62 MIL (1.6mm) +/-10%  OTHER  Refer stack up

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2   
 OTHER +/-

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2   
 OTHER +/-

**DRILLING:**

REFERENCE: AS SHOWN  NC\_DRILL FILES   
 PTH COPPER THICKNESS: 20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN: TOP  BOTTOM   
 SILKSCREEN COLOR: WHITE  OTHER   
 SOLDER RESIST COLOR: GREEN  OTHER   
 MATTE  SEMI-GLOSS

**SURFACE FINISH:** IMMERSION GOLD (ENIG)  ENIG   
 IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:** CUT AND TRIM PER M1 BOARD OUTLINE   
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS 3  RoHS  OTHER  PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:** YES   
 MICROSECTION: YES   
 BARE BOARD ELEC. TEST: NONE  REQUIRED  PER ORDER   
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE   
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE   
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE   
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design  
 DESIGNED FOR: TI Internal  
 FILE NAME: Robotics\_Design.PcbDoc

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LAYER NAME =	DRGNO =	3DA-00054	DATE	6/28/2025	08:16:54 AM	TEXAS INSTRUMENTS	ENGINEER: Garrett Godfrey LAYOUT BY: Tessadve ALTRUM DESKMAN VERSION: 23.1.1.15
PLQ.NAME =	DRGDATE =	6/28/2025	DATE	6/28/2025	08:16:54 AM	TEXAS INSTRUMENTS	SCALE: 0.72

- 001  Drill used to determine non-drill holes. The drill bit is 2.0mm. The hole is per the Lead Table in the POP notebook.
- 002  Hole locations are 400 microns. 400 microns (not in table).
- 003  Hole locations are 400 microns. 400 microns (not in table).
- 004  Hole locations are 400 microns. 400 microns (not in table).
- 005  Hole locations are 400 microns. 400 microns (not in table).

IMPEDANCE TABLE:

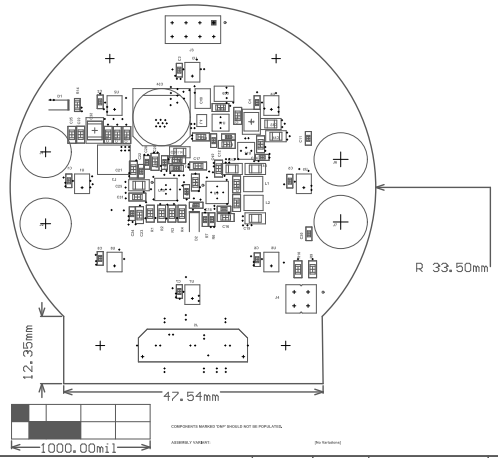
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	REFERENCE
	TRACE WIDTH	
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.25mil	3.5	
1	LL_TOP	Copper	1.83mil		
	Dielectric 1	FR4	4.00mil	4	
2	LL_GND1	Copper	1.83mil		
	Dielectric 2	FR4	4.00mil	4	
3	LL_Signal	Copper	1.83mil		
	Dielectric 3	FR4	35.20mil	4	
4	LL_GND2	Copper	1.83mil		
	Dielectric 4	FR4	4.00mil	4	
5	LL_PWR	Copper	1.83mil		
	Dielectric 5	FR4	4.00mil	4	
6	LL_Solder	Copper	1.83mil		
	Bottom Solder	Solder Resist	1.25mil	3.5	
	Bottom Overlay				
Total board thickness:			60.00mil		+/-10%

FAB NOTES

1. THIS IS IMPEDANCE CONTROLLED BOARD.
2. ALL VIAS ARE TENTED IN BOTH SIZES UNLESS OTHERWISE MASK OPENED IN GERBER.
3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1.5) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPERS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING / COVERING" REQUIREMENTS.
4. 0.075 MILS VIAS NEED TO BE FILLED WITH NON-CONDUCTIVE EPOXY/RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT. PLAINNESS TOLERANCE IS +/-0.0002(0.01") ON TOP SIDES. MINIMUM ANNUULAR RING REQUIREMENTS WAIVED FOR FILLED VIAS.



**DESIGN INFORMATION**

MIN. TRACK WIDTH: 5 MIL  
 MIN. CLEARANCE: 6 MIL  
 MIN. VIA PAD SIZE: 13.665 MIL

MINIMUM ANNUAL RING: 0.05mm (2MIL) EXTERNAL  
 PER IPC-A275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

FR4  FR-4 High Tg  OTHER Refer stack up

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  OTHER +/-

**DRILLING:**

REFERENCE:  AS SHOWN  NC\_DRILL FILES

PTH COPPER THICKNESS:  20-30 um  OTHER

**BOARD FINISH:**

SILKSCREEN:  TOP  BOTTOM

SILKSCREEN COLOR:  WHITE  OTHER

SOLDER RESIST COLOR:  GREEN  OTHER  MATTE  SEMI-GLOSS

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENERP

IMM. TIN/SILVER OR EQUIV  OTHER

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS 2  1  2  3  RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  YES  NONE  REQUIRED  PER ORDER

**BARE BOARD ELEC. TEST:**  XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  LAYER 2 & 3 (INNER LAYERS) XX MIL VIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PRODUCT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics\_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	Robotics Design	REV#:	A	DATE REV:	06/18/2025	DESIGNED BY:	Garret Godfrey	DESIGNED FOR:	TI Internal	FILE NAME:	Robotics_Design.PcbDoc
LAYER NAME =	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP	TOP
PLOT NAME =	DrillGuideDoc(LL_TOP + LL_Bottom)	GENERATED :	06/18/2025	08:16:56 AM	TEXAS INSTRUMENTS							

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Last updated 10/2025