PCB Number: 1
PCB Rev: A

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PCB
LOGO
WEEE logo

CAUTION HOT SURFACE

Repeat(Hardware,1,1)
Hardware&Ground.SchDoc

P_in
PowerIn.SchDoc

VIN_CONVERTER
IIN_SHUNT_NEG
IIN_SHUNT_POS

VIN_CONVERTER1
IIN_SHUNT_NEG1
IIN_SHUNT_POS1

Designator
(1) Tundra.SchDoc

VIN_CONVERTER1
IIN_SHUNT_NEG1
IIN_SHUNT_POS1

VIN_CONVERTER
IIN_SHUNT_NEG
IIN_SHUNT_POS

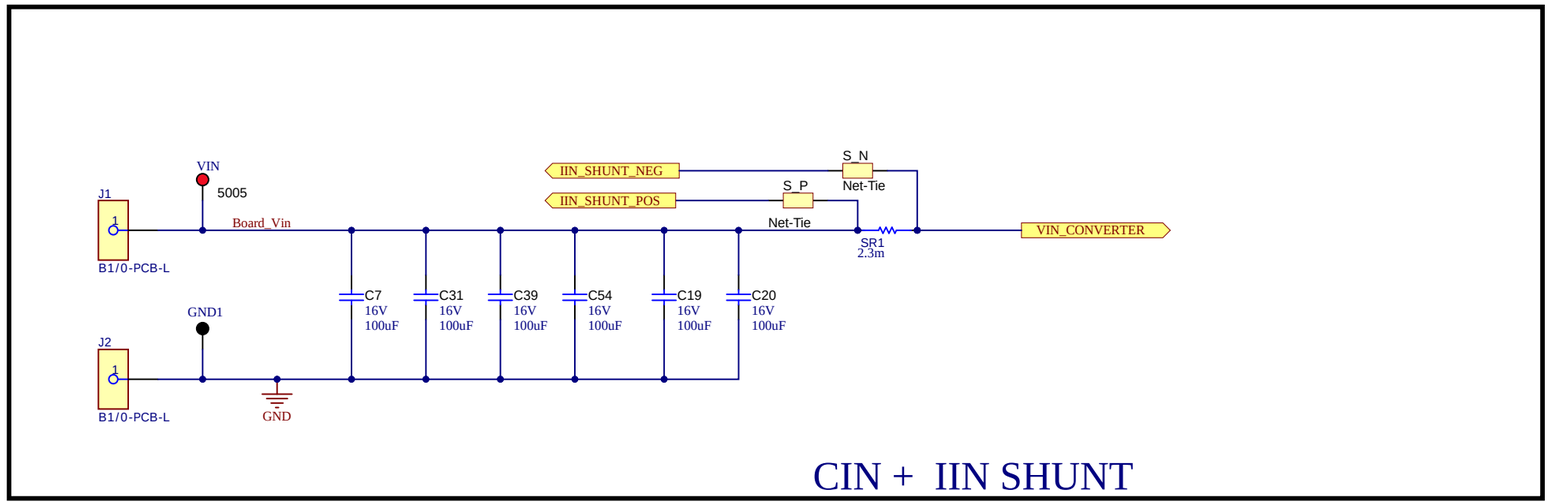
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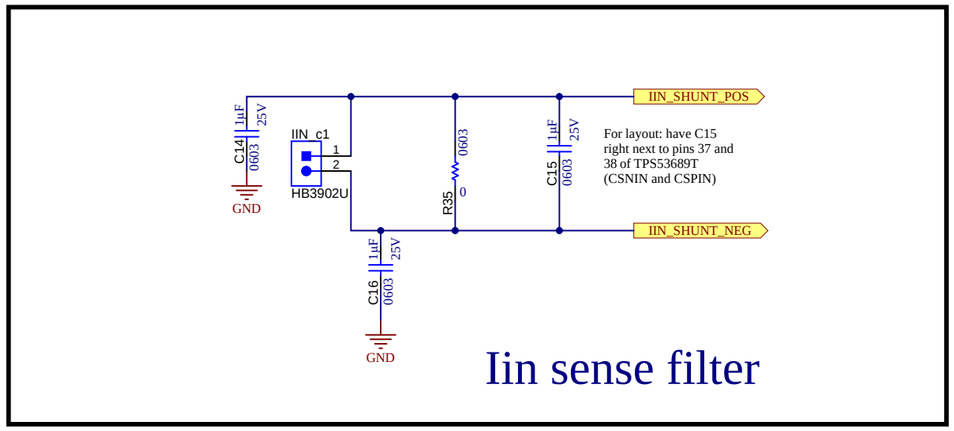
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TID #: TIDA011063		Project Title: FPGA Core Rail	
Number: 1	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: [No Variations]	Sheet: 1 of 6
Drawn By: Ryan Blake		File: CoverSheet_FPGA_Power_EVM.SchDoc	Size: B
Engineer: Ryan Blake		Contact: http://www.ti.com/support	

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CIN + IIN SHUNT



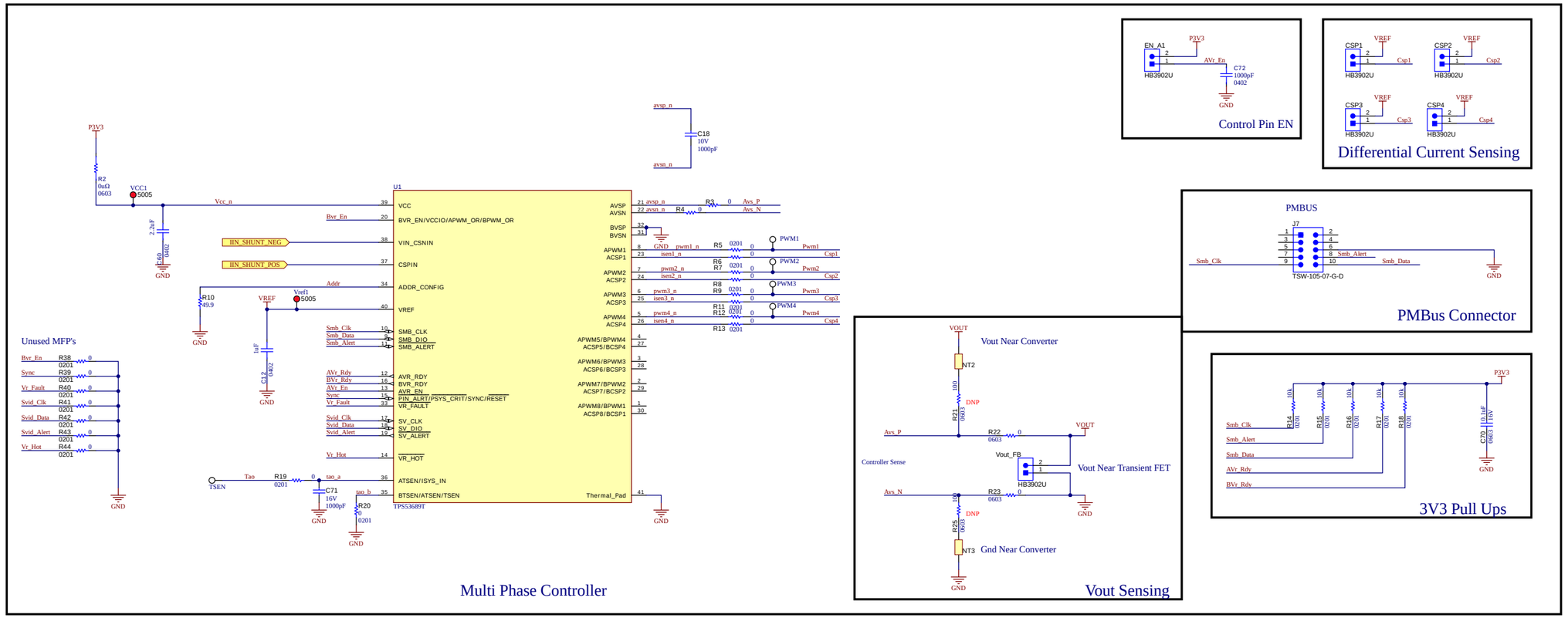
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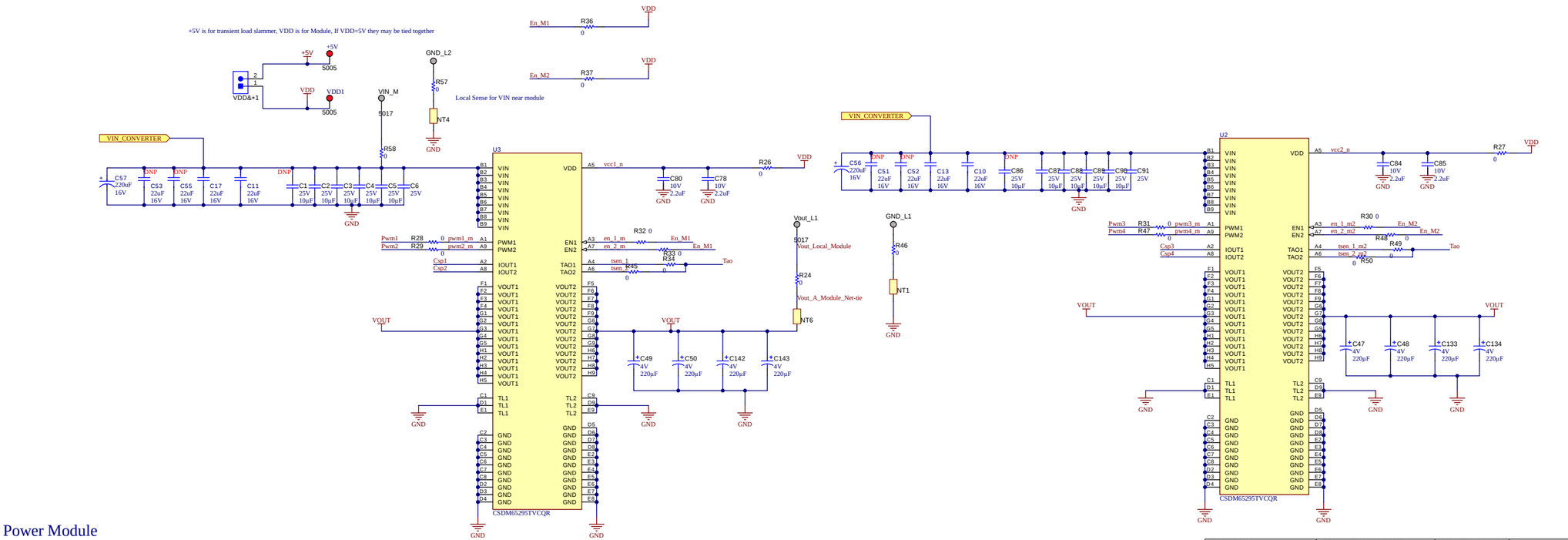
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Orderable: NA	Designed for: Public Release	Mod. Date: 6/22/2026
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Number: 1 Rev: A	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 2 of 6
Drawn By: Ryan Blake	File: PowerIn.SchDoc	Size: B
Engineer: Ryan Blake	Contact: http://www.ti.com/support	

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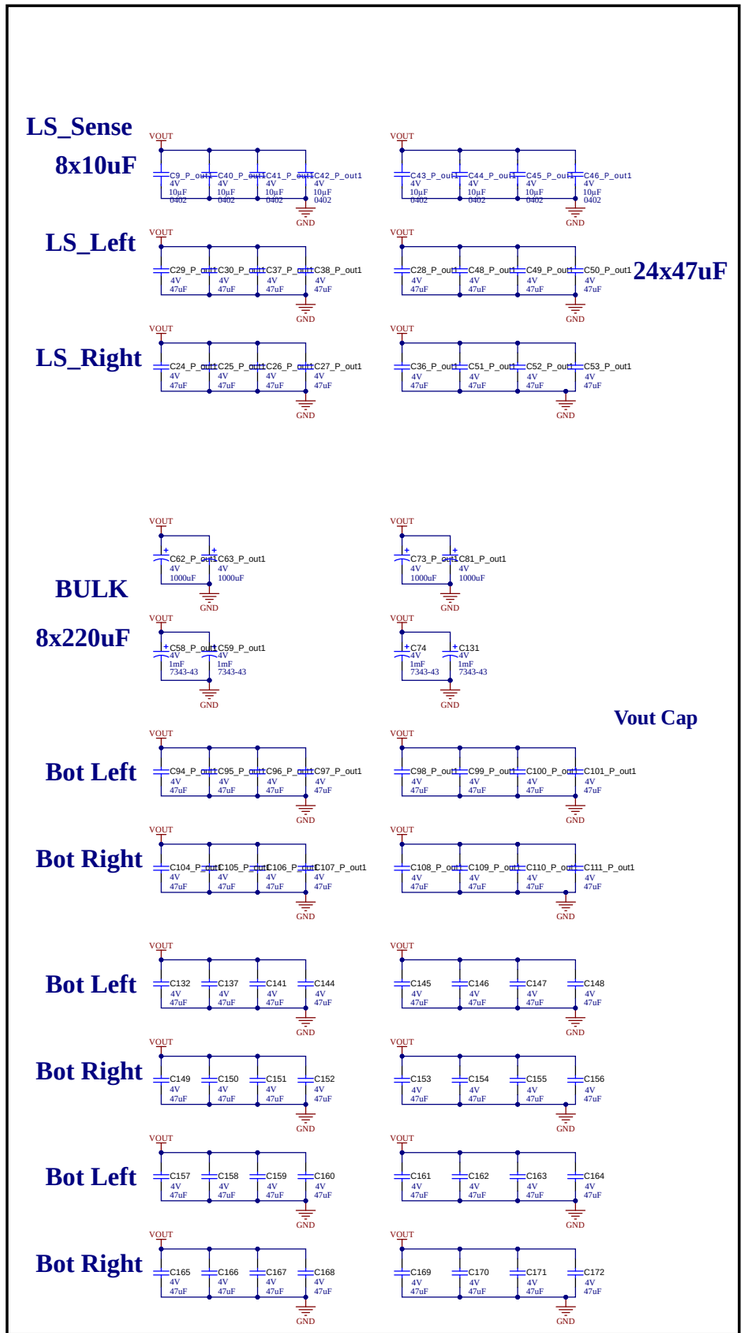


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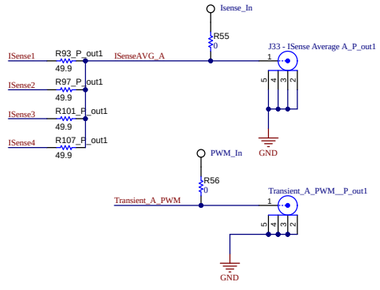
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Number: 1	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: [No Variations]	Sheet: 3 of 6
Drawn By: Ryan Blake		File: (1) Tundra.SchDoc	Size: C
Engineer: Ryan Blake		Contact: http://www.ti.com/support	

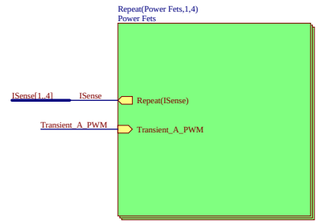
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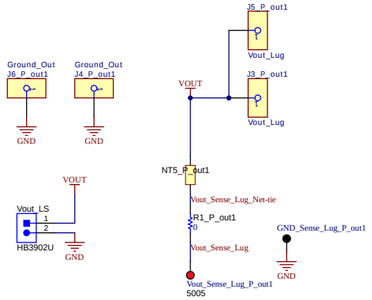
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Transient Circuit





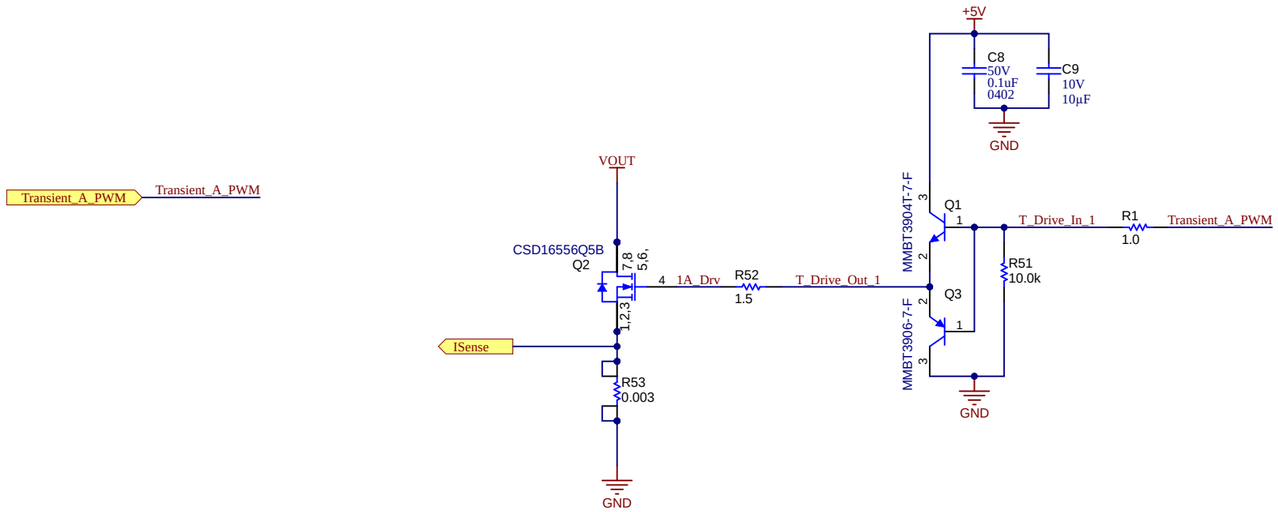


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Orderable: NA		Designed for: Public Release	Mod. Date: 8/25/2026
TID #: TIDA011063		Project Title: FPGA Core Rail	
Number: 1	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: [No Variations]	Sheet: 4 of 6
Drawn By: Ryan Blake		File: PowerOut.SchDoc	Size: C
Engineer: Ryan Blake		Contact: http://www.ti.com/support	

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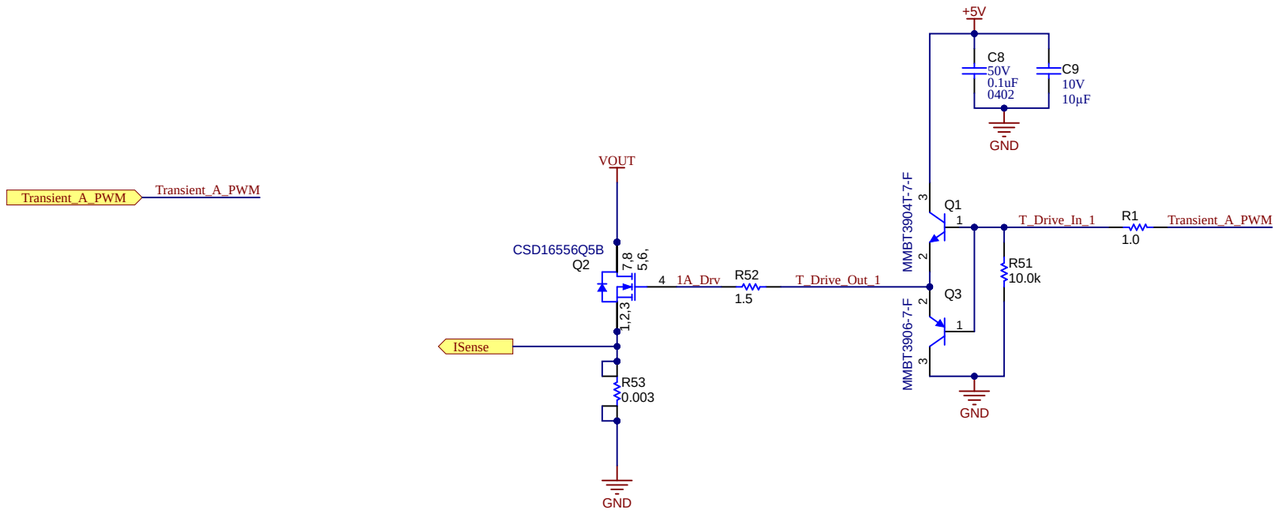


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Orderable: NA		Designed for: Public Release	Mod. Date: 8/24/2026
TID #: TIDA011063		Project Title: FPGA Core Rail	
Number: 1	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: [No Variations]	Sheet: 5 of 6
Drawn By: Ryan Blake		File: Power Fets.SchDoc	Size: B
Engineer: Ryan Blake		Contact: http://www.ti.com/support	

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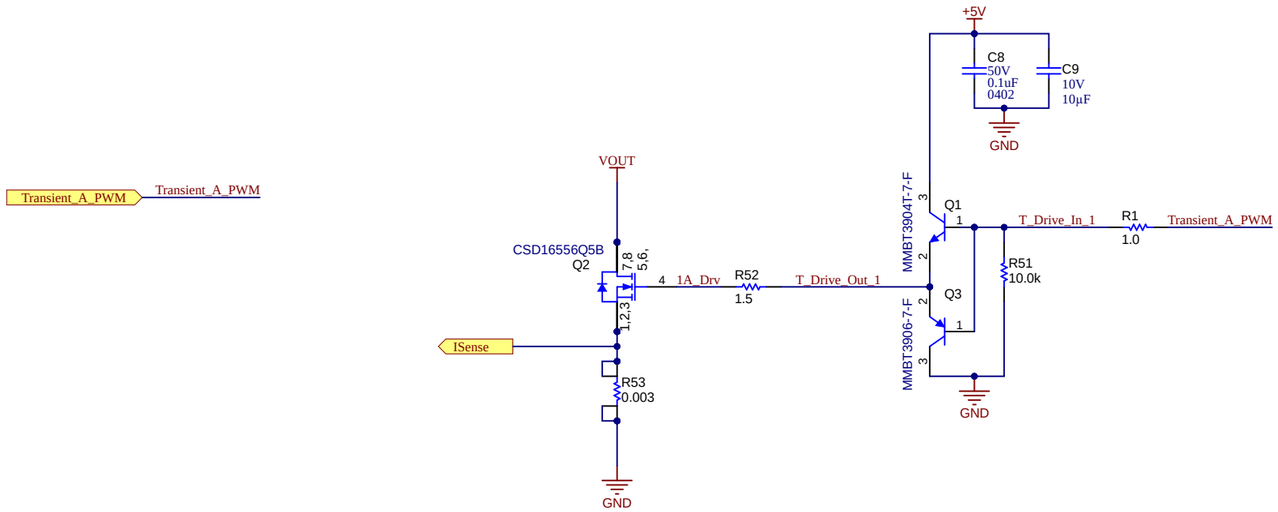


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Number: 1	Rev: A	Sheet Title:	
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Drawn By: Ryan Blake		File: Power Fets.SchDoc	Size: B
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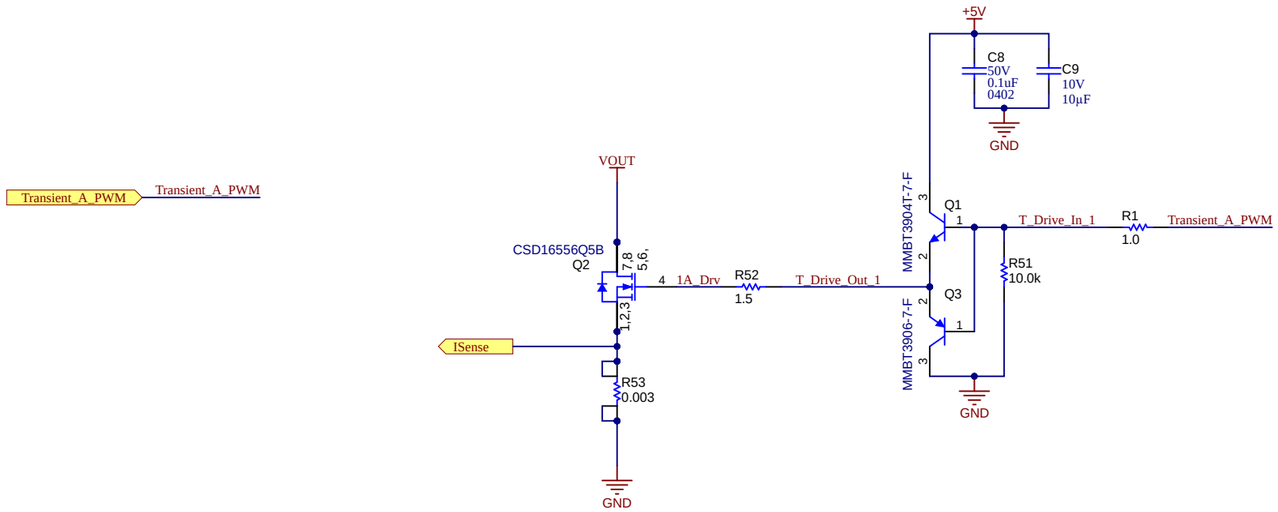


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Drawn By: Ryan Blake		File: Power Fets.SchDoc	Size: B
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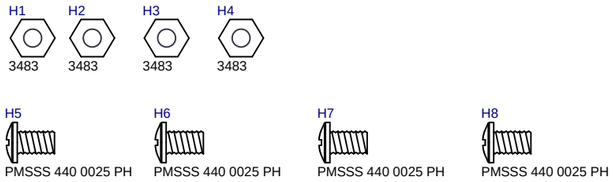


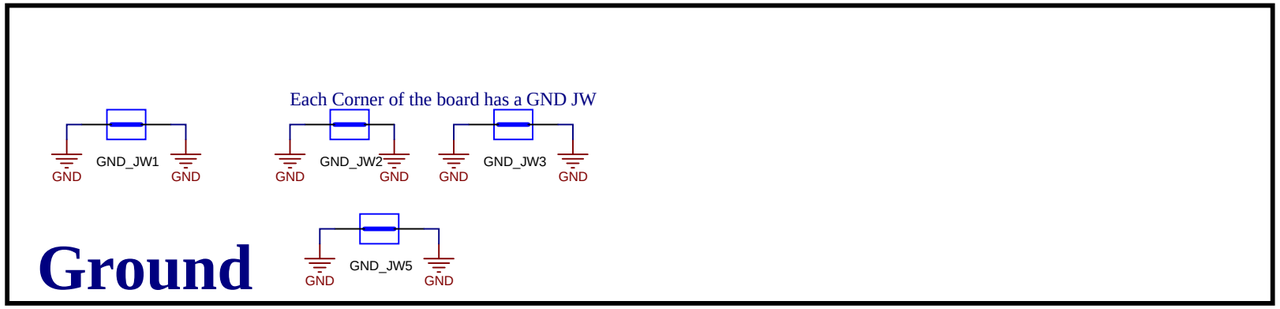
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Drawn By: Ryan Blake		File: Power Fets.SchDoc	Size: B
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Orderable: NA	Designed for: Public Release	Mod. Date: 5/23/2026
TID #: TIDA011063	Project Title: FPGA Core Rail	
Number: 1 Rev: A	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 6 of 6
Drawn By: Ryan Blake	File: Hardware&Ground.SchDoc	Size: B
Engineer: Ryan Blake	Contact: http://www.ti.com/support	

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