Test Report: PMP31007

Isolated 12-W DCM Flyback Reference Design

Description

This general purpose reference design uses the TPS40210 as controller. The isolated output voltage is 24 V with 0.5-A maximum output current. The input voltage range is from 18 V to 36 V – and used an off-the-shelf coupled inductor just providing functional isolation. Any 22-µH, 1:1 transformer can be used.

Features

- Functional isolation of 500 V is provided
- Cost-effective solution due to dual inductor from stock and dual-layer PCB
- The design is optimized for a small footprint

Applications

- Fire alarm control panel (FACP)

Top Board Photo

Bottom Board Photo

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	18 V to 36 V
Output Voltage	24 V
Output Current (max)	0.5 A
Isolation	Here: 500 V_{RMS} functional(1)

(1) Limited by dual inductor; Xcap allows up to 2 kV, optoisolator up to 3.75 kV

1.2 Considerations

Unless otherwise indicated, the resistor was used as load. The output current was adjusted to 0.5 A.

The circuit switches on at 20.8 V and off at 17.9 V. This individual circuit switches around 130 kHz (128 kHz on the reference board).

The converter itself works in DCM mode. This reference design has been optimized for low size, therefore a transformer with a small footprint was used. This small footprint results in higher heating in the inductor core. The higher temperatures can be reduced with a larger size transformer, for example, MSD-1578-223.

1.3 Dimensions

The outline of the board is 46 mm × 49.5 mm.

2 Testing and Results

2.1 Efficiency Graphs

Figure 2-1 shows the efficiency graph and Figure 2-2 shows the loss versus output current graph.

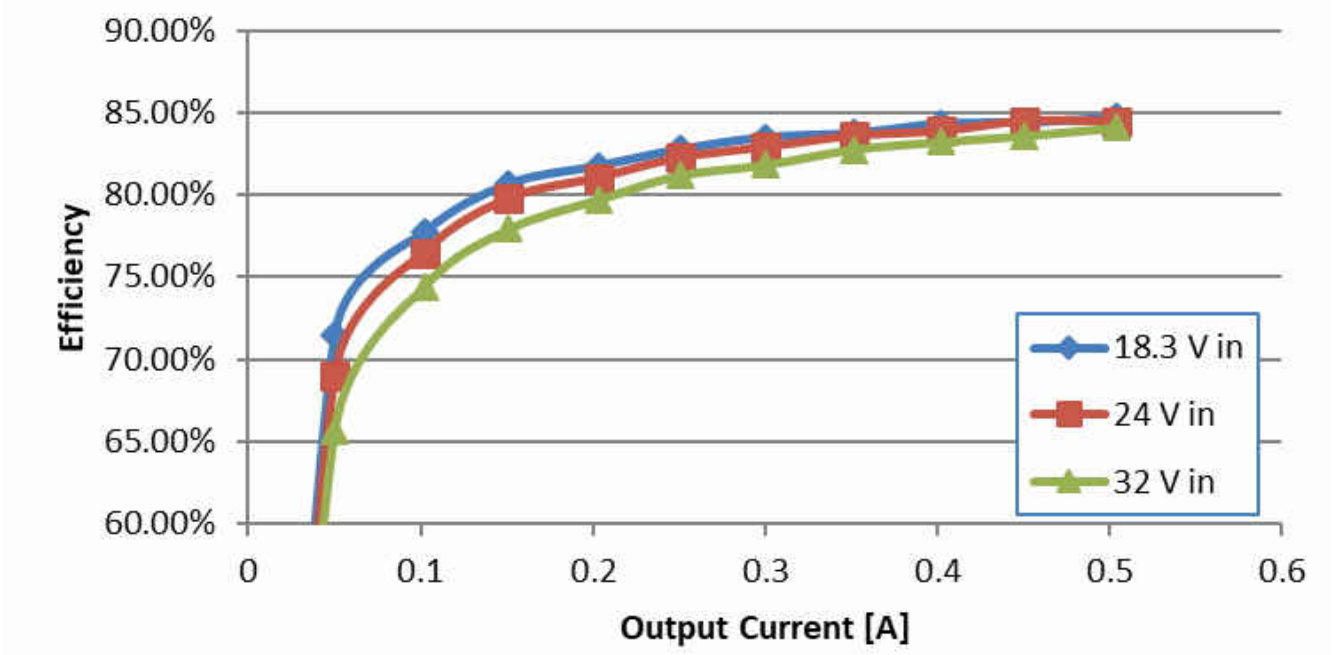


Figure 2-1. Efficiency vs Output Current

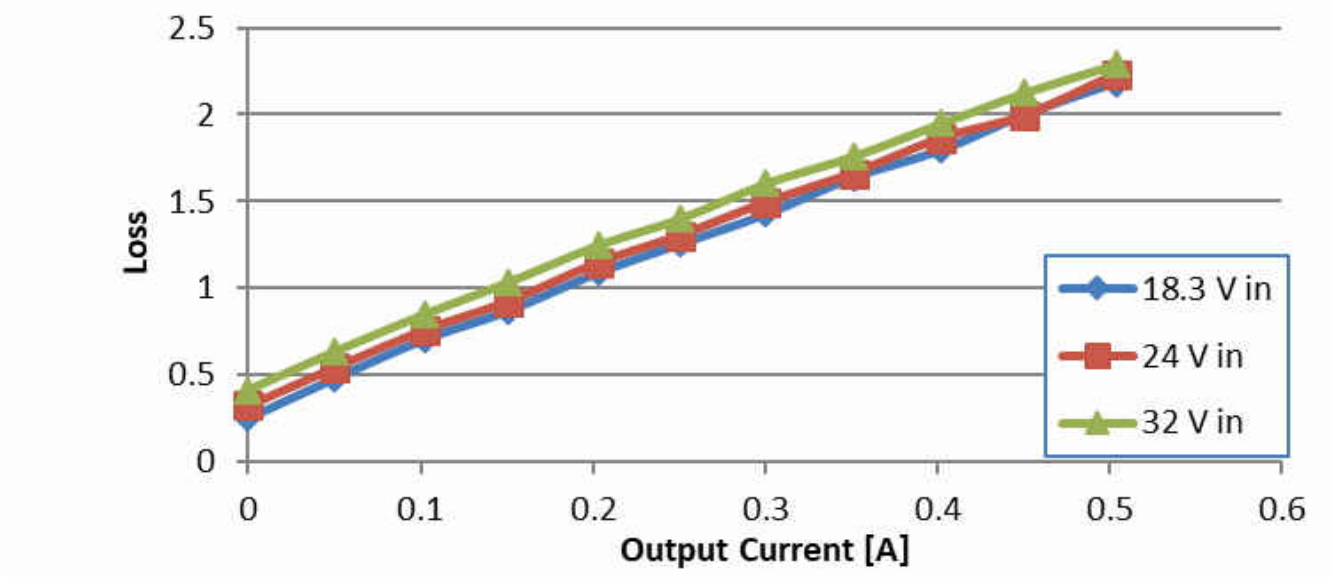


Figure 2-2. Loss vs Output Current

2.2 Load Regulation

Figure 2-3 shows the load regulation graph.

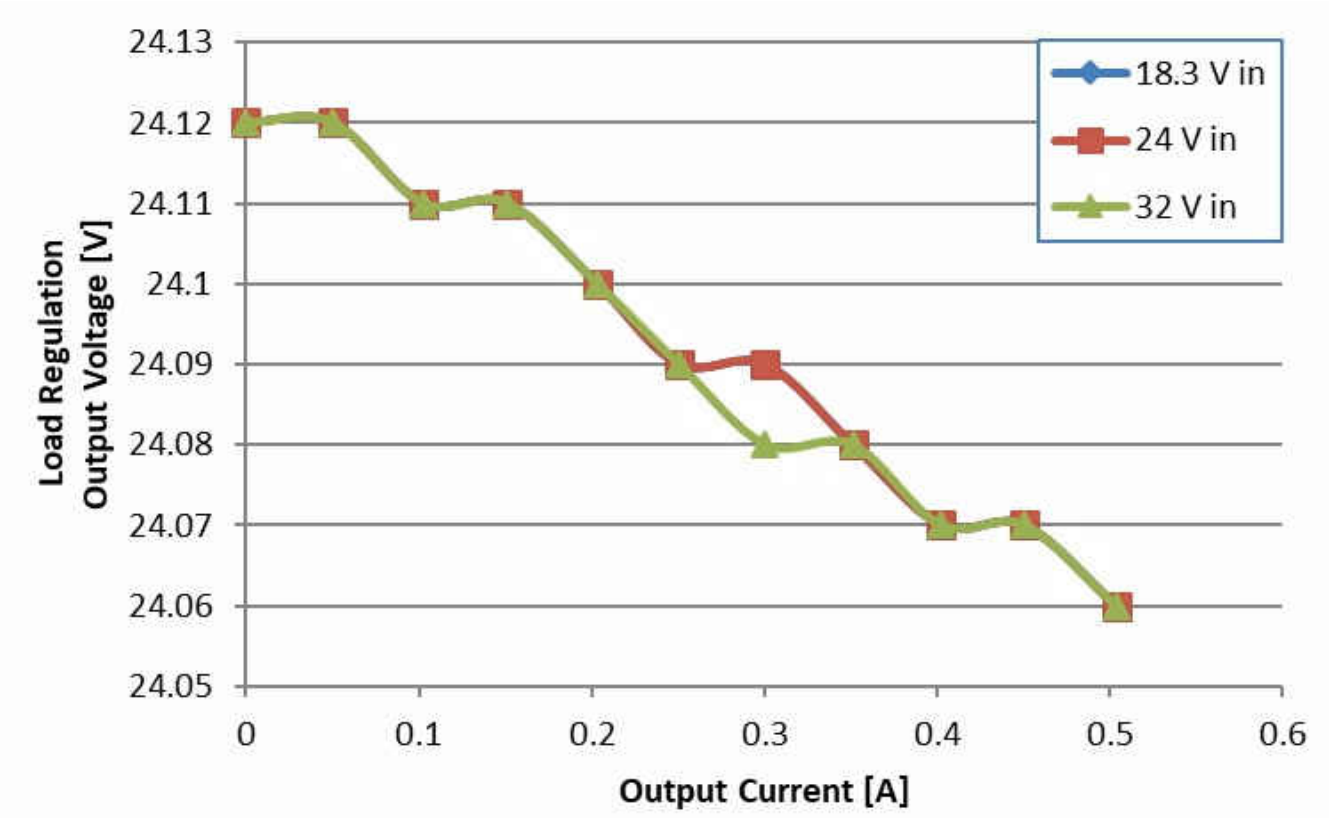


Figure 2-3. Load Regulation

2.3 Line Regulation

In the line regulation graph in Figure 2-4, the output current was adjusted to 0.5 A.

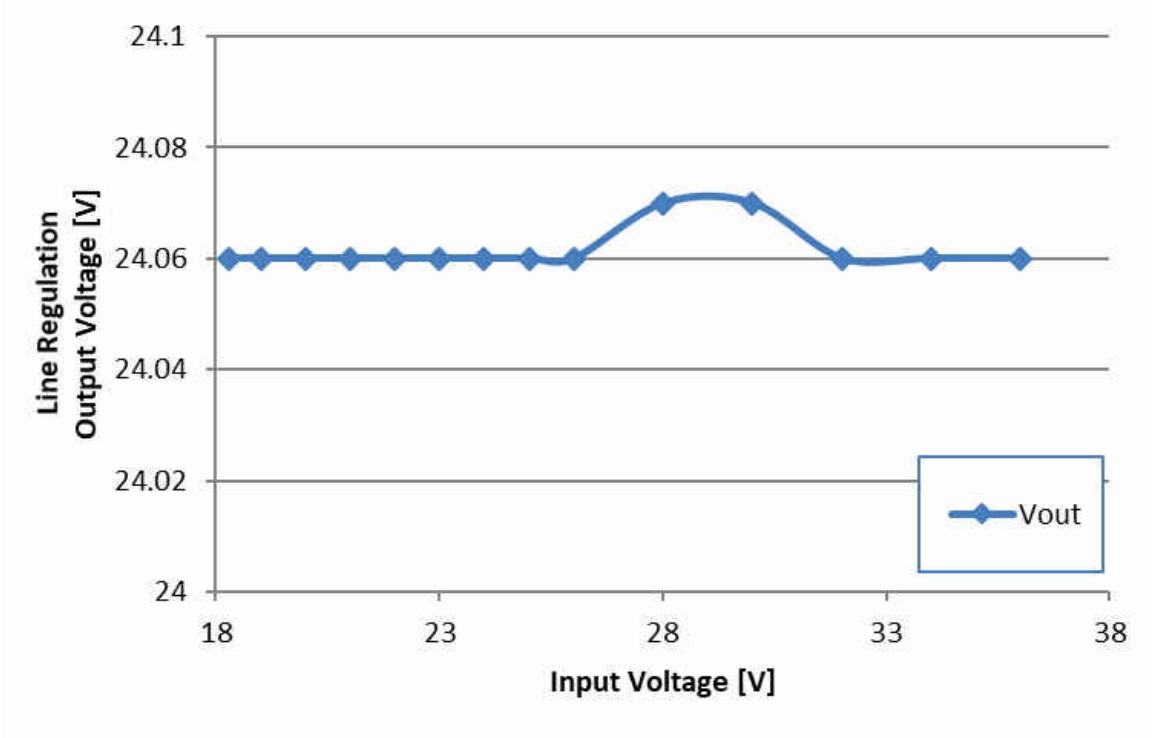


Figure 2-4. Line Regulation

With the same setup efficiency and loss were calculated as shown in Figure 2-5.

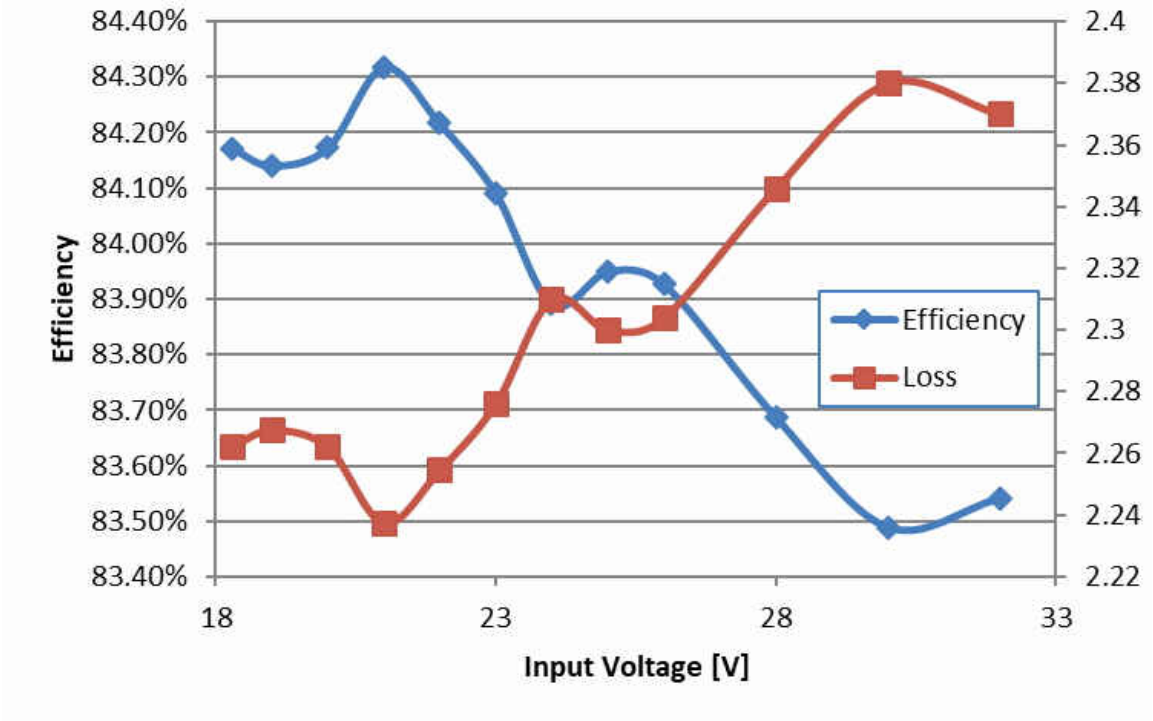


Figure 2-5. Efficiency and Loss vs Input Voltage

2.4 Thermal Images

In the following sections the thermal images with their hottest points are shown at different input voltages.

2.4.1 18-V Input Voltage and 500-mA Output Current

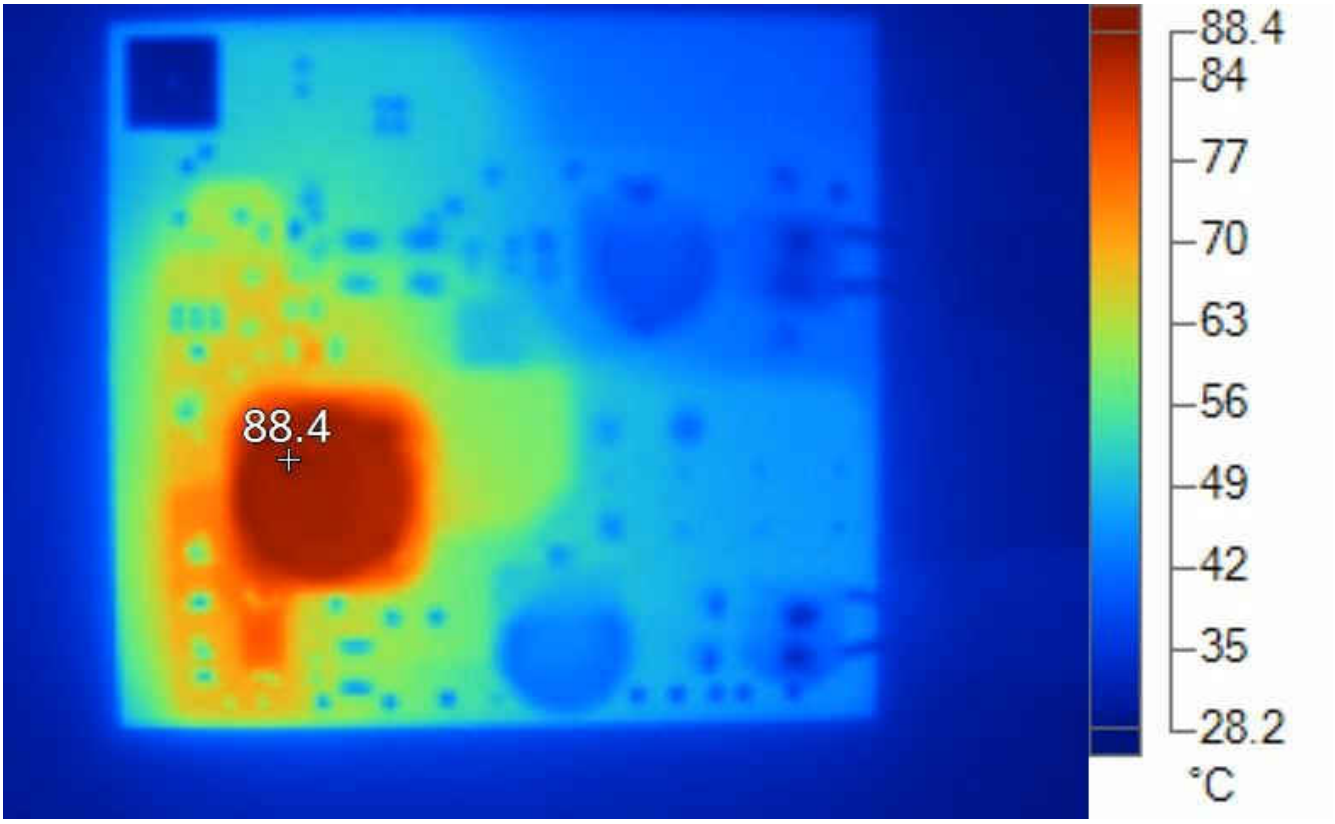


Figure 2-6. IR Photo for 18-V Input Voltage and 0.5-A Output Current

Name	Temperature
L1	88.4°C

2.4.2 24-V Input Voltage and 500-mA Output Current

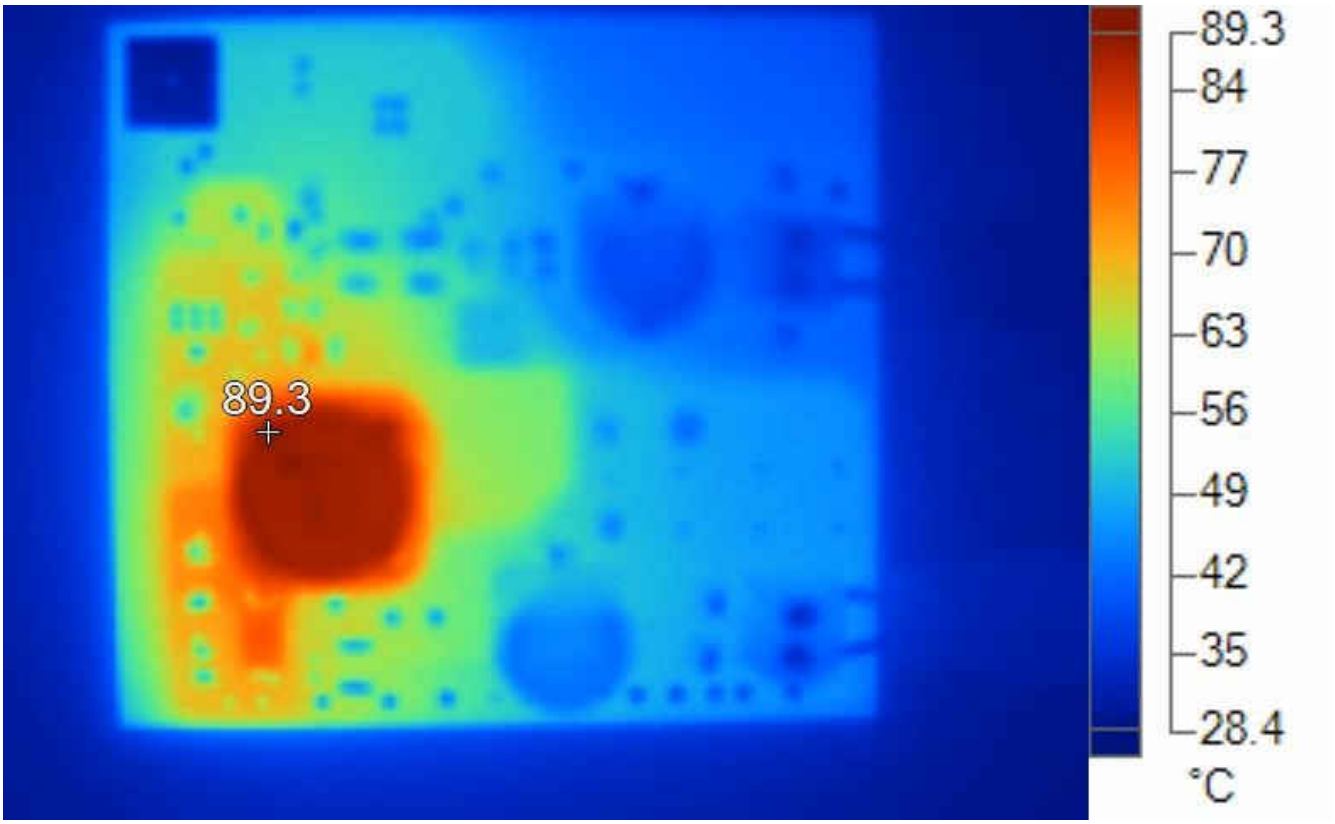


Figure 2-7. IR Photo for 24-V Input Voltage and 0.5-A Output Current

Name	Temperature
L1	89.3°C

2.4.3 36-V Input Voltage and 500-mA Output Current

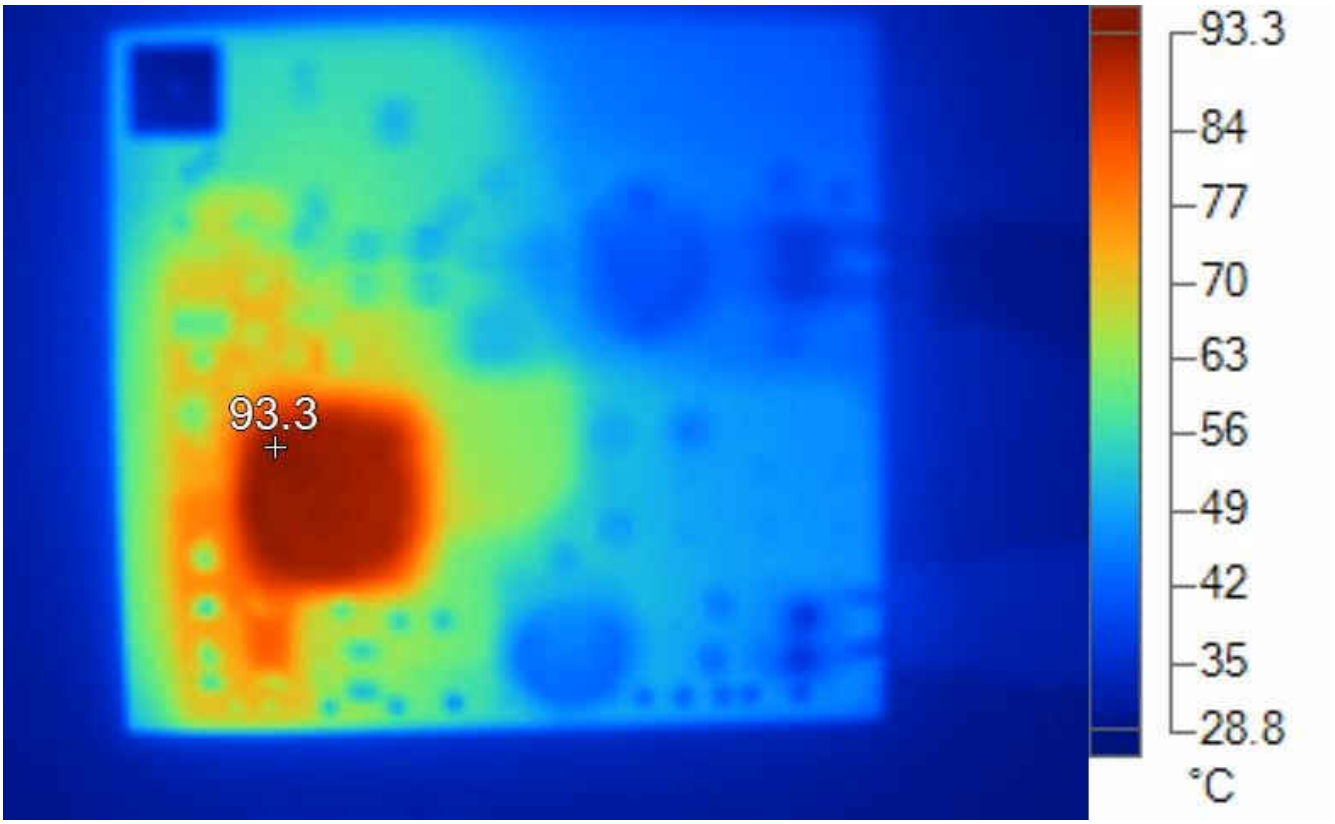


Figure 2-8. IR Photo for 36-V Input Voltage and 0.5-A Output Current

Name	Temperature
L1	93.3°C

2.5 Bode Plots

Table 2-1 summarizes the results from the bode plots.

Table 2-1. Summary of the Bode Plots

V_{IN}	18 V	24 V	32 V
Bandwidth (Hz)	3000	2500	2200
Phase Margin	80°	90°	80°
Slope (20 dB/decade)	-1.0	-1.0	-1.0
Gain Margin (dB)	18	16	20
Slope (20 dB/decade)	-1.0	-1.0	-1.0
Freq (kHz)	20	20	23

2.5.1 18-V Input Voltage

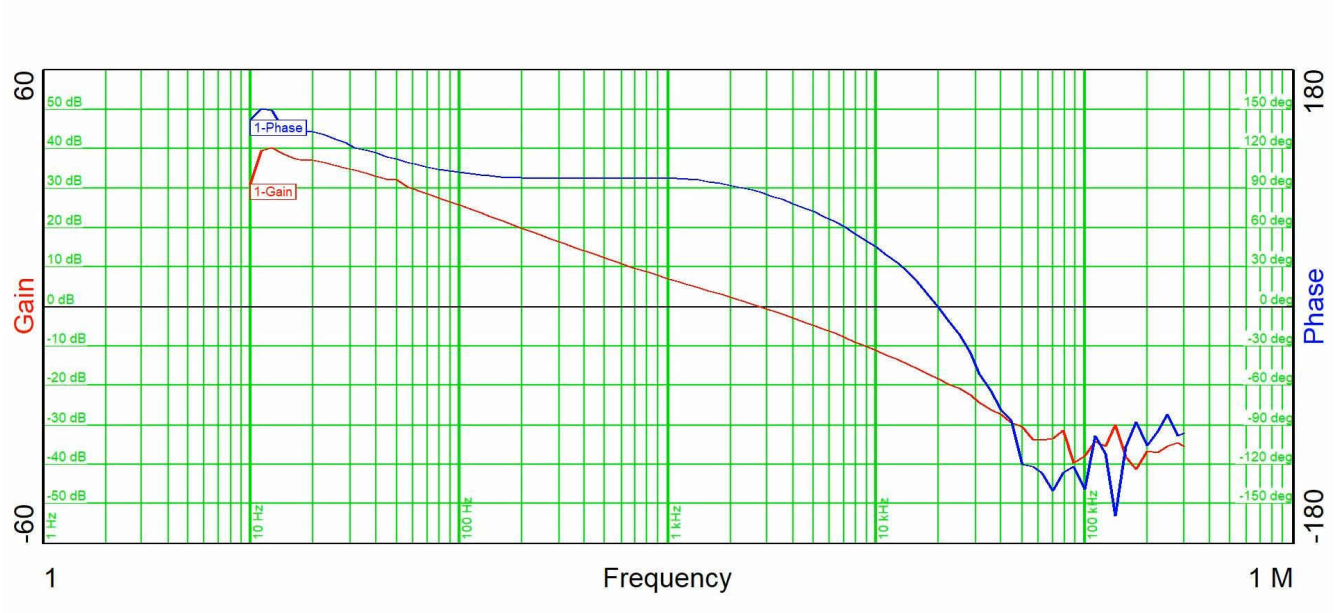


Figure 2-9. Bode Plot for 18-V Input Voltage

2.5.2 24-V Input Voltage

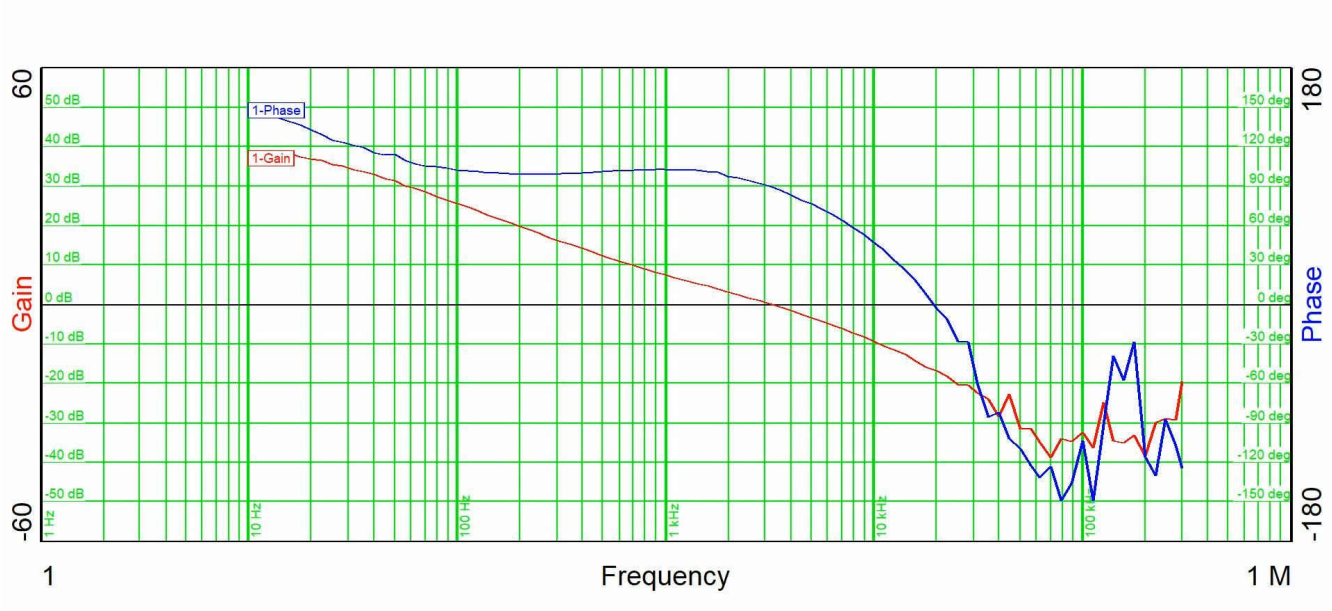


Figure 2-10. Bode Plot for 24-V Input Voltage

2.5.3 32-V Input Voltage

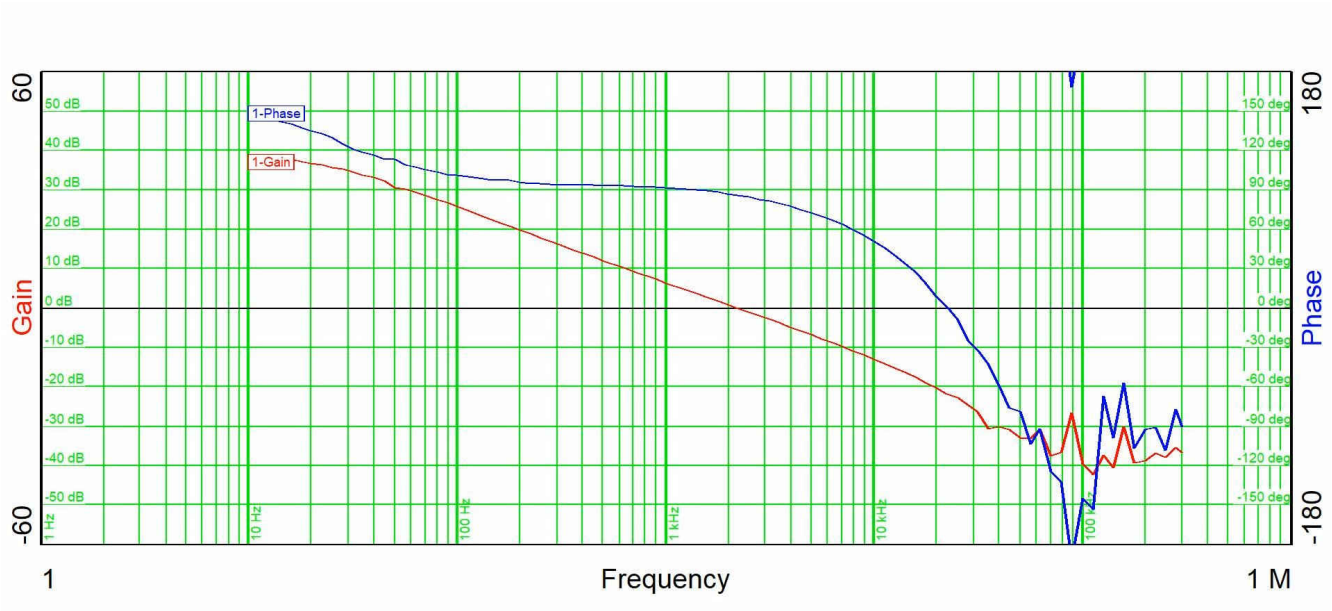


Figure 2-11. Bode Plot for 32-V Input Voltage

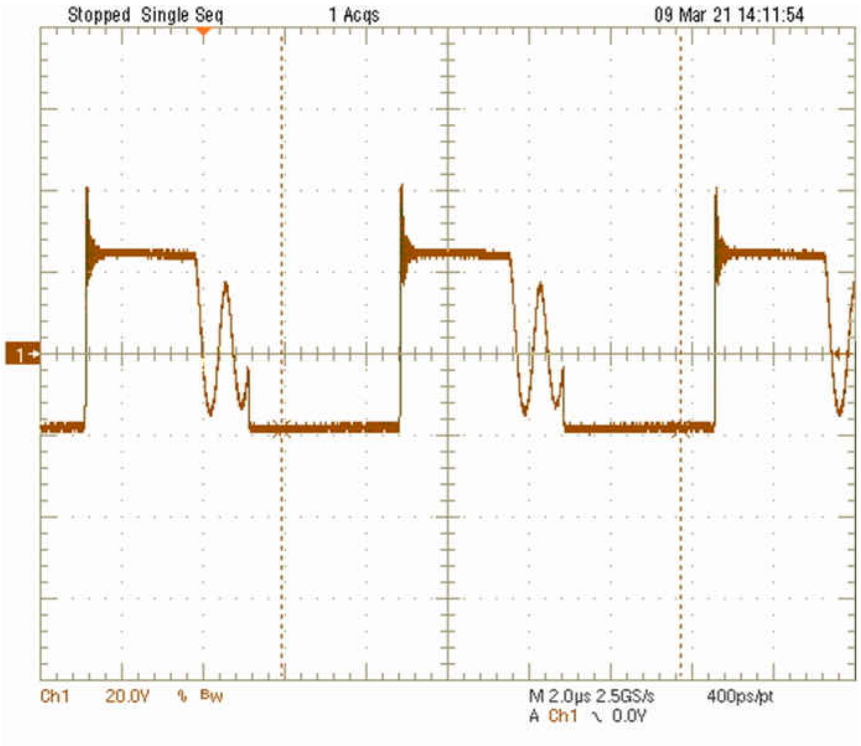
3 Waveforms

3.1 Switching

Switching behavior is shown in the following figures.

3.1.1 Transistor Q1 Drain-GND

3.1.1.1 18-V Input Voltage



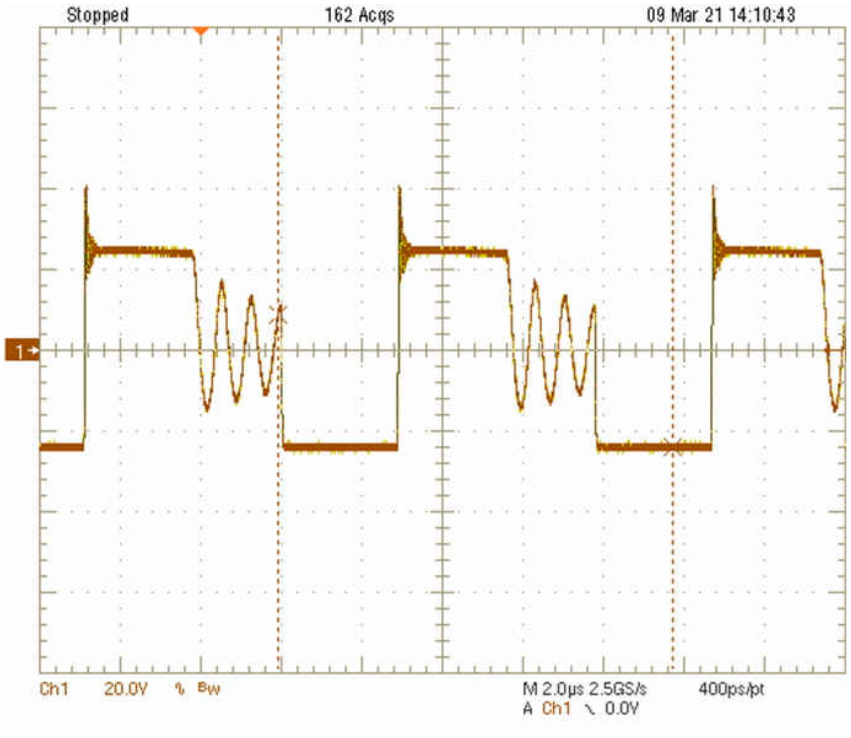
20 V / div

20-MHz bandwidth

2 µs / div

Figure 3-1. Switchnode Q1 at 18-V Input Voltage

3.1.1.2 24-V Input Voltage



20 V / div

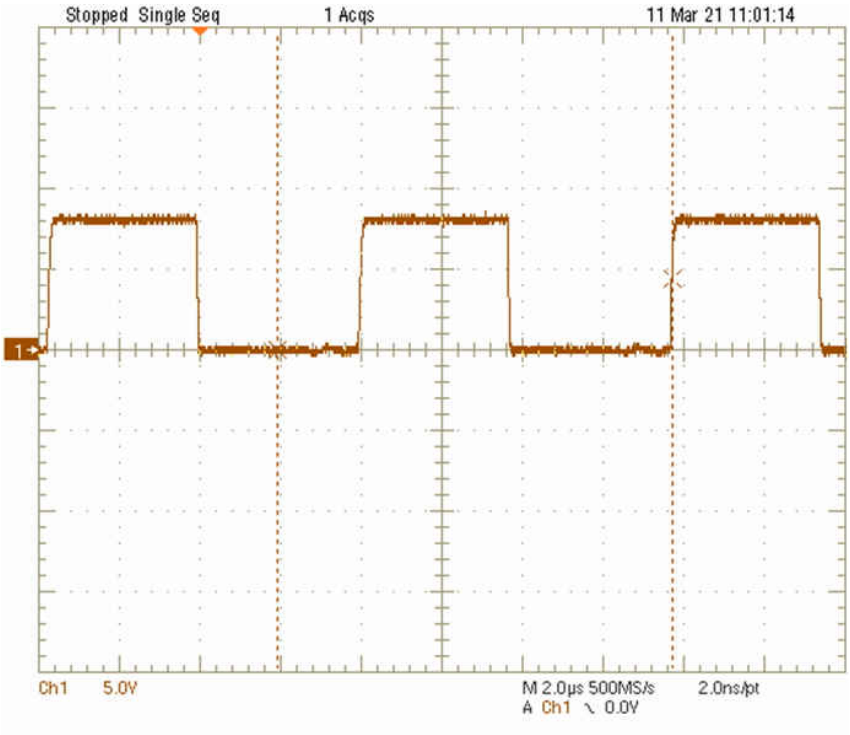
20-MHz bandwidth

2 µs / div

Figure 3-2. Switchnode Q1 at 24-V Input Voltage

3.1.2 Transistor Q1 Gate-Source

3.1.2.1 18-V Input Voltage



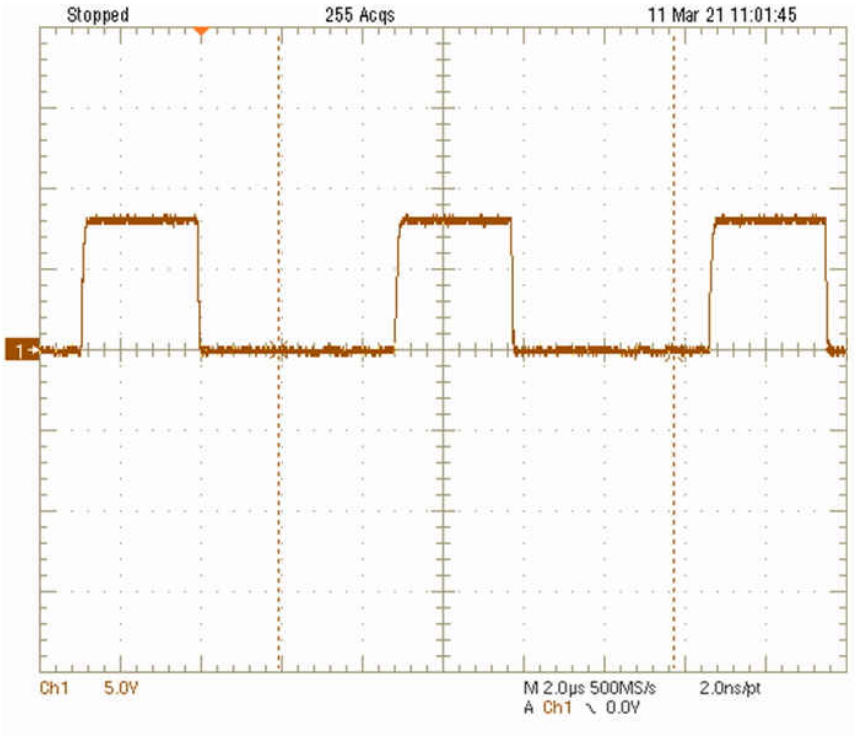
5 V / div

full bandwidth

2 µs / div

Figure 3-3. Q1 Gate at 18-V Input Voltage

3.1.2.2 24-V Input Voltage



5 V / div

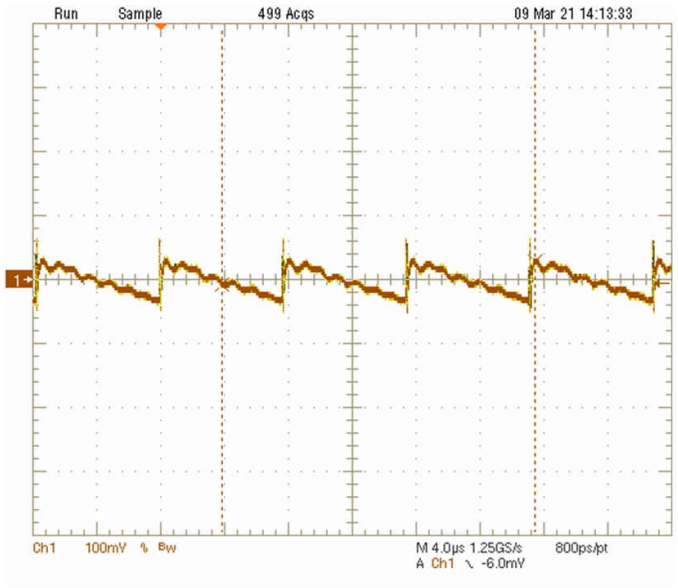
full bandwidth

2 µs / div

Figure 3-4. Q1 Gate at 24-V Input Voltage

3.2 Output Voltage Ripple

3.2.1 18-V Input Voltage

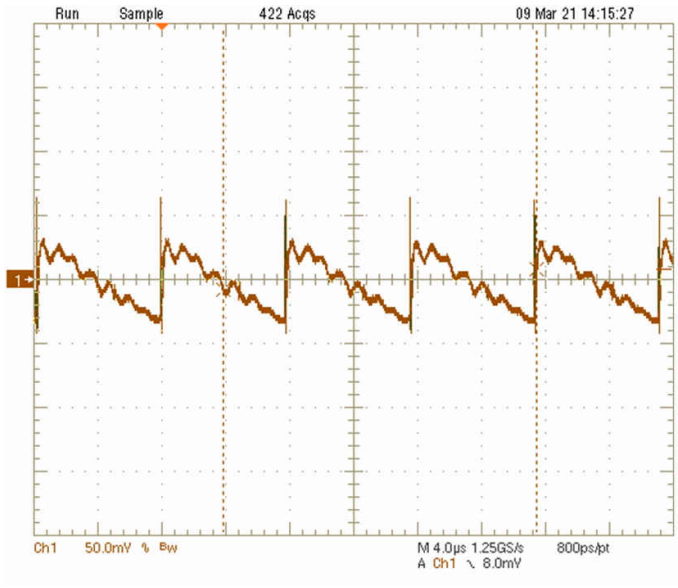


100 mV / div

20-MHz bandwidth

Figure 3-5. Output Voltage at 18-V Input Voltage

3.2.2 24-V Input Voltage



50 mv / div

20 MHz bandwidth

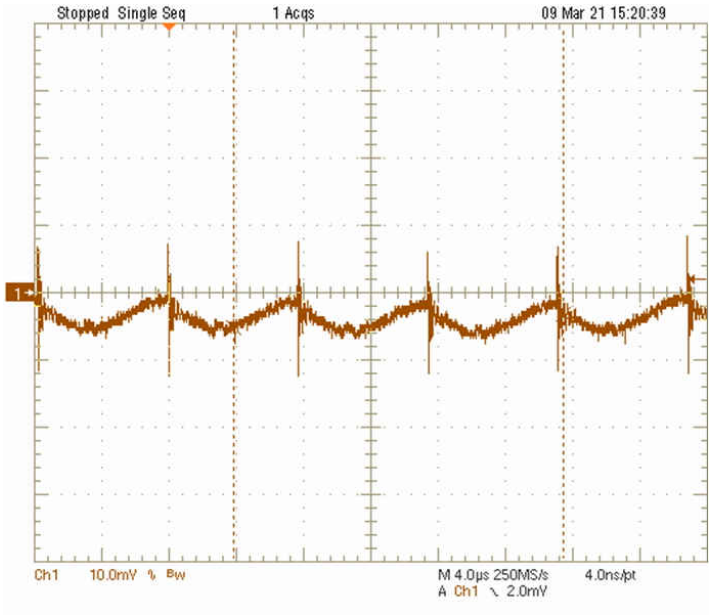
4 µs / div

Figure 3-6. Output Voltage at 24-V Input Voltage

3.3 Input Voltage Ripple

3.3.1 18-V Input Voltage

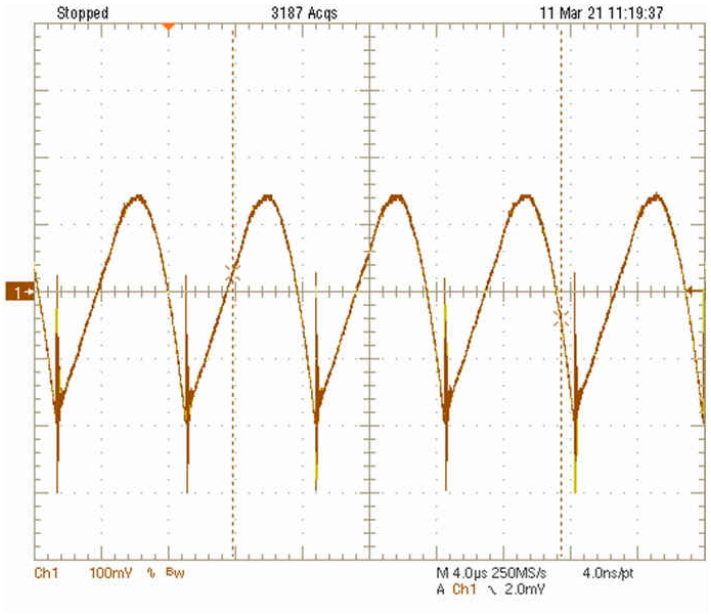
3.3.1.1 Input Terminal J2



10 mV div
20-MHz bandwidth
4 µs / div

Figure 3-7. Input Ripple Voltage (18-V Input Voltage)

3.3.1.2 Power Stage Input

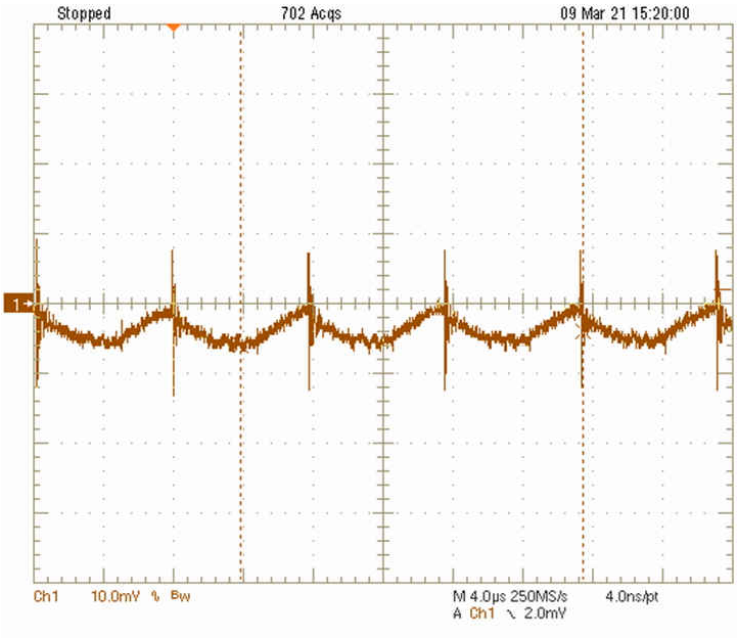


100 mV / div
20-MHz bandwidth
4 µs / div

Figure 3-8. Input Ripple Voltage Behind Filter (18-V Input Voltage)

3.3.2 24-V Input Voltage

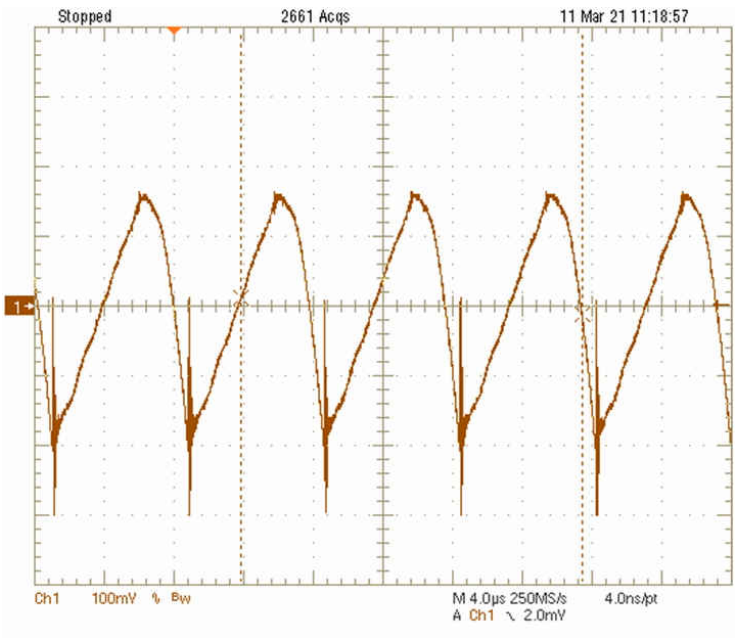
3.3.2.1 Input Terminal J2



10 mV / div
20-MHz bandwidth
4 µs / div

Figure 3-9. Input Ripple Voltage (24-V Input Voltage)

3.3.2.2 Power Stage Input



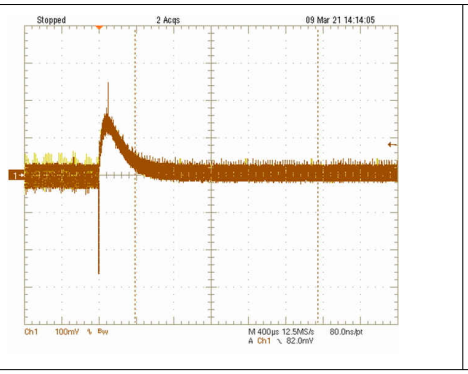
100 mV / div
20-MHz bandwidth
4 µs / div

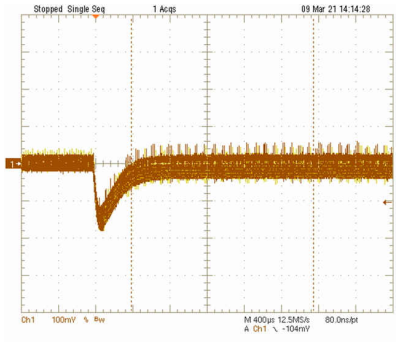
Figure 3-10. Input Ripple Voltage Behind Filter (24-V Input Voltage)

3.4 Load Transients

Load transient response is shown in the following figures.

3.4.1 18-V Input Voltage





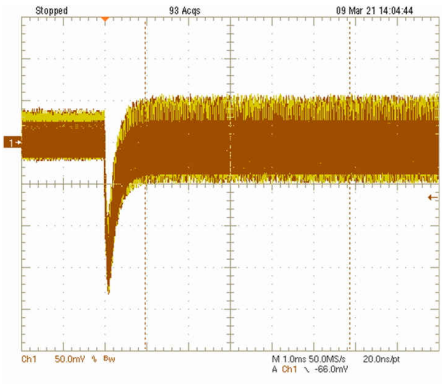
100 mV / div

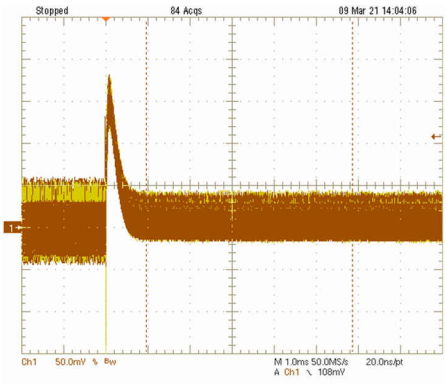
20-MHz bandwidth

400 µs / div

Figure 3-11. Load Transient With 18-V Input Voltage

3.4.2 24-V Input Voltage





50 mV / div

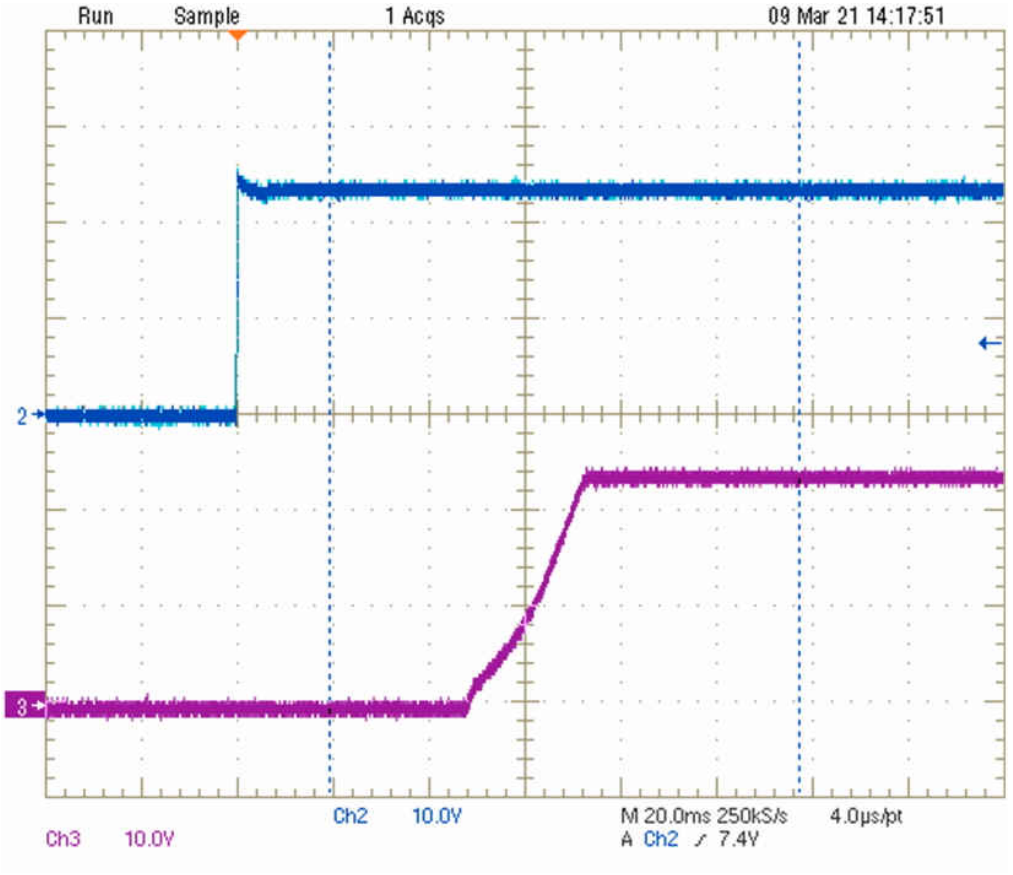
20-MHz bandwidth

1 ms / div

Figure 3-12. Load Transient With 24-V Input Voltage

3.5 Start-Up Sequence

3.5.1 18-V Input Voltage



Ch2 ⇒ input voltage

10 V / div

Ch3 ⇒ output voltage

10 V / div

20 ms / div

Figure 3-13. Start-Up With 18-V Input Voltage

3.5.2 24-V Input Voltage

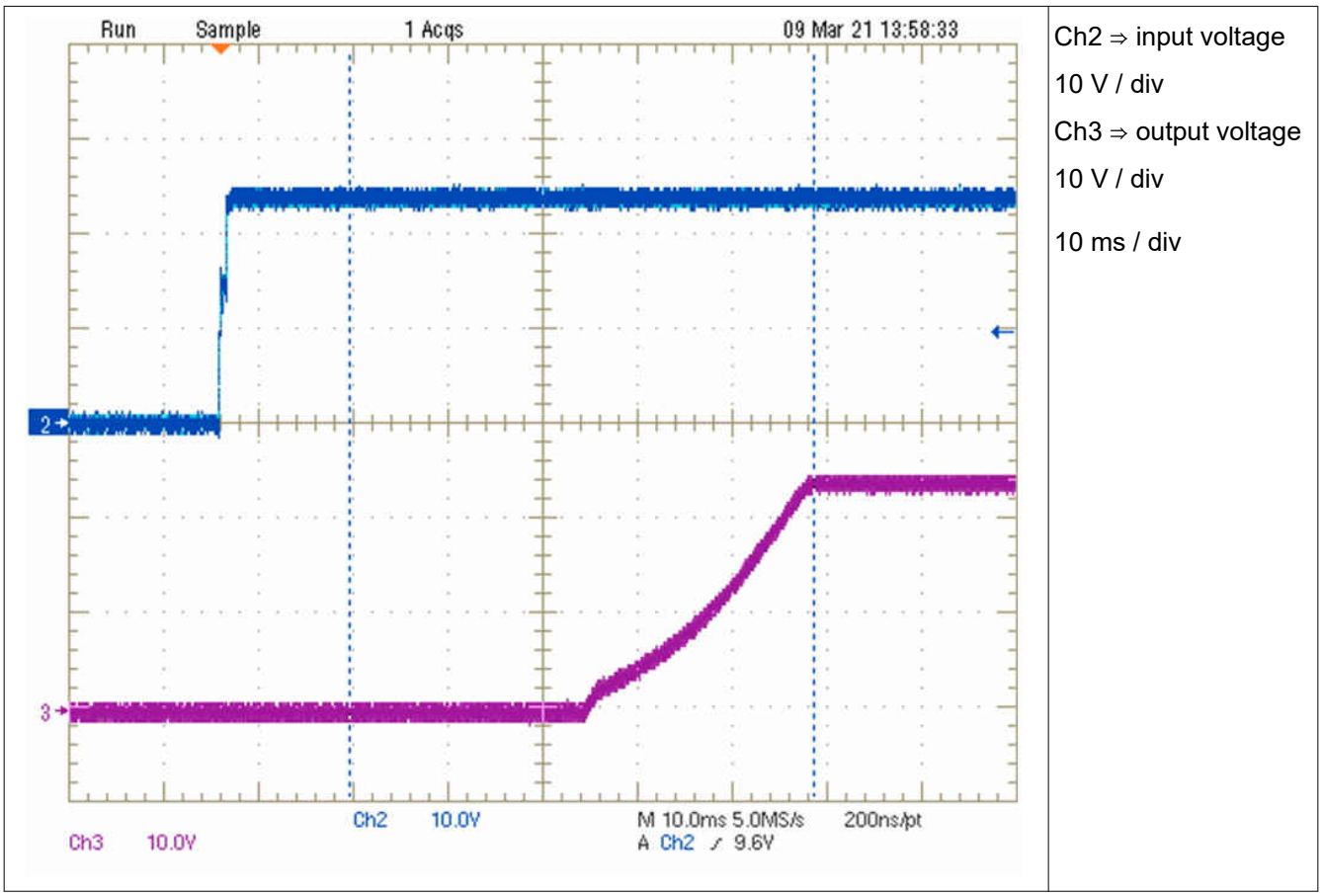
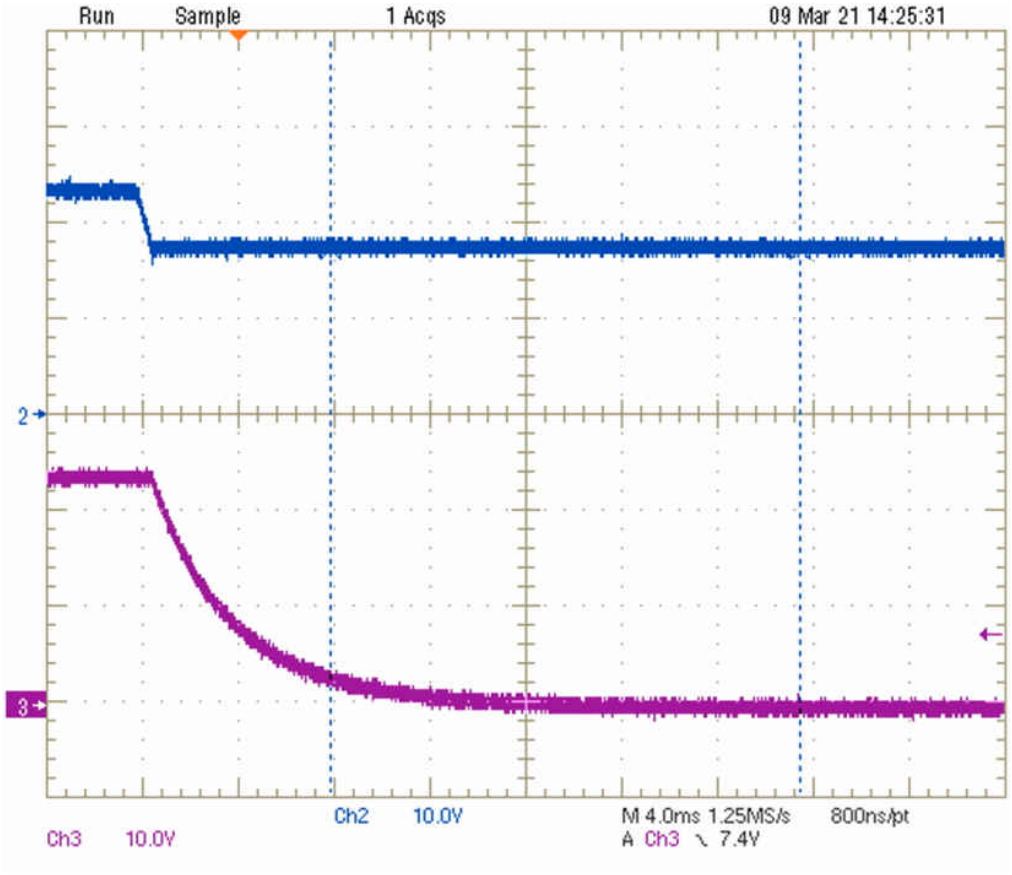


Figure 3-14. Start-Up With 24-V Input Voltage

3.6 Shutdown Sequence

3.6.1 18-V Input Voltage



Ch2 ⇒ input voltage

10 V / div

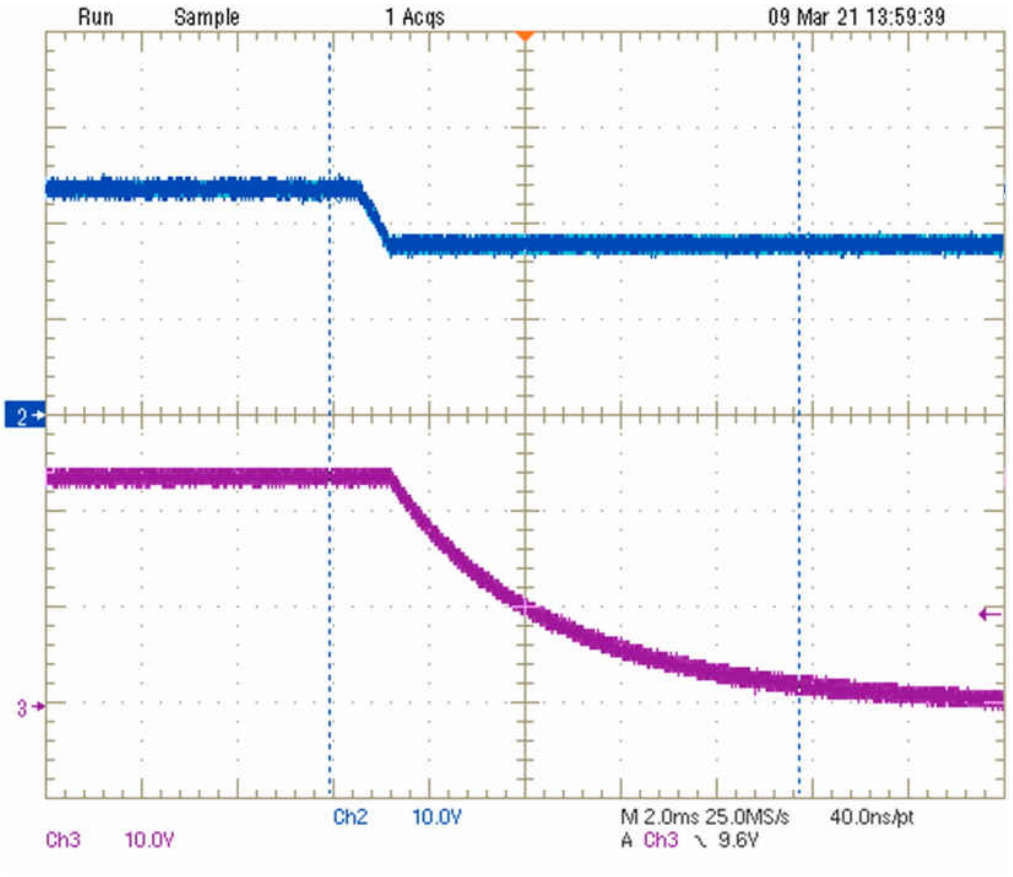
Ch3 ⇒ output voltage

10 V / div

4ms / div

Figure 3-15. Shutdown With 18-V Input Voltage

3.6.2 24-V Input Voltage



Ch2 ⇒ input voltage

10 V / div

Ch3 ⇒ output voltage

10 V / div

2 ms / div

Figure 3-16. Shutdown With 24-V Input Voltage

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265