Design Guide: TIDA-01292
650-W Power Stage Without Heat Sink Reference Design for Low-Frequency Offline UPS and Inverters

TEXAS INSTRUMENTS

Description

This reference design is a 650-W inverter power stage designed for low-frequency (transformer based), single-phase UPS operating from a 12-V battery.

The design enables low form factor and high-efficiency implementation, taking the advantage of the TI SMD MOSFET in SON5x6 package with very low $R_{DS(ON)}$ and low gate charge (Q_g). Using two devices in parallel for each leg of the full-bridge power stage, the power stage eliminates the need of a heat sink, which reduces overall system cost.

For driving the MOSFETs, this design uses the LM5101B, a 2-A gate driver with a high slew rate, which further reduces the switching losses. A bidirectional current sense amplifier INA181 is used for precision current sensing, for overcurrent, and short-circuit protection. The firmware for high-frequency sinusoidal PWM operation and robust protections is implemented using the TI Piccolo™ microcontroller TMS320F28027 LaunchPad™.

The board is tested for operation with low-frequency transformer (12-V AC:220-V AC) with both resistive and inductive load conditions. Also the board is validated for robustness of operation and for built-in protections of undervoltage, overvoltage, overload, and short-circuit conditions.

Resources

TIDA-01292	Design Folder
CSD17573Q5B	Product Folder
LM5101B	Product Folder
INA181	Product Folder
TLV704	Product Folder
LMV431B	Product Folder
LMT88	Product Folder

ASK Our E2E Experts

Features

- Designed for Standby or Offline UPS From 100 to 850 VA, Can be Extended up to 1.5 kVA With Additional FETs in Parallel
- Solution With SMD MOSFETs Enhances Manufacturability and Assembly of the UPS
- No Heat Sink for Power Dissipation Reduces System Cost and Production Time
- Tested and Validated for 100- to 650-W Operation With Bulb Loads
- Typical Efficiency of ≈ 95%, Maximum Efficiency of > 98.5%
- Protections for Overcurrent, Short Circuit, Overvoltage, and Undervoltage

Applications

- Offline and Standby UPS
- DC-to-AC Inverters
- Energy Storage Systems
- Home and Residential Inverters

Copyright © 2017, Texas Instruments Incorporated
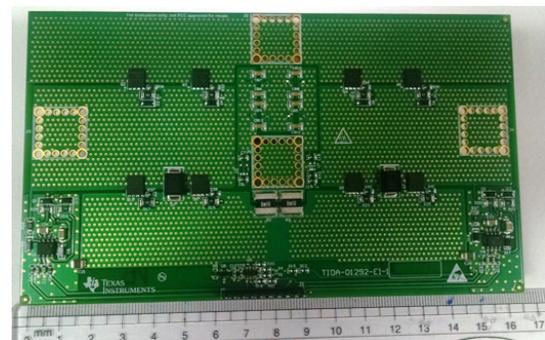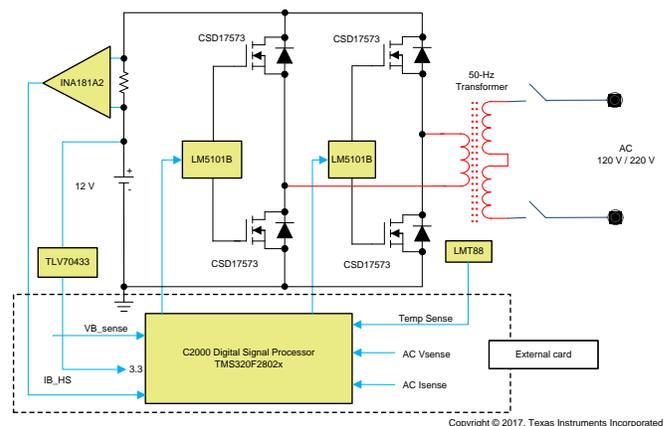
⚖ An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

A power inverter is a device that converts electrical power from a DC form to an AC form using electronic circuits. Its typical application is to convert battery voltage into conventional household AC voltage, allowing one to use household electronic equipment when AC power is not available. There are three kinds of inverters. The first set of inverters made produced a square wave signal at the output as shown in Figure 1; however, these are now obsolete.

The modified-square wave, also known as the modified-sine wave inverter, produces square waves with some dead spots between positive and negative half-cycles at the output. The cleanest utility supply-like power source is provided by a pure sine wave inverter. The present inverter market is going through a shift from traditional modified-sine wave inverters to pure sine wave inverters because of the benefits that these inverters offer.

These inverters are also part of energy storage systems where the charging of the battery is done through renewable energy means such as solar and wind, and DC-to-AC conversion is done through inverters.
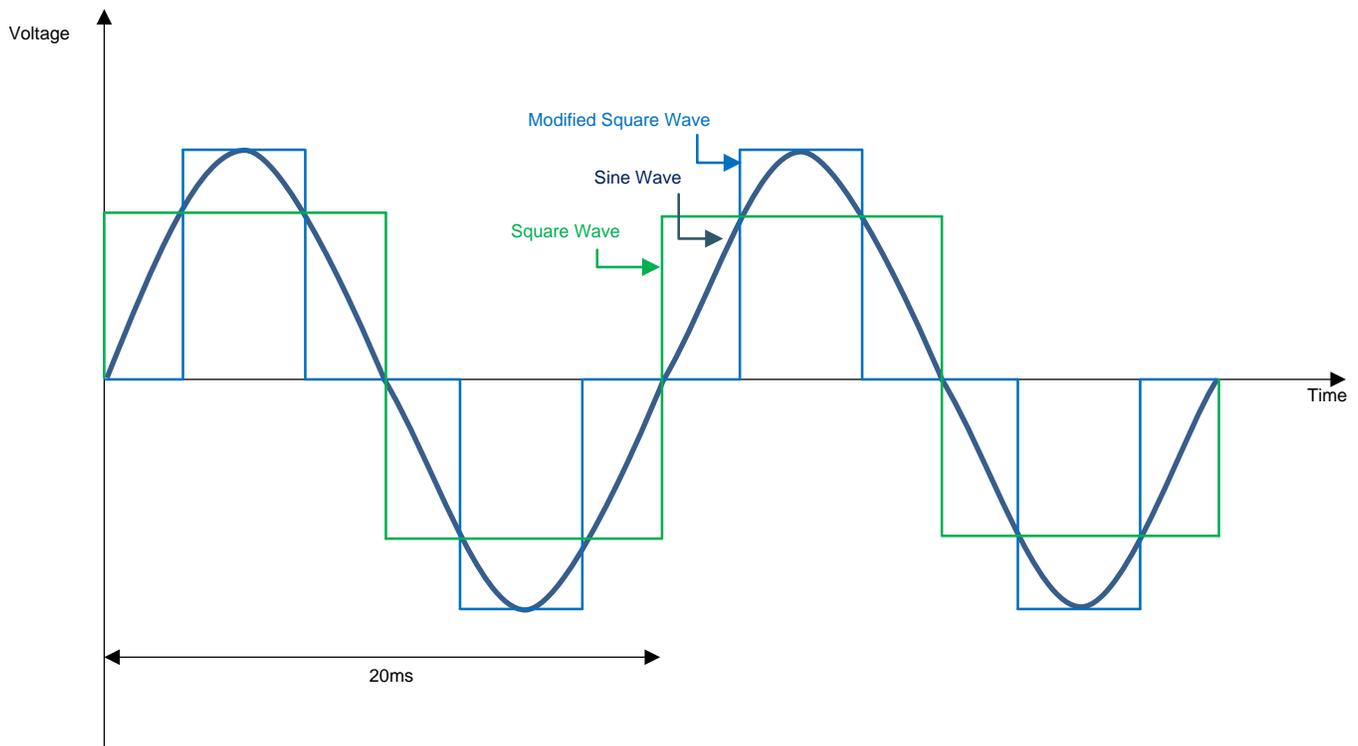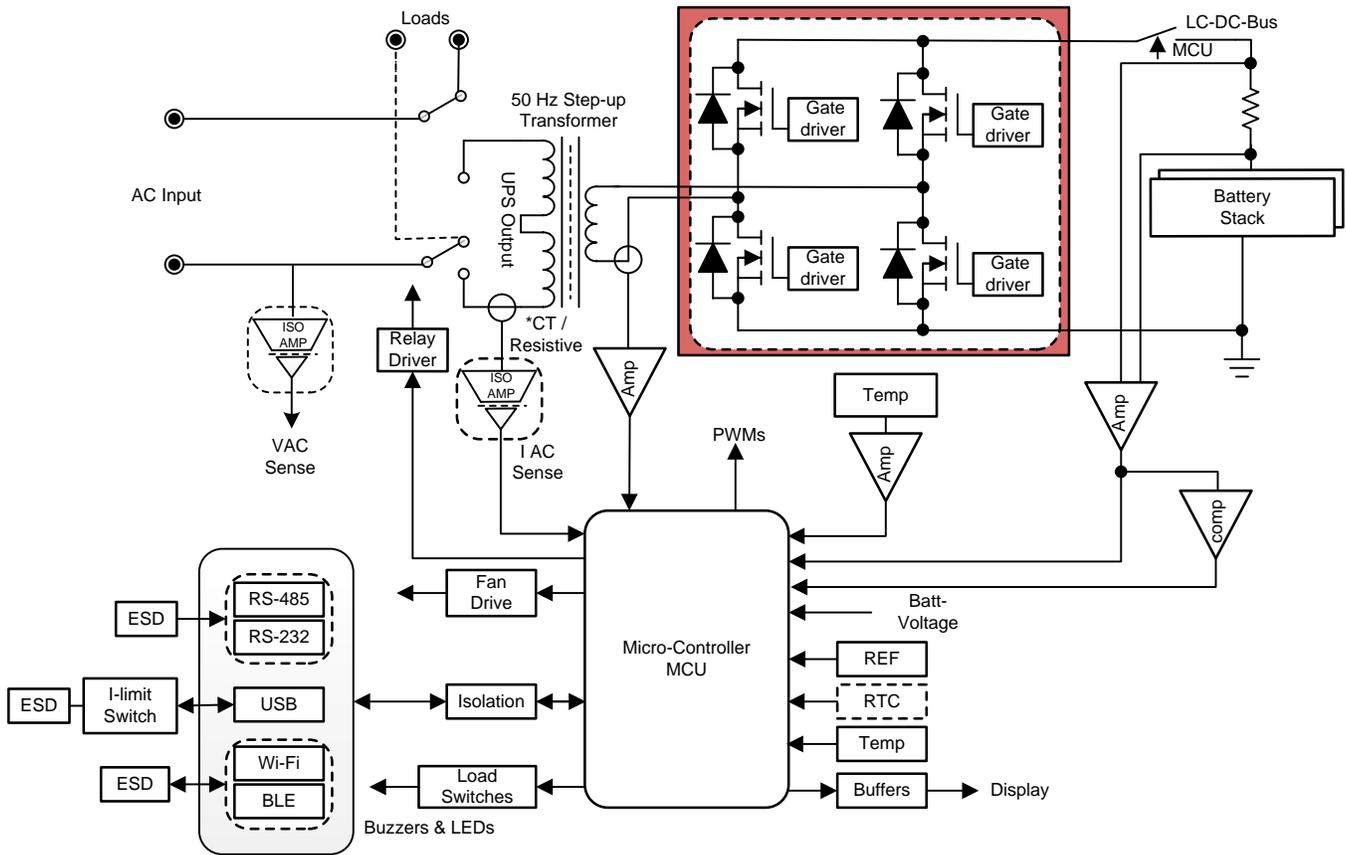

Figure 1. Types of Inverter Outputs

1.1 Design of Pure Sine Wave Inverter

Figure 2 shows the system block diagram of a single-phase UPS.

Copyright © 2017, Texas Instruments Incorporated

Figure 2. System Block Diagram of Single-Phase UPS

There are two modes of operation in a residential inverter: mains mode and inverter mode. An inverter not only converts the battery voltage to 220/120-V AC but also charges the battery when the AC mains is present.

The method in which the low-voltage DC power is converted to AC is generally done in two steps:

1. Convert low-voltage DC power to a high-voltage DC source.
2. Convert high-voltage DC to AC waveform using pulse width modulation (PWM). This step is also called a transformer-less approach.

Another method to achieve the desired outcome would be to first convert the low-voltage DC power to AC, then use a transformer to boost the voltage to 120 or 220 V (thus called the transformer-based inverter). This method is widely used in residential inverters, on which this reference design is based.

Copyright © 2017–2019, Texas Instruments Incorporated

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Input voltage	10	12	14	VDC
Rated output power	550	650	750	W
Switching frequency	—	12	—	kHz
Cooling	400	600	800	LFM
Operating ambient	−20	25	55	°C
Efficiency	—	95	98.6	%
Protections	Overcurrent			
	Overvoltage			
	Undervoltage			
	Overtemperature			
Board specification	90 mm × 155 mm, two-layer, 2-oz copper			

2 System Overview

2.1 Block Diagram

Copyright © 2017, Texas Instruments Incorporated
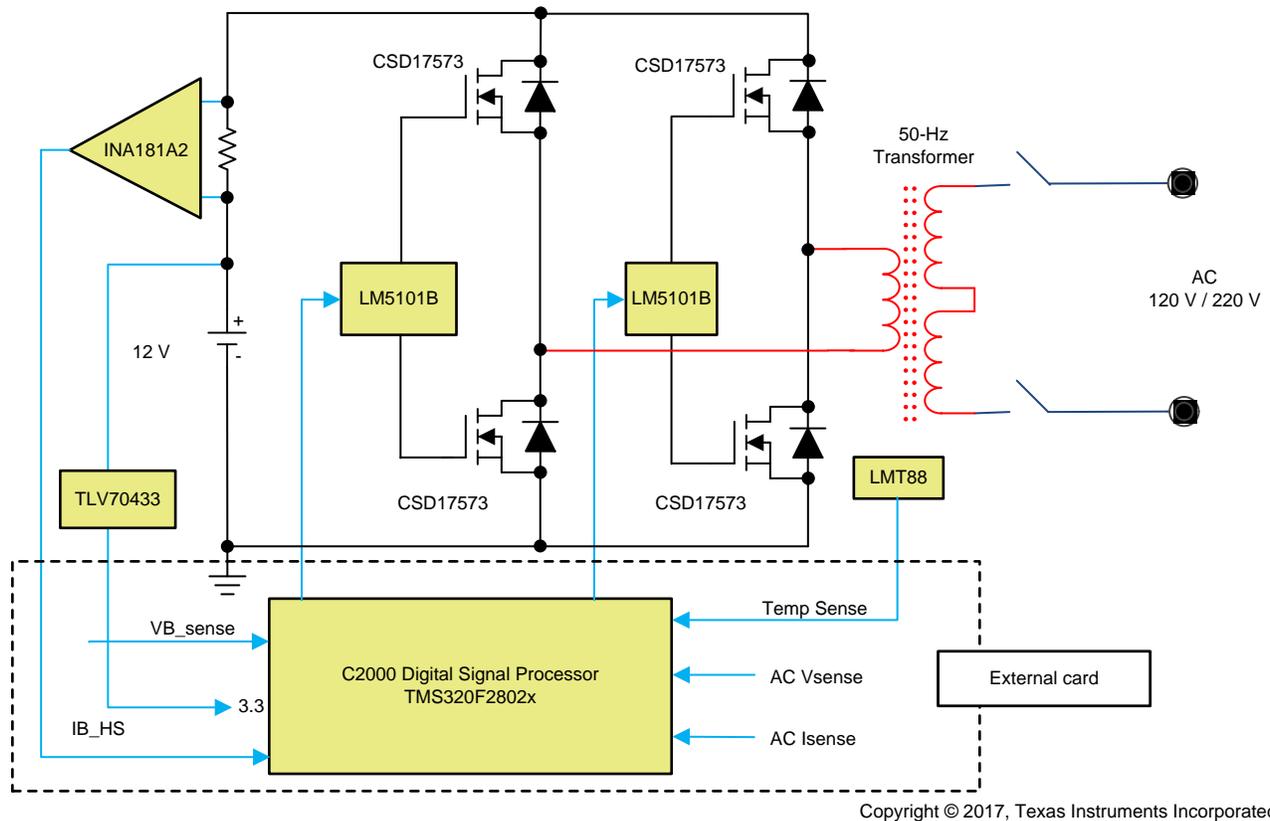
2.2 Highlighted Products

2.2.1 CSD17573Q5B

This design uses eight CSD17573Q5B MOSFETs to form the inverter stage. This FET was chosen due to its low $R_{DS(on)}$ of 0.84mΩ and a low-gate charge, designed to minimize the losses in power conversion and switching applications. The device comes in a compact, 8-pin SON 5-mm×6-mm package.

Key features of the CSD17573Q5B include:

- Low Q_g and Q_{gd}
- Ultra-low $R_{DS(on)}$
- Low-thermal resistance
- Avalanche rated
- Lead-free terminal plating
- RoHS compliant
- Halogen free
- SON 5-mm×6-mm plastic package

2.2.2 LM5101B

This design uses two LM5101B devices. The LM5101B high-voltage gate driver is designed to drive both the high- and the low-side N-channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100 V. The LM5101B provides 2 A of gate drive. The outputs are independently controlled with CMOS input thresholds.

An integrated high-voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operated at high speed while consuming low power and providing clean level transitions form the control logic to the high-side gate driver. Undervoltage lockout is provided on both the low-side and the high-side power rails.

Key features of the LM5101B include:

- Drives both a high- and low-side N-channel MOSFETs
- Independent high-and low-driver logic inputs
- Bootstrap supply voltage up to 118-V DC
- Fast propagation times: 25 ns typical
- Drives 1000-pF load with 8-ns rise and fall time
- Excellent propagation delay matching: 3 ns typical
- Supply rail undervoltage lockout
- Low power consumption

2.2.3 INA181

This design uses the INA181 to sense the current through MOSFETs and to protect the system for overcurrent. The INA181 device is a bidirectional current sense amplifier that senses voltage drop across current sense resistors at common-mode voltages from –0.2 to 26V, independent of the supply voltage. This design uses the A2 version with fixed gain of 50, which is achieved by integrated matched resistor gain network to minimize the gain error and reduce the temperature drift.

Key features of the INA181 include:

- Common-mode range (V_{CM}): –0.2 to 26 V
- High bandwidth: 350 kHz
- Offset voltage:
  - ±150 μV (max) at V_{CM} = 0 V
  - ±500 μV (max) at V_{CM} = 12 V
- Output slew rate: 2 V/μs
- Bidirectional current-sensing capability
- Accuracy:
  - ±1% gain error (max)
  - 1-μV/°C offset drift (max)
- Gain Options:
  - 20 V/V (A1 devices)
  - 50 V/V (A2 devices)
  - 100 V/V (A3 devices)
  - 200 V/V (A4 devices)
- Quiescent current: 260 μA (max per channel)

2.2.3.1 INA185

For higher-performance current sensing and overcurrent protection, the INA185 current sense amplifier can be considered.

Benefits of the INA185 over the INA181 include:

- Offset voltage:
  - ±55 µV (max) at VCM = 0 V (A2 device)
  - ±130 µV (max) at VCM = 12 V (A2 device)
- Accuracy:
  - ±0.2% gain error (max, A2 device)
  - 0.5- µV/°C offset drift (max)
- Small package:
  - SOT-563 (6): 1.6mm x 1.6mm (including pins)

2.3 System Design Theory

2.3.1 Inverter Operation and PWM Explanation

The DC-to-AC inversion can be achieved using two methods:

1. The first is the conversion of low-voltage DC to a high-voltage DC followed by the conversion of this high-voltage DC to AC using PWM.

2. Another method is to first convert the low-voltage DC to AC and then use a transformer to boost the voltage to 120 or 220 V.

This design uses the second method of inverting DC to AC using an H-bridge circuit where the MOSFETs are switched with high frequency SPWM signals. The switching waveforms used for this design is explained in the following subsections.

2.3.1.1 Switching Waveforms

Figure 3 shows the sine PWM used for each switch:
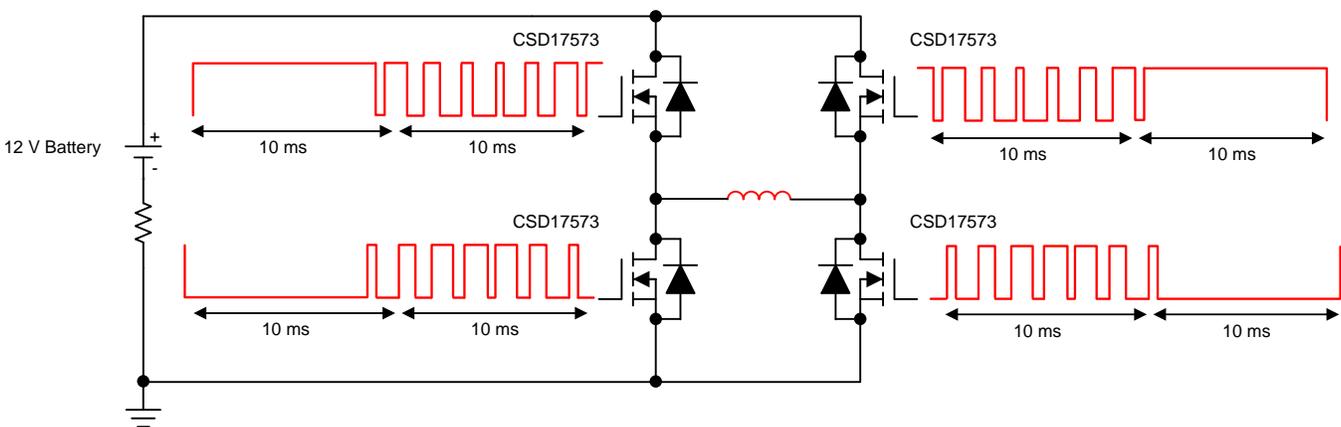
Copyright © 2017, Texas Instruments Incorporated

Figure 3. SPWM Sequence Used for TIDA-01292

The switching algorithm as shown in Figure 3 can be broken in following sequence:

1. The 50-Hz sine output can divided into two time intervals of 10 ms each.

2. During the first 10 ms:
   • The left leg is switched at 50 Hz (that is, the top-left FET) is continuously on for 10 ms and the bottom-left FET is continuously off for that time.
   • The top- and bottom-right FETs are switched at a high frequency (12 kHz in this case) such that the duty cycle for the bottom FET goes from 0 to maximum and back to 0 while the duty cycle of the top FET varies from maximum to 0 and back to maximum in sinusoidal modulation.

3. During the next 10 ms:
   • The right leg is switched at 50 Hz (that is, the top-right FET) is continuously on for 10 ms and bottom-right FET is continuously off for the same 10ms period.
   • The top- and bottom-left FETs are switched at a high frequency (12 kHz in this case) such that the duty cycle for the bottom FET goes from 0 to maximum and back to 0 while the duty cycle of the top FET varies from maximum to 0 and back to maximum in sinusoidal modulation.

2.3.1.2 Power Flow

Figure 4 to Figure 7 show the power flow for the entire 50-Hz cycle.

Figure 4 shows the power transfer from input to output during the positive half cycle where, as mentioned earlier, the top-left FET remains on and the bottom-left FET remains off continuously for 10 ms while the right-side FETs are switched at a high-frequency SPWM. As seen in Figure 5, during the positive half cycle, the current freewheels through the body diode of the top-right FET until the FET is switched on. This makes sure the design has ZVS switching across the top FET.
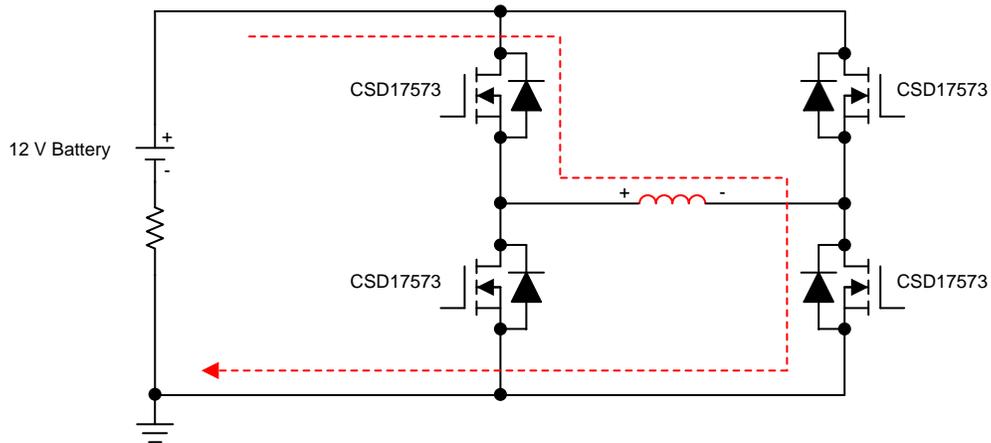
Copyright © 2017, Texas Instruments Incorporated

Figure 4. Increasing Positive Output
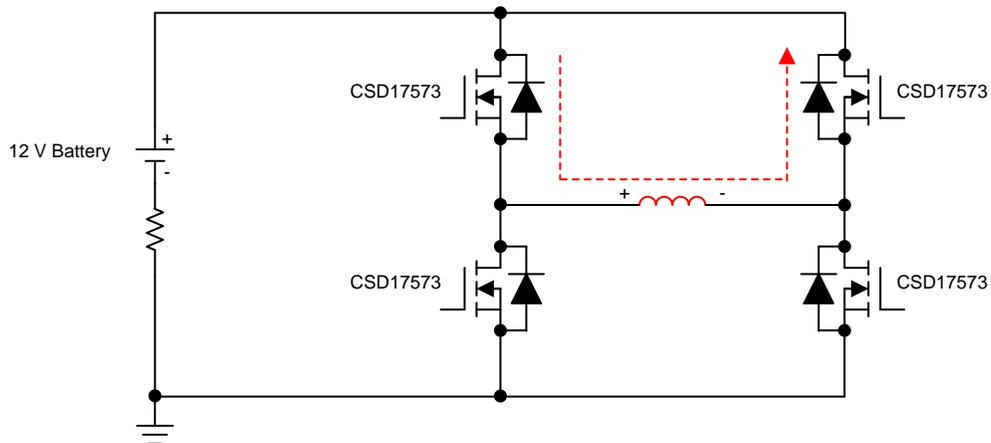
Copyright © 2017, Texas Instruments Incorporated

Figure 5. Decreasing Positive Output

A similar power flow sequence takes place in the negative half cycle where the top-right FET is continuously on and the bottom-right FET is continuously off while the left leg is switched. As a result, the power flow takes place when the left bottom FET is on and freewheeling happens when the left top FET is on, as shown in Figure 6 and Figure 7.
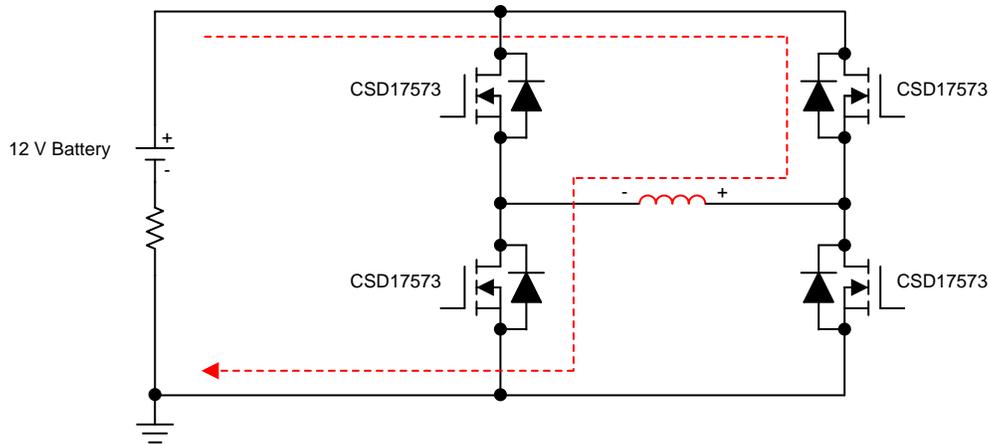
Copyright © 2017, Texas Instruments Incorporated

Figure 6. Increasing Negative Output
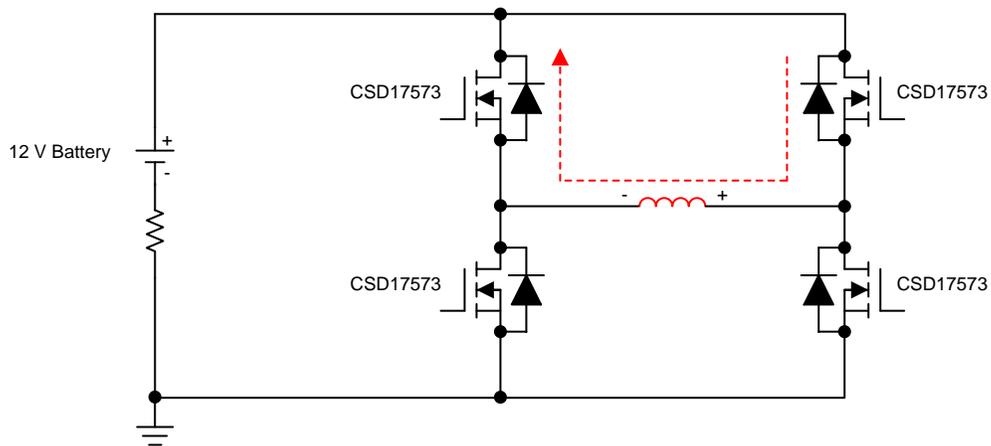
Copyright © 2017, Texas Instruments Incorporated

Figure 7. Decreasing Negative Output

The positive peak of the sine wave is achieved during maximum duty cycle switching of the bottom-right FET, and the negative peak is observed when the bottom-left FET is switched at the highest duty cycle. Also, the top FETs are always synchronous switching, which reduces the switching loss across them, while the bottom FETs are kept off for half the cycle and only switched during the other half, which reduces the conduction losses across them.

2.3.2 Gate Driver Design

2.3.2.1 *Bootstrap and VDD Capacitor*

The bootstrap capacitor must maintain the HB pin voltage above the UVLO voltage for the HB circuit in any circumstances during normal operation. Thus, the maximum allowable drop across the bootstrap capacitor is calculated with lowest battery voltage, as shown in Equation 1:

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL} = 10 - 0.7 - 6.7 = 2.6 \text{ V} \tag{1}$$

where:

- V_{DD} = Supply voltage of the gate drive IC
- V_{DH} = Bootstrap diode forward voltage drop
- $V_{HBL} = V_{HBR} - V_{HBH} = 6.7$ V, HB falling threshold based on the LM5101B datasheet (SNOSAW2)

The maximum quiescent current required by the driver and the bootstrap circuit is 0.2 mA as per the LM5101B datasheet. Also, due to the kind of switching scheme implemented for the inverter, the top FET remains on for 10 ms continuously; thus, the bootstrap capacitor must be able to supply the charge required during this entire time. The total charge required by the bootstrap capacitor can be calculated using Equation 2:

$$Q_{Total} = Q_{gmax} + I_{HBmax} \times T_{on} \tag{2}$$

where:

- Q_{gmax} is the total gate charge of the FET
- I_{HBmax} is the maximum quiescent current requirement of the driver and the bootstrap circuit
- T_{on} is the maximum on time of the FET (10 ms)

The total charge required by the bootstrap capacitor is: $Q_{Total} = 64 \text{ nC} + 0.2 \text{ mA} \times 10 \text{ ms} = 2.064 \text{ }\mu\text{C}$

The value of the bootstrap capacitor is calculated using Equation 3:

$$C_{BOOT} = \frac{Q_{Total}}{\Delta V_{HB}} = \frac{2.064 \text{ }\mu\text{V}}{2.6 \text{ V}} = 0.8 \text{ }\mu\text{F} \tag{3}$$

In practice, the value for the C_{BOOT} capacitor must be greater than the calculated value to allow for situations where the power stage may skip a pulse due to load transients. It is recommended to use 10 times the calculated value and place the bootstrap capacitor as close to the HB and HS pin as possible. A 10-µF capacitor is used for C_{BOOT} in this design.

As a general rule, the local V_{DD} bypass capacitor must be 10 times greater than the value of C_{BOOT}. For this design, a 100-µF electrolytic capacitor and a 10-µF ceramic capacitor is used for the V_{DD} supply.

2.3.2.2 *External Bootstrap Diode and Resistor*

The bootstrap capacitor is charged by the V_{DD} through the internal bootstrap diode every cycle when the low-side MOSFET turns on. The charging of the capacitor involves high-peak currents; therefore, transient power dissipation in the internal bootstrap diode may be significant and dependent on its forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver and need to be considered in the power dissipation of the gate driver.

For high-frequency and high-capacitive loads, consider using an external bootstrap diode placed in parallel with the internal bootstrap diode to reduce power dissipation of the driver. For this design, a 20-V Schottky diode with a typical forward voltage drop of 0.38V at 1A is used in parallel to the internal bootstrap diode.

Bootstrap resistor R_{BOOT} is selected to reduce the inrush current in D_{BOOT} and limit the ramp-up slew rate of the voltage of HB-HS. This resistor serves two purposes: one is limiting the inrush current through D_{BOOT}; the other is protecting the driver from the negative voltage spikes at the common-mode point. The value of this resistor must be just large enough to protect the diode. A very large value resistor cannot be used because this creates a potential difference between the source of the high-side MOSFET and the HS pin of the driver at the beginning of the PWM cycles until the C_{BOOT} is not charged to full voltage. Due to this potential difference, the gate of the FET is only pulled low to the HS pin voltage level and not to the actual source level, which might create issues. For this design, a 1-Ω R_{BOOT} resistor is used in the path of C_{BOOT} and common-mode point, as shown on Figure 8.

It is also recommended to place a Schottky diode at the HS pin to further protect the driver from negative spikes.

Copyright © 2017, Texas Instruments Incorporated

Figure 8. Gate Driver Schematic

2.3.2.3 *Gate Drive Resistor*

Resistor R_{Gate} is sized to reduce ringing caused by parasitic inductances and capacitances and to limit the current coming out of the gate driver. For this design, a 6-Ω resistor is used for turnon and a 3-Ω resistor for turnoff. Maximum high-side and low-side turnon and turnoff currents are calculated using Equation 4 to Equation 7.

$$I_{HOH} = \frac{V_{DD} - V_{DH} - V_{OH}}{R_{Gate}} = \frac{10\ V - 0.7\ V - 0.45\ V}{6\ \Omega} = 1.475\ A \tag{4}$$

$$I_{LOH} = \frac{V_{DD} - V_{OH}}{R_{Gate}} = \frac{10\ V - 0.45\ V}{6\ \Omega} = 1.592\ A \tag{5}$$

$$I_{HOL} = \frac{V_{DD} - V_{DH} - V_{OL}}{R_{Gate}} = \frac{10\ V - 0.7\ V\ 0.25\ V}{3\ \Omega} = 3.02\ A \tag{6}$$

$$I_{LOL} = \frac{V_{DD} - V_{OL}}{R_{Gate}} = \frac{10\ V - 0.25\ V}{3\ \Omega} = 3.25\ A \tag{7}$$

2.3.3 Current Sensing

To protect the FETs from overcurrent failure, a current sensing circuitry is implemented in this design. Usually, an inverter requires to sense both the battery charging and discharging current. Thus, it is necessary to sense current in both directions. This design uses the low-cost bidirectional current sense amplifier INA181 with low-offset voltage, high-gain bandwidth product, and high accuracy, which can be used for high-side and low-side sensing. The current sensing schematic is shown in Figure 9.
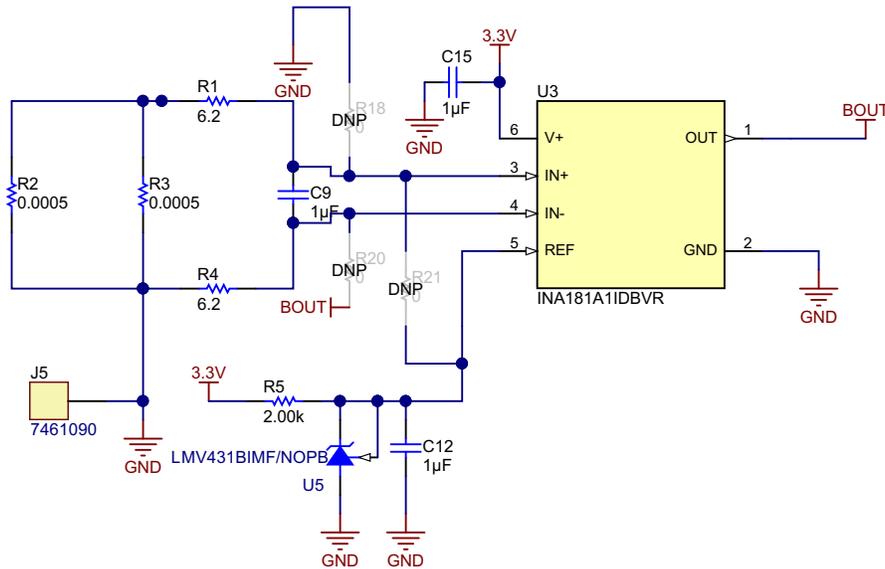
Copyright © 2017, Texas Instruments Incorporated

Figure 9. Current Sensing Schematic

The LMV431B is used for shunt reference, which provides a reference voltage of 1.24 V. Equation 8 shows the transfer function of current sensing circuitry.

$$\frac{V_{OUT}}{V_{IN}} = \left(I_{LOAD} \times R_{SENSE} \times Gain \right) + V_{REF}$$

(8)

To provide flexibility for overall gain, two sense resistors are used in parallel. The TIDA-01292 design uses two 0.5-mΩ resistors in parallel for R_{SENSE} and the INA181 with a fixed gain of 50. This design also uses a low-pass filter with a cutoff frequency of around 13 kHz at the input of the INA181.

A provision to use an op amp and external resistors for adjustment of gain is also provided in this design.

2.3.4 Loss Calculation

Loss calculation is important to theoretically estimate the temperature of various components on the board to estimate the total power handling capability of the design.

The majority of losses that take place in the inverter are the conduction loss, switching loss, body diode conduction loss, loss in the current sense resistor, and loss in the bulk of the PCB.

2.3.4.1 Conduction Loss in MOSFETs

To calculate conduction loss, have the equivalent RMS current through each MOSFET. Due to the nature of the switching technique used, calculating RMS current is not as straight forward as for a normal sine wave.

To calculate the RMS current, the 50-Hz sine wave is divided is two time intervals of 10 ms each. For 10 ms, the top FET is conducting continuously while the bottom FET is off. During this time, conduction loss happens only in the top FET. For the other 10 ms, the top and bottom FETs are switching with sinusoidally varying duty cycle. Note that at any instant, the peak current through the FETs is also varying sinusoidally. Based on Figure 4 to Figure 7, the current through top and bottom FETs would look something like Figure 10 and Figure 11, respectively.
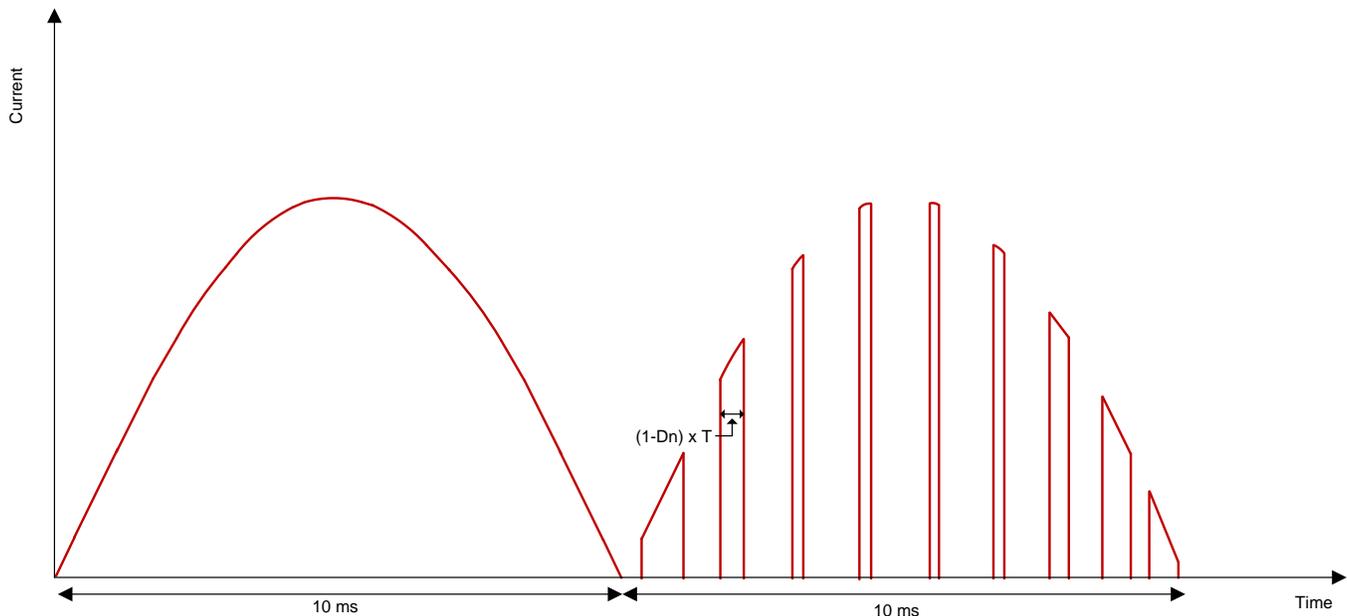

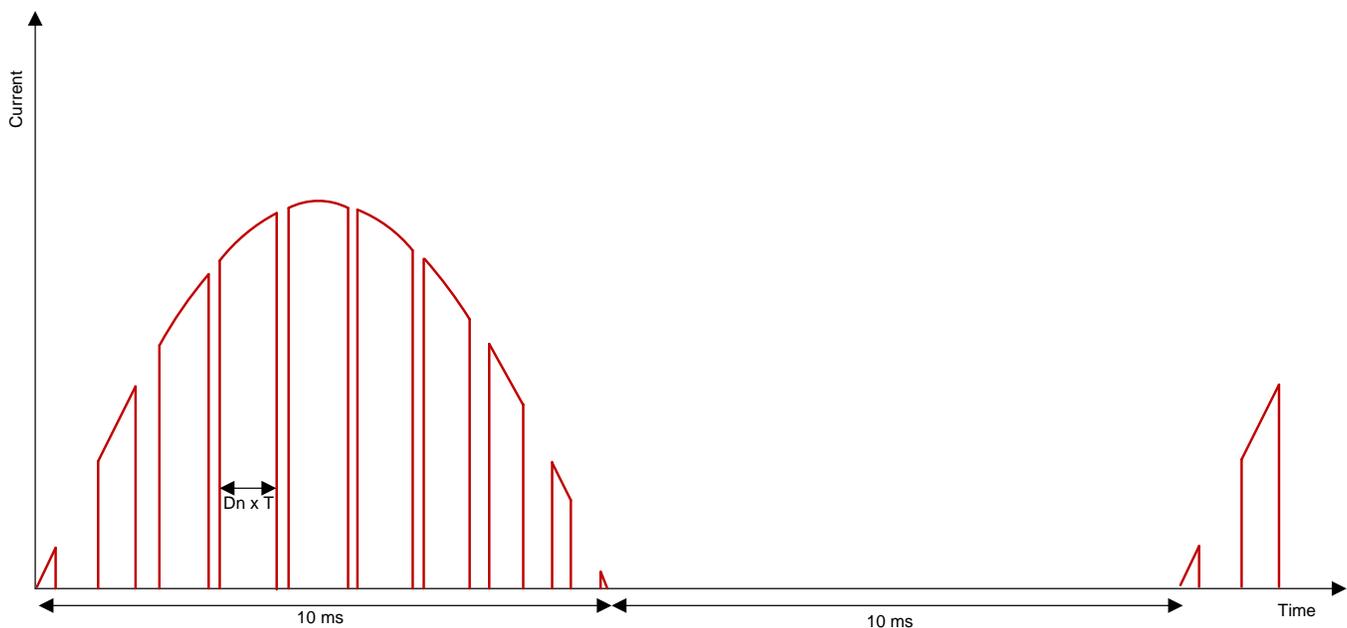**Figure 10. Current Waveform Through Top FET**

Figure 11. Current Waveform Through Bottom FET

During the switching period, the total current through the bottom FET is $D_n \times I_{Pn}$ while the current through top FET is $(1 - D_n) \times I_{Pn}$, where D_n is the duty cycle and I_{Pn} is the peak current at that particular switching instant n.

To calculate the total RMS current, the current waveform is divided into two parts of 10 ms each. The RMS current through each FET then would be calculated using Equation 9:

$$I_{RMS} = \sqrt{\frac{\left(I_{RMS1}\right)^2 + \left(I_{RMS2}\right)^2}{2}}$$

(9)

where:

• I_{RMS1} is the RMS current in the first 10 ms
• I_{RMS2} is the RMS current in the next 10 ms

For the bottom FETs, current flows through them only for 10 ms. To calculate the overall RMS current for the waveform as shown in Figure 11, first find out the RMS current for each switching instant given that the duty cycle and peak current for each instant is different and varies sinusoidally. For doing so, all the pulses can be assumed as square pulses because the time period is very small when compared to the 50-Hz sine. For a square pulse of magnitude A, the RMS value is $\sqrt{D} \times A$, where D is the duty cycle of the given pulse. Similarly, the RMS values for the individual pulses shown in Figure 11 is $\sqrt{D_n} \times I_{pn}$, where n is the instant of switching. Total switching instants are calculated using Equation 10:

$$n = \frac{f_{sw}}{50\,Hz} = \frac{12\,kHz}{50\,Hz} = 240$$

(10)

The RMS current through the bottom FET at any instant n is calculated as Equation 11:

$$I_{RMSn\_B} = \sqrt{D_n} \times I_P \times \sin\left(\frac{2n\pi}{240}\right)$$

(11)

To get sinusoidal output, the duty cycle is also varied in the same fashion. Assuming a modulation index of 1, the duty cycle for n^{th} instant can be calculated using Equation 12. Because the current though the bottom FET flows only for half the time (10 ms), for these calculations, n varies from 0 to 120.

$$D_n = \sin\left(\frac{2n\pi}{240}\right)$$

(12)

The total RMS current for this 10 ms is calculated using Equation 13:

$$I_{RMS1\_B} = \sqrt{\frac{\sum_{n=1}^{120} I_{RMSn\_B}^2}{120}}$$

(13)

Therefore, the RMS current for bottom FET I_{RMS_B} is calculated using Equation 14:

$$I_{RMS\_B} = \sqrt{\frac{\left(I_{RMS1\_B}\right)^2 + \left(I_{RMS2\_B}\right)^2}{2}} = \sqrt{\frac{\left(\sqrt{\frac{\sum_{n=1}^{120} I_{RMSn\_B}^2}{120}}\right)^2 + (0)^2}{2}} = \sqrt{\frac{\sum_{n=1}^{120} I_{RMSn\_B}^2}{120 \times 2}}$$

(14)

I_{RMS2} for the bottom FET is zero because one of the bottom FETs is continuously off for 10 ms.

Calculating the RMS current for the top FET is similar to the bottom FET. The only difference is that the conduction time for the top FET is $(1 - D_n)$ for I_{RMS1}, ignoring the dead time, and I_{RMS2} is not zero but a sine output. Again approximating the pulses to be square, the I_{RMSn} for n^{th} switching instant for the top FET can be calculated using Equation 15:

$$I_{RMSn\_T} = \sqrt{(1 - D_n)} \times I_p \times \sin\left(\frac{2n\pi}{240}\right)$$

(15)

Calculating D_n remains same as given by Equation 12. The RMS current for the switching time, I_{RMS1}, for the top FET is calculated using Equation 16:

$$I_{RMS1\_T} = \sqrt{\frac{\sum_{n=1}^{120} I_{RMSn\_T}^2}{120}}$$

(16)

The total RMS current for top FET is thus calculated using Equation 17:

$$I_{RMS\_T} = \sqrt{\frac{\left(I_{RMS1\_T}\right)^2 + \left(I_{RMS2\_T}\right)^2}{2}} = \sqrt{\frac{\left(\sqrt{\frac{\sum_{n=1}^{120} I_{RMSn\_T}^2}{120}}\right)^2 + \left(\frac{I_P}{\sqrt{2}}\right)^2}{2}} = \sqrt{\frac{\frac{\sum_{n=1}^{120} I_{RMSn\_T}^2}{120} + \left(\frac{I_P}{\sqrt{2}}\right)^2}{2}}$$

(17)

2.3.4.2 Switching Loss

One calculates the total switching loss usually by multiplying the energy lost and frequency to get the power loss. But in this case, because the peak current at every switching instant is different, the energy transferred at each instant is also different. Thus, to find out the total switching power loss, add up the energy transferred at each instant and find its average over the 50-Hz cycle.

The average of Equation 4 and Equation 5 gives the average turnon current (I_{Turnon}), and the average of Equation 6 and Equation 7 gives the average turnoff current ($I_{Turnoff}$). Because a 2-A driver is used for this design, the upper limit on the source and sink current is 2 A.

The energy transferred during the nth turnon and turnoff instant is calculated using Equation 18 and Equation 19, respectively:

$$E_{Turnon\_n} = \frac{1}{2} \times V_{DS} \times I_n \times \frac{\left(Q_{gs} - Q_{gs(th)} + Q_{gd}\right)}{I_{Turnon}}$$

(18)

$$E_{Turnoff\_n} = \frac{1}{2} \times V_{DS} \times I_n \times \frac{\left(Q_{gs} - Q_{gs(th)} + Q_{gd}\right)}{I_{Turnoff}}$$

(19)

where:
- V_{DS} is the drain-source voltage across FET
- I_n is the current at n^{th} switching instant and is given by Equation 20
- Q_{gs} is the total gate-source charge of the MOSFET, 17.1 nC for the CSD17573Q5B FET
- $Q_{gs(th)}$ is the gate-source charge at the threshold voltage, 8.6 nC for the CSD17573Q5B
- Q_{gd} is the gate-drain charge of the MOSFET, 11.9 nC for the CSD17573Q5B

$$I_n = I_p \times \sin\left(\frac{2n\pi}{240}\right)$$

(20)

The total power loss at turnon and turnoff is calculated using Equation 21 and Equation 22:

$$P_{loss\_on} = \frac{\sum_{n=1}^{120} E_{Turnon\_n}}{20 \text{ ms}}$$

(21)

$$P_{loss\_off} = \frac{\sum_{n=1}^{120} E_{Turnoff\_n}}{20 \text{ ms}}$$

(22)

Note that any of the four MOSFETs switches, only for half the cycle (10 ms)—thus only 120 energy instants—are added up to calculate power loss. Due to the switching scheme used, the top FET is always soft switching. As a result, the majority of switching losses are in the bottom FETs only. To calculate the switching loss across top FET accurately, replace V_{DS} with the forward drop of the body diode of the FET.

2.3.4.3   *Body Diode Loss*

To ensure there is not any shoot-through condition, a dead time of 500 ns is provided in the firmware. During this dead time, the entire load current flows through the body diode, causing power loss across it. Because the dead time appears twice during one switching cycle, that is at turnon and turnoff, consider it twice at all switching instants. Again, because the peak current flowing through it varies sinusoidally, calculate the energy at all these instants, add them up, and find the average over one entire cycle of 50 Hz. The energy at any instant n is calculated using Equation 23:

$$E_{n\_body\_diode} = 2 \times V_f \times I_n \times t_d \tag{23}$$

where:
- V_f is the forward voltage drop of the body diode
- I_n is the current at n^{th} instant given by Equation 20
- t_d is the dead time (500 ns for this design)

The total power loss in one leg is thus calculated using Equation 24:

$$P_{body\_diode} = \frac{\sum_{n=1}^{120} E_{n\_body\_diode}}{20 \text{ ms}} \tag{24}$$

Body diode loss occurs only in the top MOSFETs for the PWMs used for this design because bottom switches are hard switched every time.

2.3.4.4   *Miscellaneous Losses*

In addition to the major losses mentioned previously:
- Board copper: This loss depends on board dimension, Cu thickness, and FET placement. There is also a considerable amount of conduction losses in the board copper as well.
- Input bulk capacitors: The electrolytic capacitors present at the input also result in conduction loss depending on the ripple current and the ESR of the capacitor.
- Sense resistor: Because the load current for this design is large, there is conduction loss in sense resistor as well, which cannot be ignored.
- Other than these components, there is also power loss in the gate drivers and LDOs, but this is usually very small compared to other losses and thus can be ignored.

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware

Figure 12 shows the test setup of the board with the transformer, bulb loads, and interface to the TMS320F28027 LaunchPad for firmware.
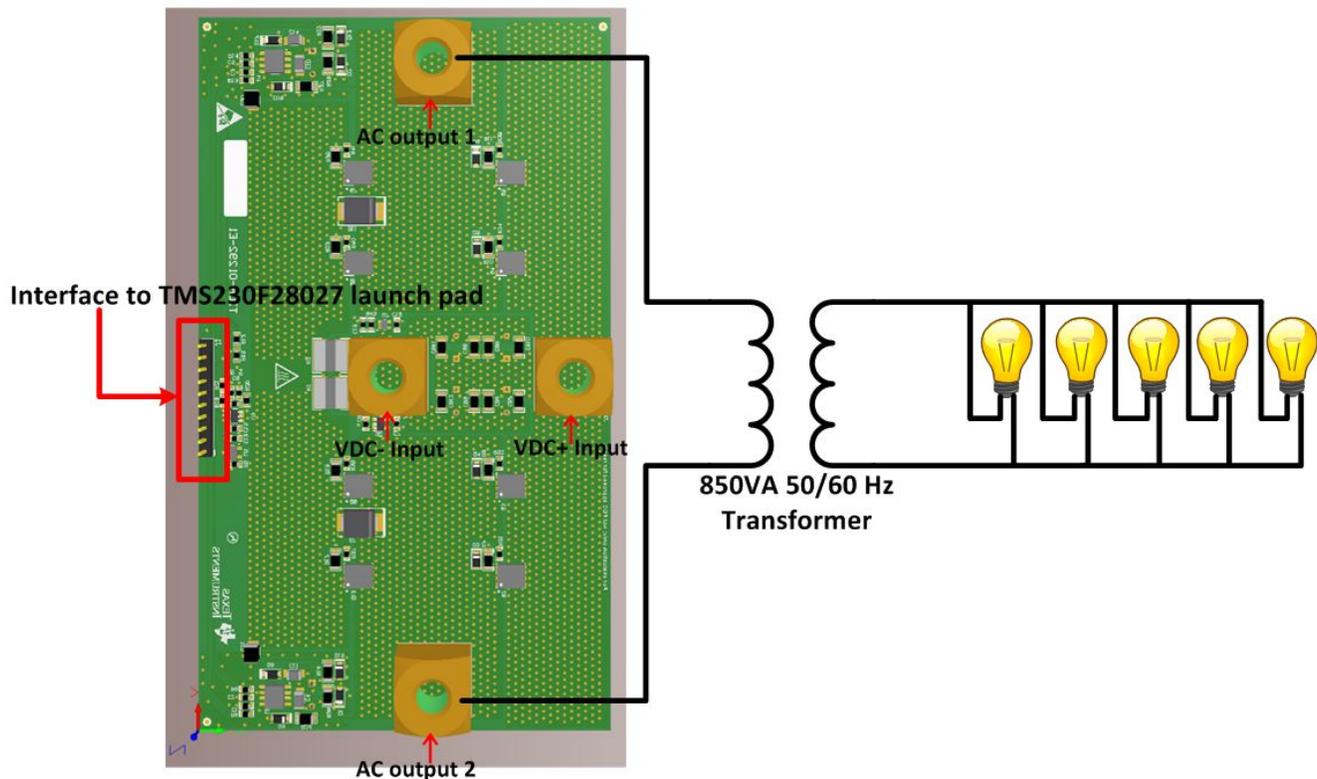

Figure 12. TIDA-01292 Test Setup

The details of the interface to the LaunchPad, connector J1 are as follows:

- Pin 1: Gate input for the high-side FET of left leg
- Pin 2: Gate input for the low-side FET of left leg
- Pin 3, 6, 7: Ground reference
- Pin 4: Analog output of current sense amplifier
- Pin 5: VDC sense output
- Pin 8: Temperature sense output
- Pin 9: Gate input for the high-side FET of right leg
- Pin 10: Gate input for the low-side FET of the right leg

3.2 Testing and Results

The TIDA-01292 design is tested with bulb loads and a 850-VA, 50-Hz transformer at the output.

3.2.1 Efficiency

The efficiency of the design is tested at various FAN speeds. Table 2, Table 3, and Table 4 show the efficiency of the design at 800-LFM, 600-LFM, and 400-LFM fan speeds with a 12-V battery input. The efficiency figures are for the TIDA-01292 board only and do not include the losses in the transformer.

Table 2. Efficiency With 12-V Battery Input and 800-LFM Fan Speed

V_{IN_RMS} (V)	I_{IN_RMS} (A)	P_{IN} (W)	V_{OUT_RMS} (V)	I_{OUT_RMS} (A)	P_{OUT} (W)	EFFICIENCY
11.88	14.58	139.54	9.03	21.04	138.66	99.37%
11.83	26.43	250.07	8.88	33.30	246.88	98.72%
11.78	38.30	357.56	8.73	46.93	350.11	97.92%
11.73	49.50	456.03	8.59	60.18	442.76	97.09%
11.71	55.02	504.55	8.51	66.90	487.51	96.62%
11.68	60.42	550.85	8.44	73.45	529.71	96.16%
11.66	65.52	594.07	8.37	79.73	568.84	95.75%
11.64	70.44	635.16	8.30	85.89	606.28	95.45%
11.63	72.85	655.61	8.27	88.85	623.86	95.16%
11.62	75.13	674.30	8.24	91.70	640.38	94.97%

Table 3. Efficiency With 12-V Battery Input and 600-LFM Fan Speed

V_{IN_RMS} (V)	I_{IN_RMS} (A)	P_{IN} (W)	V_{OUT_RMS} (V)	I_{OUT_RMS} (A)	P_{OUT} (W)	EFFICIENCY
11.94	4.14	21.37	9.22	15.14	21.31	99.72%
11.88	14.57	139.30	9.03	21.07	138.54	99.45%
11.83	26.42	249.88	8.88	33.29	246.56	98.67%
11.77	38.24	356.95	8.73	46.85	349.35	97.87%
11.73	49.42	455.98	8.59	60.12	442.26	96.99%
11.71	54.97	504.10	8.51	66.81	486.86	96.58%
11.68	60.33	550.21	8.44	73.36	529.13	96.17%
11.66	65.45	593.32	8.37	79.72	568.74	95.86%
11.64	70.38	634.89	8.30	85.77	605.15	95.32%
11.63	72.67	653.64	8.26	88.68	621.73	95.12%
11.62	74.91	671.90	8.23	91.47	638.22	94.99%

Table 4. Efficiency With 12-V Battery Input and 400-LFM Fan Speed

V_{IN_RMS} (V)	I_{IN_RMS} (A)	P_{IN} (W)	V_{OUT_RMS} (V)	I_{OUT_RMS} (A)	P_{OUT} (W)	EFFICIENCY
11.88	14.56	139.07	9.03	21.10	138.43	99.54%
11.83	26.39	249.67	8.88	33.27	246.21	98.61%
11.78	38.21	356.72	8.73	46.82	349.14	97.88%
11.73	49.36	455.35	8.59	60.02	441.45	96.95%
11.70	54.93	503.56	8.51	66.79	486.64	96.64%
11.68	60.23	549.20	8.44	73.26	528.42	96.22%
11.66	65.28	591.93	8.37	79.49	567.01	95.79%
11.64	70.30	634.54	8.30	85.61	604.31	95.24%
11.63	72.60	653.54	8.27	88.50	621.06	95.03%
11.62	74.87	672.21	8.23	91.33	637.45	94.83%

The design was also tested for efficiency at 10-V and 14-V battery inputs at a 600-LFM fan speed. Table 5 and Table 6 show the data for the 10-V and 14-V battery inputs, respectively.

Table 5. Efficiency With 10-V Battery Input and 600-LFM Fan Speed

V_{IN_RMS} (V)	I_{IN_RMS} (A)	P_{IN} (W)	V_{OUT_RMS} (V)	I_{OUT_RMS} (A)	P_{OUT} (W)	EFFICIENCY
10.06	2.03	13.74	7.78	6.77	14.30	104.05%
10.01	12.94	105.20	7.61	16.31	104.79	99.61%
9.96	23.84	190.11	7.47	28.90	187.55	98.65%
9.91	34.60	271.78	7.33	41.78	265.68	97.76%
9.87	44.65	346.19	7.20	54.05	335.75	96.98%
9.83	54.28	415.84	7.08	65.86	399.48	96.07%
9.81	58.54	445.90	7.02	71.18	426.65	95.68%
9.79	62.81	476.23	6.96	76.40	452.83	95.09%
9.78	66.72	503.00	6.90	81.36	476.59	94.75%
9.76	70.59	529.58	6.85	86.25	499.96	94.40%
9.74	75.15	560.71	6.79	91.95	525.88	93.79%
9.73	78.63	584.16	6.74	96.38	545.06	93.31%

Table 6. Efficiency With 14-V Battery Input and 600-LFM Fan Speed

V_{IN_RMS} (V)	I_{IN_RMS} (A)	P_{IN} (W)	V_{OUT_RMS} (V)	I_{OUT_RMS} (A)	P_{OUT} (W)	EFFICIENCY
13.91	10.06	43.62	10.92	41.55	37.66	86.34%
13.83	17.07	182.85	10.48	34.48	179.27	98.04%
13.76	29.37	320.80	10.33	42.63	315.12	98.23%
13.72	42.07	456.39	10.18	54.67	445.75	97.67%
13.69	48.94	527.83	10.09	61.99	513.55	97.29%
13.65	55.50	595.23	10.00	69.28	576.93	96.93%
13.63	61.78	658.97	9.92	76.51	636.25	96.55%
13.60	67.94	720.42	9.83	83.69	692.64	96.14%
13.58	73.77	778.77	9.75	90.58	744.19	95.56%

3.2.2 Functional Waveforms

Figure 13 and Figure 14 show the gate-to-source waveform of high- and low-side FET and drain-to-source waveform for the turnon and turnoff of the bottom FETs.

> **NOTE:** Channel 1 (Yellow): VDS_LS—Drain-source waveform of low-side FETs, 10 V/div
> Channel 2 (Green): VGS_LS—Gate-source waveform of low-side FETs, 10 V/div
> Channel 3 (Purple): VGS_HS—Gate-source waveform of high-side FETs, 10 V/div
> Time scale: 200 ns/div

Figure 13. Switching Waveform for Turnon of Bottom FETs
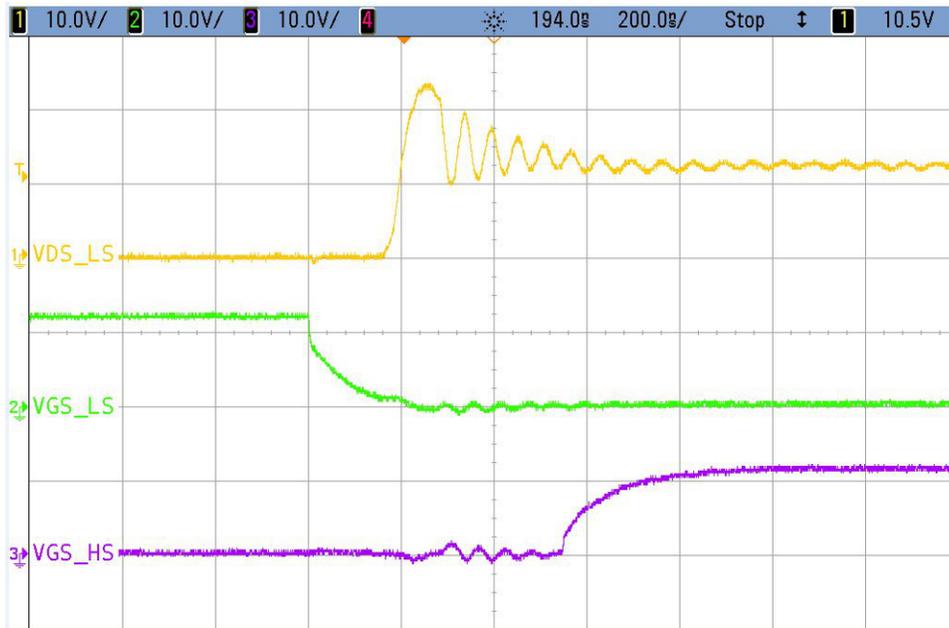

Figure 14. Switching Waveform for Turnoff of Bottom FETs

The TIDA-01292 design has a dead time of about 350 ns existing between the top and bottom FETs.

This design was also tested for inductive load where the primary winding of an auto-transformer was used as the inductive load. Figure 15 shows the filtered voltage and current output for the inductive load.
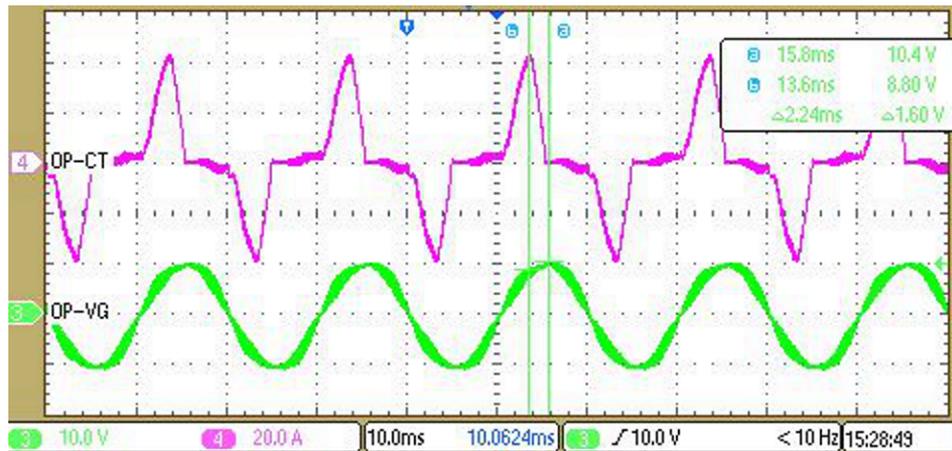

Figure 15. Output Waveform for Inductive Load

To further protect the FETs, this design has an overload and overcurrent protection algorithm where if the current hits the assigned peak, the PWMs shut off for 2 ms before starting again. Figure 16 and Figure 17 show the response during the overcurrent situation.

NOTE: Channel 2 (Purple): 220-V AC output voltage, 500 V/div
Channel 3 (Green) : Output of INA181, 2 V/div
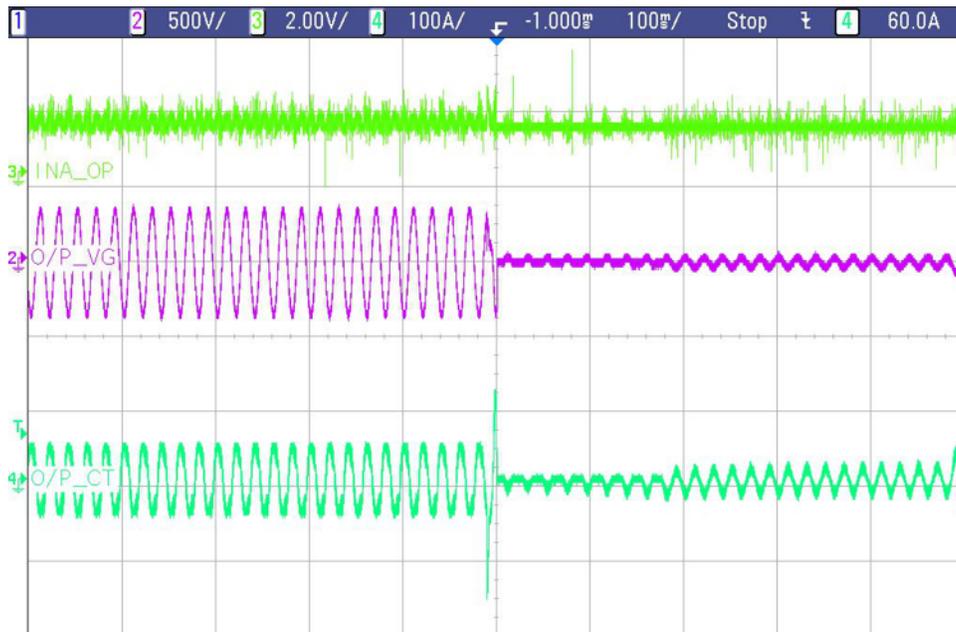Channel 4 (Teal): Output current, 100 A/div
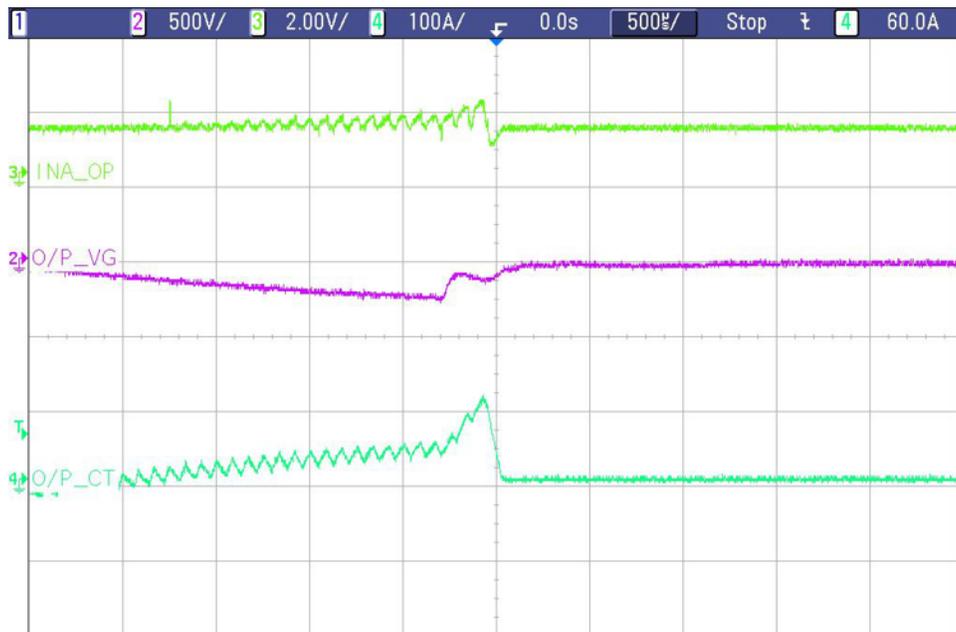

Figure 16. Overcurrent Protection

Figure 17. Overcurrent Protection (Zoomed)

3.2.3 Thermal Performance

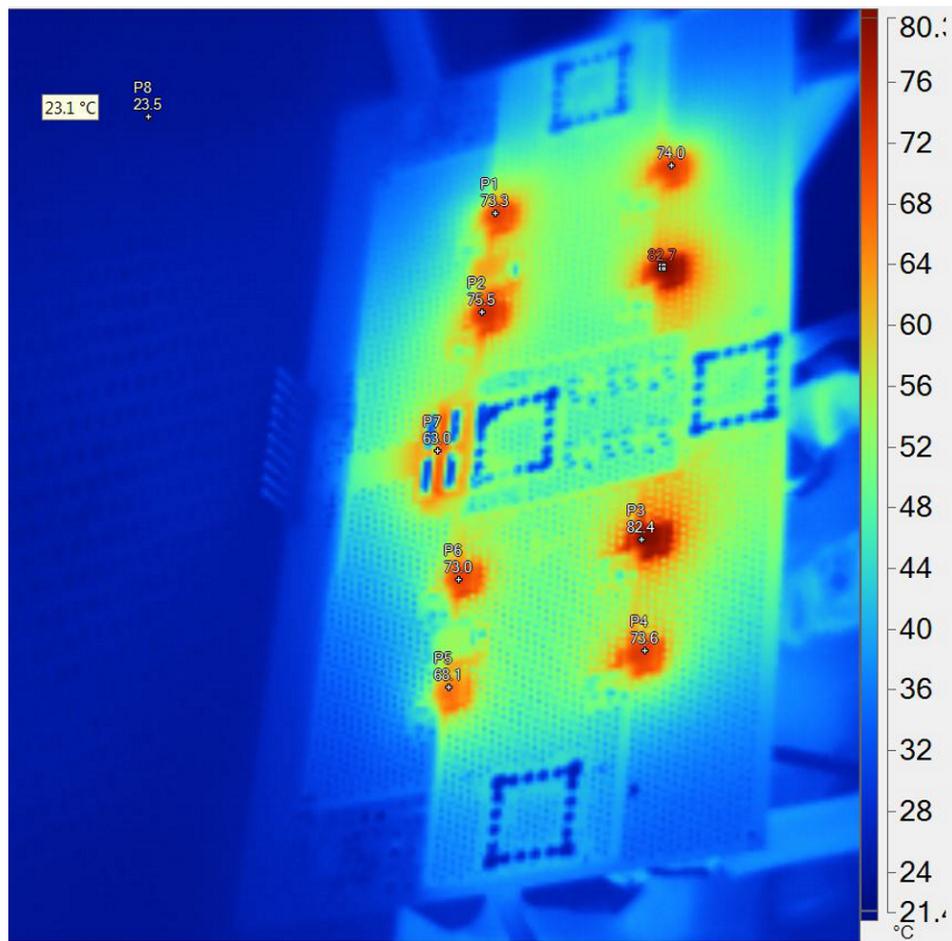Figure 18 shows the thermal performance of the design at full load, 12-V battery input, and 400-LFM fan speed.

Figure 18. Thermal Image at Full Load, 12-V Battery Input, and 400-LFM Fan Speed

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01292.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01292.

4.3 PCB Layout Recommendations

The optimum performance of high- and low-side gate drivers cannot be achieved without taking due considerations during the circuit board layout. Consider the following during the board layout:

- Connect low-ESR or ESL capacitors close to the device, between VDD and VSS pins to support the high-peak currents being drawn from VDD during turnon of the external MOSFET.
- Connect a low-ESR electrolytic capacitor between MOSFET drain and ground (VSS) to prevent large voltage transients at the drain of the top MOSFET.
- Minimize the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET to avoid large negative transients on the switch node (HS pin).
- Grounding considerations:
    1. The first priority in designing grounding connections is to confine the high-peak currents that charge and discharge the MOSFET gate into a minimal physical area. This current decreases the loop inductance and minimizes noise issues on the gate terminal of the MOSFET. Place the MOSFETs as close as possible to the gate driver.
    2. The second high-current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimize this loop length and area on the circuit board to ensure reliable operation.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01292.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01292.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01292.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01292.

5 Software Files

To download the software files, see the design files at TIDA-01292.

6   Related Documentation

1. Texas Instruments, *AN-2296 SM72295: Highly Integrated Gate Driver for 800VA to 3KVA Inverter*, Application Report (SNVA678)

2. Texas Instruments, *800VA Pure Sine Wave Inverter's Reference Design*, Application Report (SLAA602)

6.1   *Trademarks*

Piccolo, LaunchPad are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

7   About the Authors

NEHA NAIN is a systems engineer at Texas Instruments, where she is responsible for developing reference design solutions for the power delivery, industrial segment. Neha earned her bachelor in electrical and electronics engineering from the PES Institute of Technology (now PES University), Bangalore.

SHREENIDHI PATIL is an analog application engineer at Texas Instruments, where he is responsible for supporting various customers in North India. Shreenidhi earned his bachelor in electrical and electronics engineering from the RV College of Engineering, Bangalore.

7.1   *Acknowledgments*

Special thanks to **VIKAS CHOLA**, Field Applications Engineer, for his invaluable assistance in helping with the firmware and implementing various protections while testing this design.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (February 2018) to B Revision   **Page**

• Added *INA185*   7

Changes from Original (September 2017) to A Revision   **Page**

• Omitted note for Equation 14... 15

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated