Design Guide: TIDEP-01033

60GHz Integrated Radar Cost-Optimized Small Form Factor Reference Design

Description

This reference design with IWRL6432, targets applications for bill of material (BOM)-optimized millimeter wave (mmWave) with low cost and small form factor. This 60GHz mmWave design contains a form factor of 16mm x 33mm and provides 120˚ field of view, up to 15 meters pedestrian detection and angular resolution of 19˚. The radar sensor is developed with FR4 material using 4-layer PCB stack-up. This design guide addresses development of the design architecture and cost optimization steps. Two different antenna configurations with 3-dimensions and 2-dimensions detection capabilities are discussed in this document.

Resources

TIDEP-01033	Design Folder
IWRL6432	Product Folder
TPS6285020MDRLR	Product Folder
TLV75533PDRVR	Product Folder

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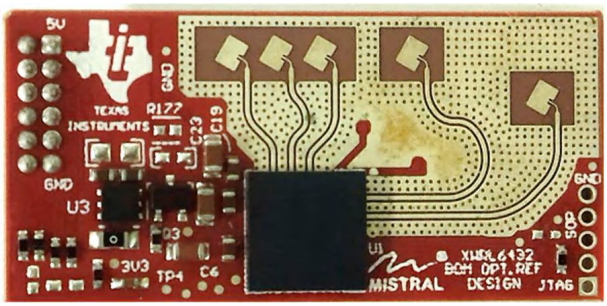
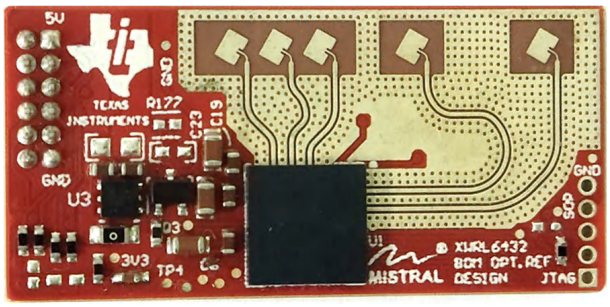
Features

- Low-power, low-cost, 57GHz to 64GHz mmWave sensor using the IWRL6432
- Design dimensions: 16mm x 33mm.
- Single 5V supply with on board power distribution network.
- Communication interfaces: UART, SPI, I2C (2-GPIOs and optional debug interface JTAG)
- Antenna features:
  - Single element patch antenna.
  - 120° field of view
  - Angular resolution of 19° in azimuth plane and 58° (for 2D antenna variant only) in elevation plane
  - Person detection up to 15 meters
- FR4 based 4-layer PCB stack up using only through hole vias for cost optimization.
- Simple, easy to integrate, one page schematic.

Applications

- Personal Electronics
- PC and notebooks
- Television
- Building Automation
- Lighting





1 System Description

Industrial applications equipped with radar in industrial building automation, parking area automation, personal electronics, lighting and other end-equipments provide quality of life and safety benefits in day to day living.

Frequency-modulated continuous-wave (FMCW) radars allow accurate measurement of range, angular resolution and relative velocity. Therefore, radars are widely used for presence detection, motion detection, tracking, and so on. An important advantage of radars over camera and light-detection-and ranging (LIDAR)-based systems is that radars are relatively immune to environmental conditions (such as the effects of dust and smoke). FMCW radars can work in complete darkness and also in bright light environments as radars are not affected by glare.

This reference design is a single chip, bill of material (BOM) optimized, small-scale, 60GHz mmWave design that is easy to integrate for the design's simplified schematic and only 4-layers layout. The antenna provides about 15 meters range for person presence or motion detection. The Antenna also provides ±60° field of view in azimuth and elevation planes. With smaller overall dimensions, the single element patch antenna design allows the reference design to fit into the bezel of personal electronic devices and other equipments. This is achieved using TI's IWRL6432 from the *60GHz low power mmWave* device family.

1.1 Terminology

FCCSP FCCSP stands for Flip Chip Chip-Scale Package. The term *flip chip* describes the method of electrically connecting the die to the package substrate. Flip chip microelectronic assembly is the direct electrical connection of face-down (or flipped) integrated circuit (IC) chips onto substrates, circuit boards, or carriers, using conductive bumps on the chip bond pads. The package of the IWRL6432 device used in the reference design is FCCSP.

Virtual antenna array For multi-transceiver systems, often called multiple-input-multiple-output (MIMO), each transmitter-receiver antenna pair forms a virtual antenna element. Each virtual element comes together to form a virtual antenna array. If the system consists of N-transmitters and M-receivers, the virtual antenna array contains M x N elements. Each of these elements can be considered as the number of receiver antennas for a single transmitter system. Since this array exists as a mathematical convenience, but not a physical reality, the array is called a *virtual antenna array.* This reference design uses a system of 2-transmiters and 3-receivers. Therefore, the virtual array for this design contains 6 elements.

BOM Bill of Materials

1.2 Key System Specifications

This reference design uses an on-board single element patch antenna design for the mmWave sensor. There are two different antenna designs depending on the spatial position of a transmitter antenna. One design gives a two-dimensional detection capability (1-D antenna variant) and another with three-dimensional detection capability (2-D antenna variant).

Table 1-1. Key specification

PARAMETERS	2-D Antenna Variant	1-D Antenna Variant	Description
Maximum range	15 meters	15 meters	Maximum range is the maximum distance that the RADAR can detect an object at.
Azimuth FoV	± 60 degrees	± 60 degrees	This represents the field of view the RADAR covers in azimuth direction.
Elevation FoV	± 60 degrees	± 60 degrees	This represents the field of view the RADAR covers in elevation direction.
Azimuth angular resolution	19 degrees	19 degrees	Angle resolution is the ability of a radar system to distinguish between two or more targets with the same range and velocity but different angles.
Elevation angular resolution	58 degrees	NA	Elevation angle resolution is only available for the 2D antenna variant.

2 System Overview

2.1 Block Diagram

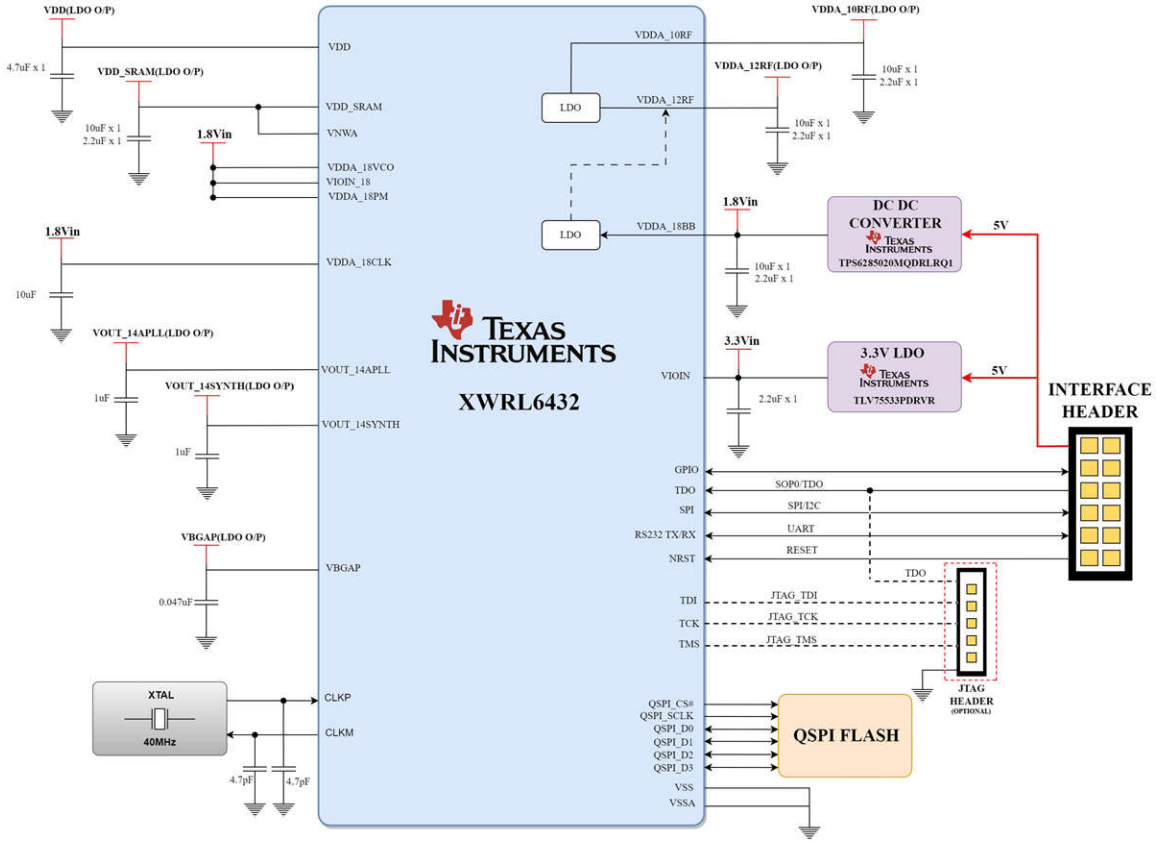


Figure 2-1. Functional Block Diagram

2.2 Highlighted Products

2.2.1 IWRL6432

The *IWRL6432* is TI's low-power low-cost radar that offers industry leading RF performance. IWRL6432 is an integrated single chip, low power, frequency modulated continuous wave (FMCW) radar sensor capable of operating in the 57GHz to 64GHz frequency band. The device is built with TI's low power 45-nm RF CMOS process and enables unprecedented levels of integration in an extremely small form factor. The device has three receivers and two transmitters with binary phase modulation for MIMO radar, TX Beam forming application as well as programmable back off support.

The single-chip radar transceiver comes with an integrated ARM Cortex M4F at 160MHz, an ARM Cortex M3F at 80MHz and a Radar Hardware Accelerator (HWA) at 80MHz for radar processing. The device supports IF bandwidths up to 5MHz.

The IWRL6432 is designed for low power, self-monitored, ultra-accurate radar systems in the industrial (and personal electronics) space for applications such as building or factory automation, commercial or residential security, personal electronics, presence or motion detection, and gesture detection or recognition for human machine interfaces.

2.3 Design Considerations

This reference design has been developed to target applications that require lower power consumption, lower BOM cost, as well as, smaller sensor size. Following are the main design considerations:

- **Low power consumption**
  The design consumes less power for applications like motion and presence detection, gesture recognition, and so on.
- **Low cost**
  The design has a reduced BOM (bill of material) cost.
- **Small overall size**
  The reference design has a small form factor to allow the same to be placed into space constrained environments such as TVs, monitor, and digital picture frames. In these and similar end equipments, the radar needs to be placed in the bezel region. Therefore, the antenna region must be optimized to fit into an area which nowadays can often be less then 2 cm in width.
- **Antenna FoV and angle resolution**
  The antenna design has a wide FoV and a good angular resolution that helps covering larger areas.

With these design considerations, the reference design has been developed with the following communication interfaces: UART, SPI, and I2C. This section describes how different components used in this design supports the requirements.

2.3.1 Reference Design Features

The reference design uses the IWRL6432's BOM optimized topology with onboard option to switch the IO voltages. The design includes two on-board supplies for 3.3V and 1.8V from the 5V external supply, a QSPI flash to store the application programs, a 40MHz XTAL as clock source and an antenna array of two transmitters and three receivers along with the radar device. Table 2-1 states the high level description of the reference design board features along with the elementary components:

Table 2-1. Features

Feature	Description
IWRL6432	Single-chip radar transceiver with integrated LO, with 3 RX and 2 TX, low power, low cost
2-TX and 3-RX antennas	Single element patch antenna with 120° FoV
Azimuth array	The antenna design forms a 6-element virtual array which allows 19° angular resolution
Elevation array (2D)	2-element virtual array – enabling 58-degree angular resolution
Elevation array (1D)	1 element virtual array
Clock source	40MHz crystal oscillator
QSPI Flash	Ultra-low power, 80MHz, 16M-Bit flash memory
Serial peripherals	SPI, I2C, UART, GPIO

2.4 IWRL6432 Reference Design Architecture

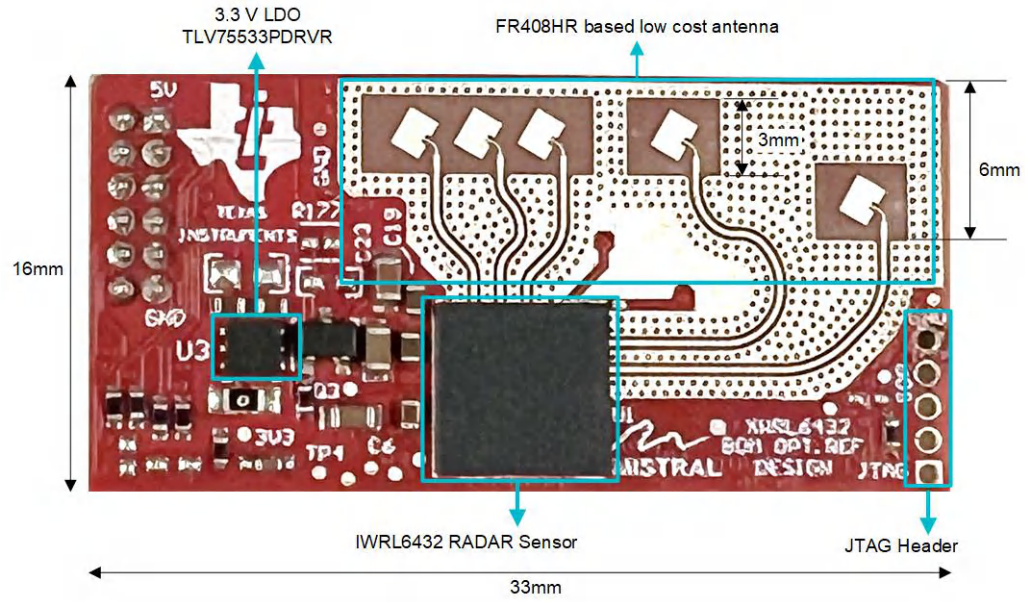


Figure 2-2. Board Labeling Front View: 2D Antenna

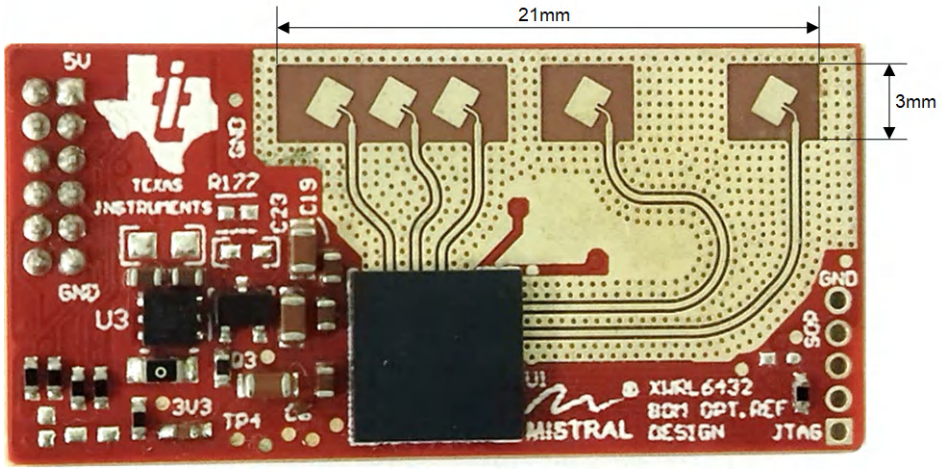


Figure 2-3. Board Labeling Front View: 1D Antenna

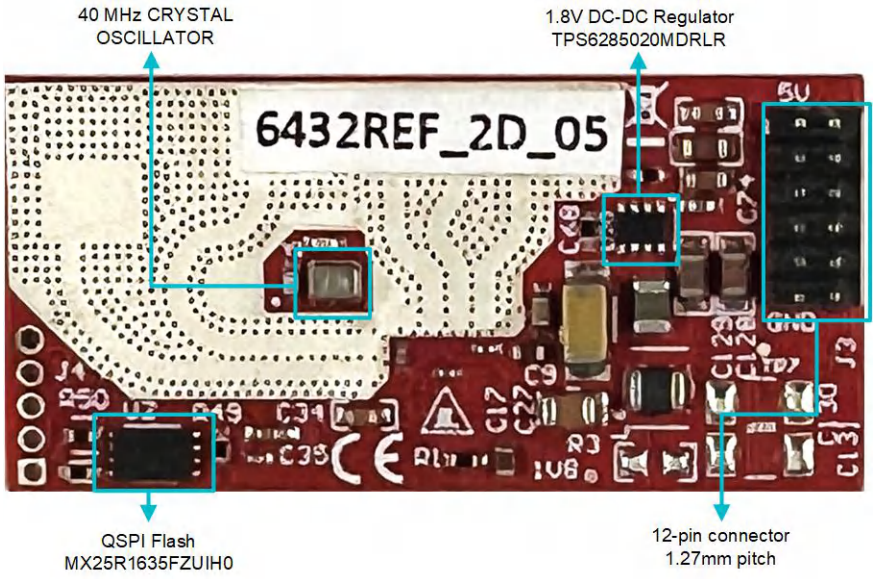


Figure 2-4. Board Labeling Back View

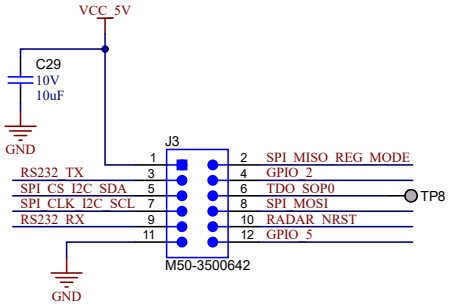


Figure 2-5. 12-Pin Connector Details

Primary radar SOC: IWRL6432.

Additional FLASH memory: MX25R1635F.

Power distribution network: TPS6285020M (1.8V supply), TLV75533P (3.3V supply)

Connector: 1.27mm pitch 12-pin male header. Figure 2-5 provides details about the connector.

Interface options: UART (RS232), SPI and I2C with 2 GPIOs and 1 optional JTAG interface.

Note

If JTAG needs to be used, SOP0 is not recommended to be directly connected to power lines (VIO or GND). In that case a pull-up pull-down network can be used. For more details on SOP circuits, please refer to the IWRL6432BOOST EVM design files.

This section explains the design architecture in terms of the on-board and on-chip power distribution network and the component selection. This discussion includes several cost reduction techniques that have been followed to optimize the BOM of the reference design.

2.4.1 IWRL6432: BOM Optimized Design

This subsection provides an overview of the radar device operation in terms of on-chip power distribution (different power topologies) and explains which power topology of the device has been selected for this reference design.

2.4.1.1 Device Power Topology

The IWRL6432 can be operated in four different power topologies based on availability of the power supplies to the device with power consumption and BOM (cost) trade-off.

There are two topologies: power optimized topology and BOM optimized topology for IWRL6432. At most, three different supply voltages can be provided to the IWRL6432: 3.3V, 1.8V and 1.2V. The topologies are determined depending on whether the 1.2V is externally supplied to the device.

In power optimized topology, the 1.2V supply is externally provided. Higher current is provided by 1.2V rail which reduces the overall power consumption. This is why the topology is called power optimized. In BOM optimized topology, the 1.2V is NOT externally provided to the device. The on-chip LDOs generate the 1.2V supply there-by eliminating the need of external 1.2V rail. This is why this topology is called the BOM (bill of material) optimized topology.

The device supports two IO voltages: 3.3V and 1.8V. Thus, each of the power topologies can be further subdivided into two configurations depending on the IO voltage. At start-up, the device senses the number of external voltages provided and adjusts the IOs and determines whether the internal 1.2V supplies need to be activated. This creates incredible application based flexibility in terms of power topology and IO configuration.

The following tables summarize the power delivery to internal subsystems in different IO voltage operations under different topologies.

Table 2-2. Power Supply Rails Characteristics: Power Optimized 3.3V I/O Topology

Supply	Device Blocks Powered From the Supply
3.3V	Digital I/Os
1.8V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC
1.2V	Core Digital and SRAMs, RF, VNWA

Table 2-3. Power Supply Rails Characteristics: Power Optimized 1.8V I/O Topology

SUPPLY	Device Blocks Powered From the Supply
1.8V	Digital IOs, Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC
1.2V	Core Digital and SRAMs, RF, VNWA

Table 2-4. Power Supply Rails Characteristics: BOM Optimized 3.3V I/O Topology

SUPPLY	Device Blocks Powered From the Supply
3.3V	Digital I/Os
1.8V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC

Table 2-5. Power Supply Rails Characteristics: BOM Optimized 1.8V I/O Topology

SUPPLY	Device Blocks Powered From the Supply
1.8V	Digital IOs, Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC

Note

In BOM optimized topology, digital cores, SRAM, RF and VNWA are all fed from the internally generated 1.2V rails.

In BOM optimized mode, the device can be operated using one rail (1.8V) or two rails (3.3V and 1.8V) depending upon 1.8V IO or 3.3V IO respectively.

In power optimized mode, the device can either be powered using two rails (1.8V and 1.2V) or with three rails (3.3V, 1.8V and 1.2V). During initial boot up, the device senses whether the external 1.2V supply is present or not and based on that determines if internally generated 1.2V LDOs are needed. With the 1.2V rail externally provided, the on-chip LDOs are not enabled in this case.

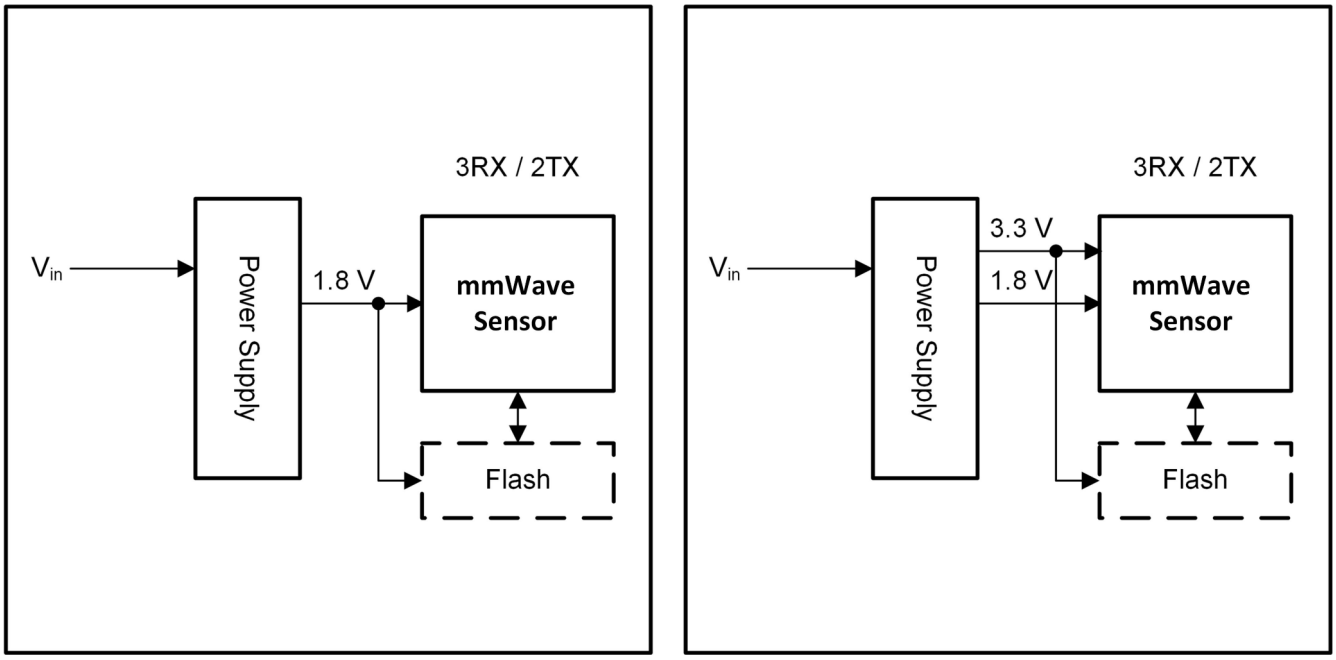


Figure 2-6. BOM Optimized Mode Power Management (Left: Single Rail 1.8V I/O Topology, Right: Two Rails 3.3V I/O Topology)

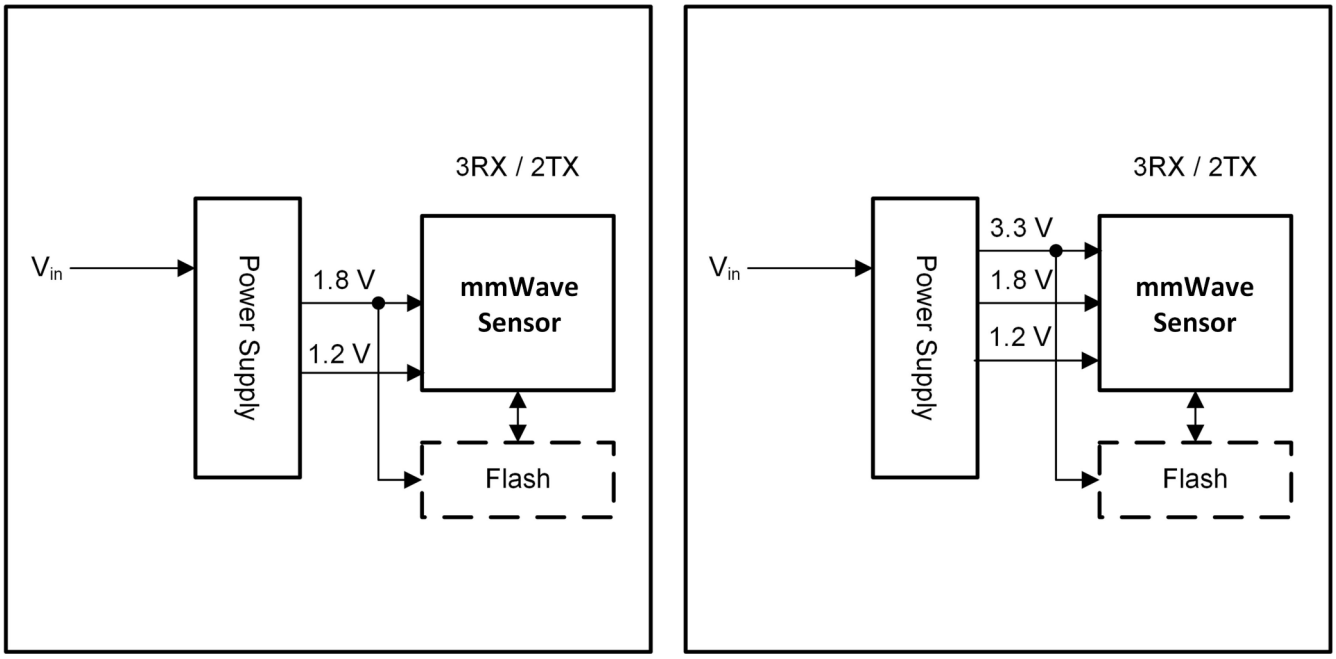


Figure 2-7. Power Optimized Mode Power Management (Left: Two Rails 1.8V I/O Topology, Right: Three Rails 3.3V I/O Topology)

This reference design uses the BOM optimized topology (Figure 2-6) with provision to switch between 3.3V and 1.8V IO voltage operations.

The BOM optimized topology consumes little more power compared to that in the power optimized topology but optimizes the design cost significantly. Therefore, to optimize power consumption as well as cost, BOM optimized topology is used. For the power consumption comparison between different topologies, please refer to *IWRL6432 Single-Chip 57- to 64GHz Industrial Radar Sensor*, data sheet, section *Typical Power Consumption Numbers*.

2.4.2 Power Distribution Network

The reference design requires 5V supply from an external source. The on-board low drop-out (LDO) regulator and DCDC regulator generate 3.3V and 1.8V respectively, from the single 5V external supply. The default IO voltage is 3.3V. Based on use-case requirements the IO voltage can be changed to 1.8V. In that case the 3.3V LDO output is disconnected from the device.

Figure 2-8 and Figure 2-9 show the power distribution network with 3.3V IO and 1.8V IO.

Note

Figure 2-8 and Figure 2-9 are only for representing the on-board power distribution to the device and power distribution inside the device for the BOM optimized topology. For functional block diagram please refer to Section 2.1.

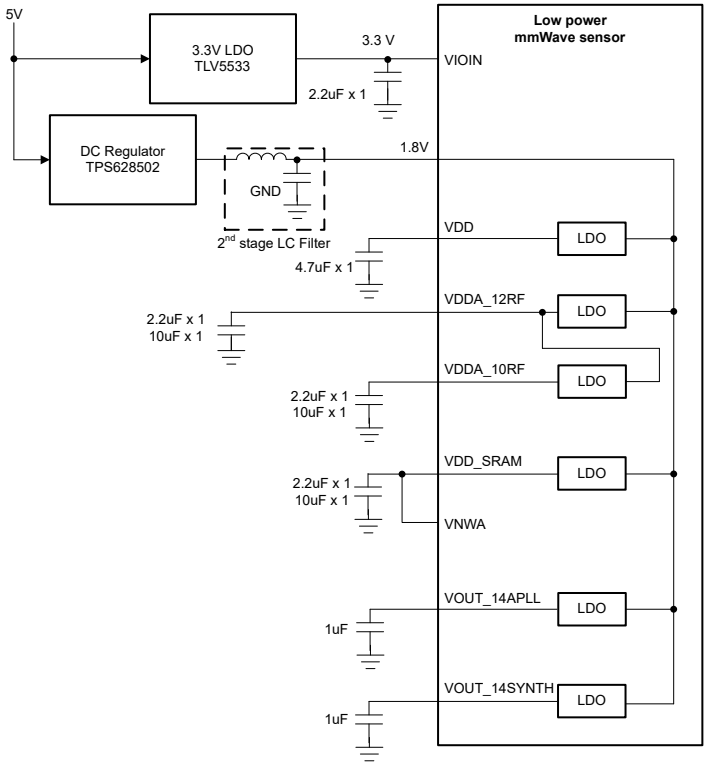


Figure 2-8. Power Distribution Network for 3.3V IO

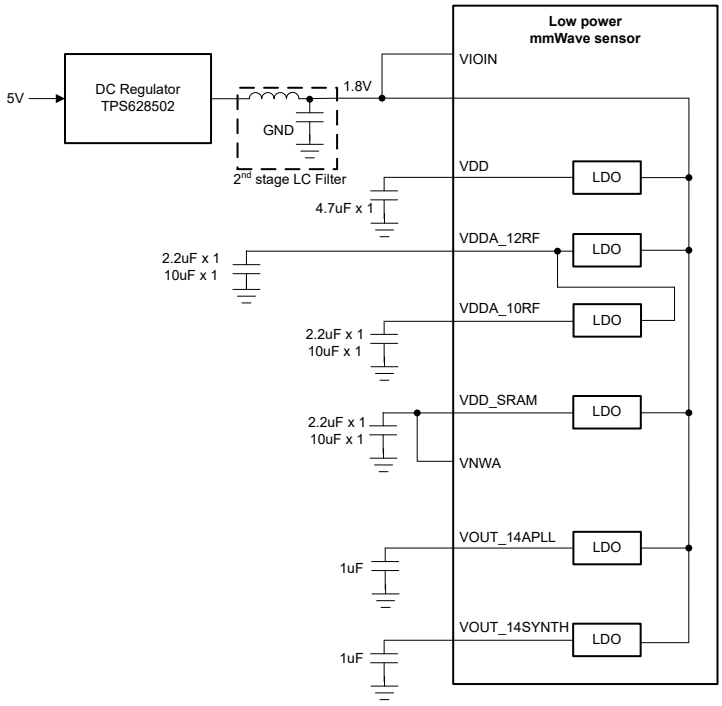
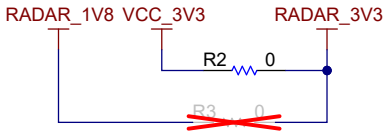


Figure 2-9. Power Distribution Network for 1.8V IO

Figure 2-10 shows the on-board provision for switching between 3.3V and 1.8V IO voltage.



Design Note: Default I/O operation is 3.3V,
for 1.8V I/O operation need to mount R3 & unmount R2

Figure 2-10. On-Board Provision for IO Voltage Switching

2.4.3 Internal LDOs

This section describes about the behavior of the internally generated power supplies. The IWRL6432 uses multiple on-chip LDOs (as depicted in Section 2.4.2) to generate power supply for different internal digital and RF blocks.

Table 2-6 lists down the specifications of the external capacitors for each of the internally generated power supply outputs.

Table 2-6. Recommended Values of External De-coupling Capacitor for the Internal LDOs

LDO output	Signal name	External capacitor	Capacitor Type
1.2V digital power supply	VDD	4.7uF	X7R
1.2V SRAM power supply	VDD_SRAM	2.2uF + 10uF	X7T, X7S
1.2V RF power supply	VDDA_12RF	2.2uF + 10uF	X7T, X7S
1.0V RF power supply	VDDA_10RF	2.2uF + 10uF	X7T, X7S
1.4V APLL power supply	VOUT_14APLL	1uF	X5R
1.4V SYNTHESIZER	VOUT_14SYNTH	1uF	X5R
Band gap	VBGAP	0.047uF	X5R

The IWRL6432 supports a low power mode of operation that can be controlled by the device configuration. When low power mode is ON, the device consumes even lesser power.

2.4.3.1 Enabling and Disabling Low Power Mode

The IWRL6432 is both programmable and configurable. Once the core is programmed with the application specific binaries, the front end needs to be configured by sending a configuration file with specific commands. The device's low power mode can be controlled by a specific command in the configuration file, that is *lowPowerCfg*. Details about configuration of IWRL6432 device are available in the MMWAVE-L-SDK.

To enable low power mode, the lowPowerCfg value needs to be "1," and to disable low power mode, the *lowPowerCfg* value needs to be "0."

2.4.3.2 1.4V Power Supplies: APLL and Synthesizer

The IWRL6432 has two on-chip 1.4V LDOs to supply the APLL and SYNTHESIZER. These two LDOs use 1.8V supply as input. Following are the characteristics of the APLL 1.4V supply and RF SYNTHESIZER 1.4V supply.

The following chirp configuration have been used to capture the waveforms.

- Refresh rate: 2Hz
- Number of chirps per frame: 32
- Burst period: 10ms
- Active chirp time: 4ms

2.4.3.2.1 APLL 1.4V

When low power mode is disabled (lowPowerCfg 0), the APLL supply stays at 1.4V always.

The APLL supply in low power mode (lowPowerCfg 1), stays at 1.4V initially, after the device power up and before configuration is sent. Once the configuration is sent the device starts chirping. During the active burst time of every frame the APLL supply rises sharply to and remains at 1.4V until the end of the active burst time. At the end of the active burst time, the supply drops to 0V until the next frame starts. Figure 2-11 and Figure 2-12 show the behavior of the 1.4V APLL supply, when the low power mode is enabled.

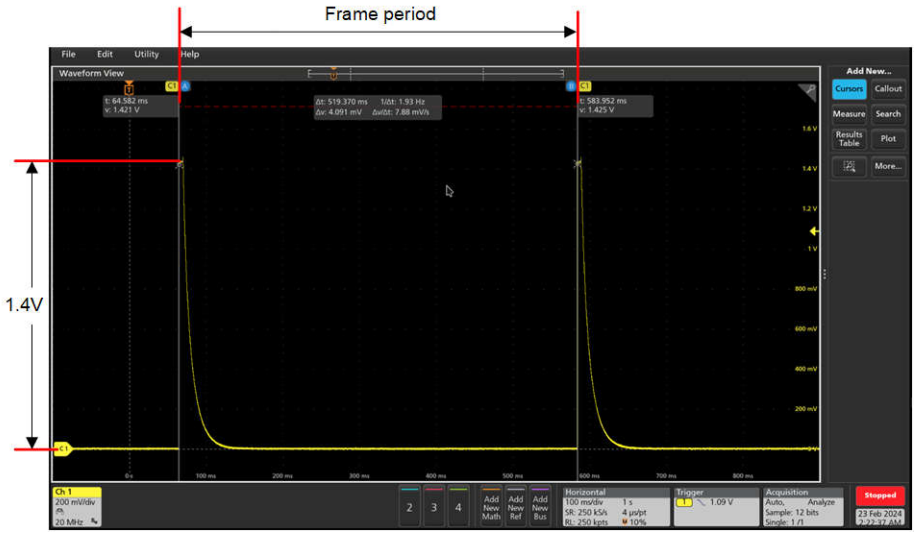


Figure 2-11. 1.4V APLL - Wide Window

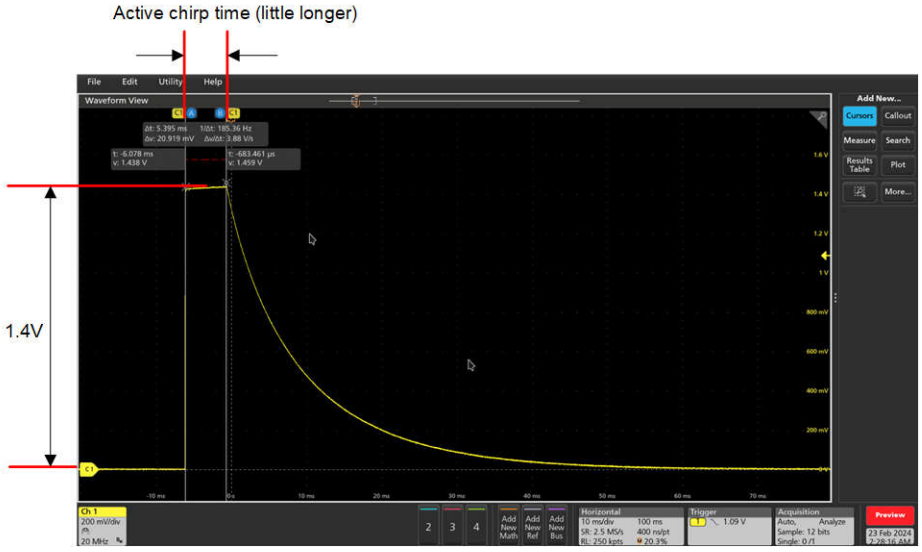


Figure 2-12. 1.4V APLL - Close Window

In low power operation the 1.4V APLL supply stays at 1.4V for a duration little longer than the active chirping duration, 5.4ms for this case, as the APLL needs to be turned off *after* the SYNTHESIZER turns off at the end of active chirping time. After that the supply drops to 0V until the next frame starts.

2.4.3.2.2 SYNTHESIZER 1.4V

The 1.4V SYNTH supply stays at 0V after the device power up, until the device starts chirping. The supply rises to 1.4V sharply once chirping starts, and stays at the same voltage level until chirping ends in every frame. After that the supply drops to 0V until the next frame starts. Figure 2-13 and Figure 2-14 show the behavior of the 1.4V SYNTH supply.

Irrespective of low power mode, the synthesizer supply displays the same behavior.

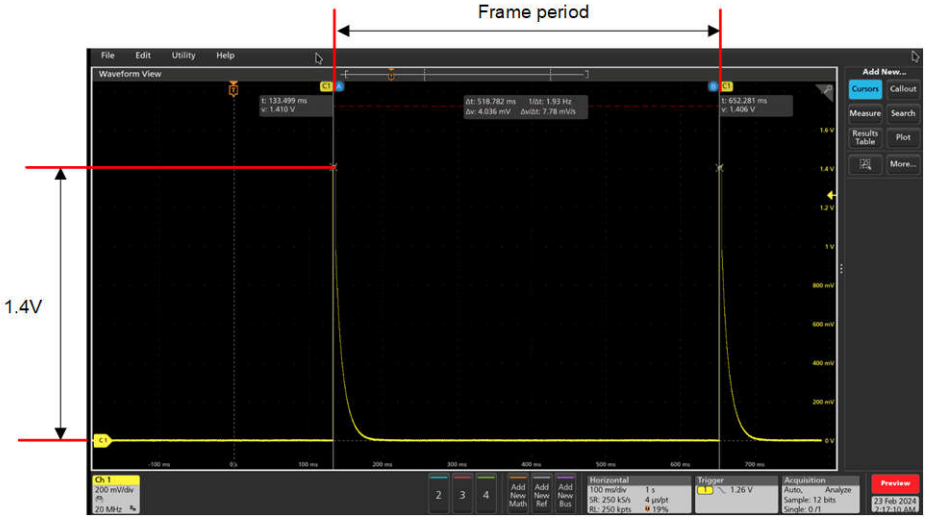


Figure 2-13. 1.4V SYNTH - Wide Window

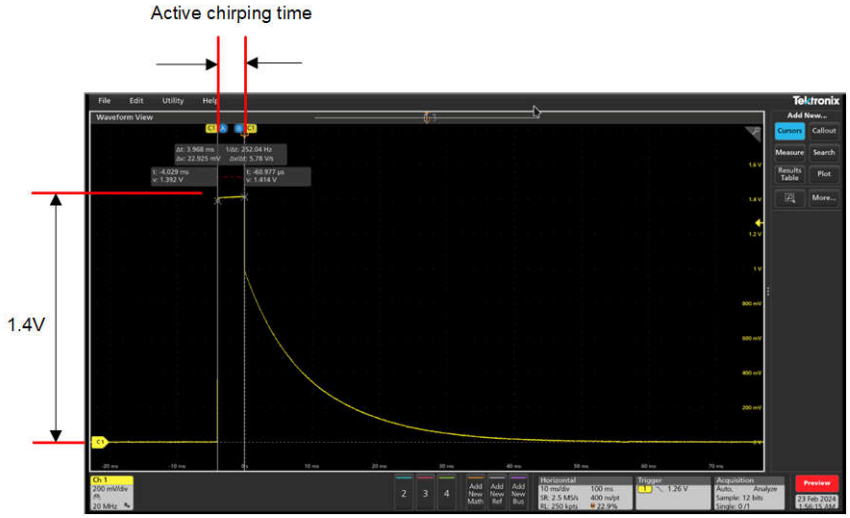


Figure 2-14. 1.4V SYNTH - Close Window

The 1.4V SYNTH supply in low power operation, stays at 1.4V for the active chirp duration, 4ms for this case. After that the supply drops down to 0V until the next frame starts.

2.4.3.3 1.2V Power Supplies

The IWRL6432 uses three on-chip 1.2V LDOs, in the BOM optimized topology, to supply the Digital blocks, SRAM, and RF sections. The 1.2V LDOs use external 1.8V as input. These LDOs are high bandwidth LDOs and require special care to control the output path parasitic elements to make sure the stability of the respective systems. The details regarding this are discussed in Section 3.5.

The following chirp configuration have been used to capture the waveforms.

- Refresh rate: 2Hz
- Number of chirps per frame: 32
- Burst period: 10ms
- Active chirp time: 4ms

2.4.3.3.1 RF 1.2V Supply

The RF sub-system of the IWRL6432, in BOM optimized mode is powered by an internal 1.2V LDO. When low power mode is disabled, the supply voltage always stays at 1.2V.

When low power mode is enabled, the RF supply line stays at 1.2V during the active chirping time and then falls slowly. In the deep sleep mode, the analog and RF sub-systems are powered down. The connected external decoupling capacitor, eventually discharges the supply line. Figure 2-15 shows this behavior of the 1.2V RF power supply.

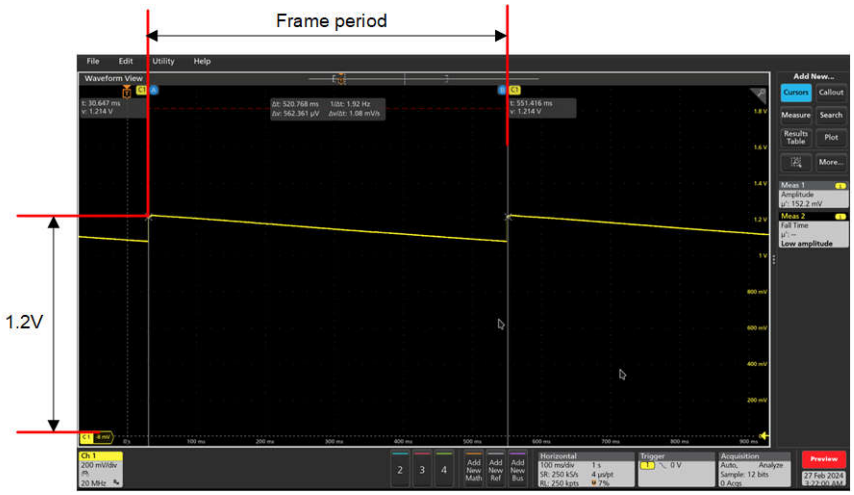


Figure 2-15. 1.2V RF Supply

Depending on refresh rate and or duty cycle, the voltage level for 1.2V RF can drop to any voltage level down to 0V. A slow discharge waveform is expected for this signal.

2.4.3.4 RF 1.0V Power Supply

The IWRL6432 uses a 1.0V supply line for certain RF and analog operations. This supply line stays at 1.0V for the active chirping time and then drops to 0V until the next frame starts. Similar to the other internal LDO outputs, the 1.0V supply also needs to be provided with required decoupling capacitors externally. This supply behaves the same irrespective of the device low power mode status.

Figure 2-16 and Figure 2-17 show the characteristics of the 1.0V RF supply.

The following chirp configuration have been used to capture the waveforms.

- Refresh rate: 2Hz
- Number of chirps per frame: 32
- Burst period: 10ms
- Active chirp time: 4ms

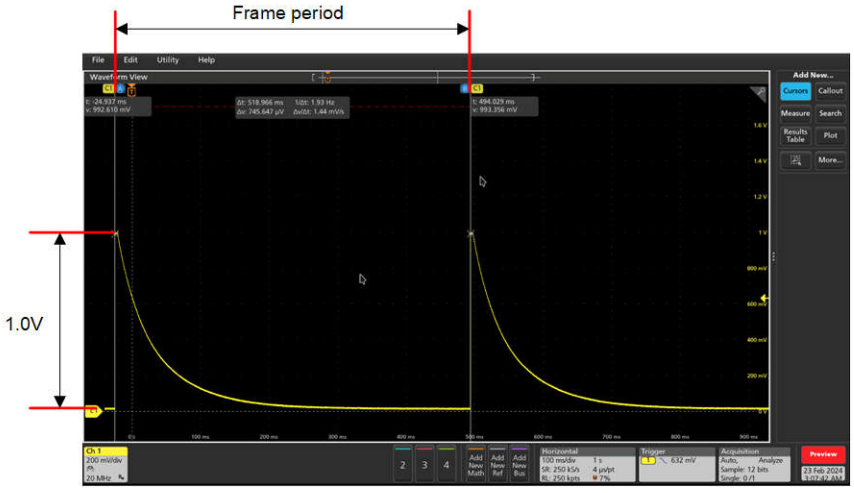


Figure 2-16. 1.0V RF Supply - Wide Window

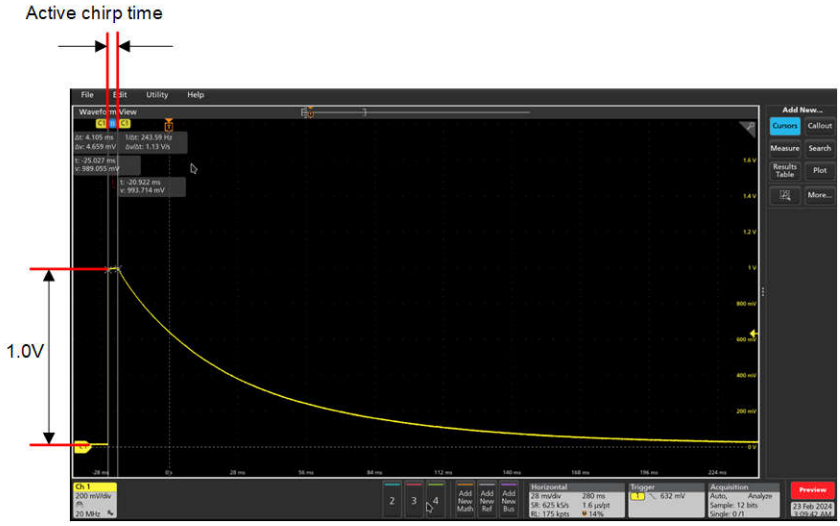


Figure 2-17. 1.0V RF Supply - Close Window

The 1.0V RF supply stays at 1V for the entire active chirping duration, 4ms, for this case. After that, the voltage drops to 0V until the next frame starts.

2.4.4 Component Selection

This reference design supports the radar device with a very limited set of components including: a 1.8V DCDC regulator, a 3.3V LDO, a QSPI flash, a 40MHz crystal, and an optimized number of resistors, capacitors, and inductors. The following sections demonstrate how the respective parts are selected based on device requirements.

2.4.4.1 1.8V DC-DC Regulator

The 1.8V supply is the an important power source for the radar device for any selected power topology. The digital subsystem along with RF subsystem, SRAM and analog front end are entirely powered by the 1.8V supply. If 1.8V IO voltage is selected, this becomes the single power supply to the device. Details on this have been discussed in Section 2.4.2.

TPS6285020M is TI's 2A (continuous), high efficiency, synchronous step-down DC-DC converter that has been used in this reference design to generate the 1.8V supply.

The peak current requirement from the 1.8V rail of the device needs to be met. Please refer to IWRL6432 data sheet, section "Peak Current Requirement per Voltage Rail" to get more details on this. Along with the current requirement, the DC-DC regulator needs to have *forced PWM mode* (or auto mode of switching) and *spread spectrum clocking (SSC)* features.

2.4.4.1.1 Need for Forced PWM Mode Switching

DC-DC switching converters use pulse width modulation (PWM) and or pulse frequency modulation (PFM) modes of switching. For light load conditions PFM switching scheme provides higher efficiency, however, injects a wide range of frequency components as ripple into the output. For higher load current requirement, PWM switching is required. Table 2-7 features the ripple specification for the radar device. This relates the very low ripple voltage that is allowable for the radar device.

Table 2-7. Noise and Ripple Specifications

FREQ (kHZ)	Noise Specification		Ripple Specification	
	1.8V(μV/√Hz)	1.2V (μV/√Hz)[1]	1.8V(mVpp)	1.2V (mVpp)[1]
10	6.057	44.987	0.035	1.996
100	2.677	26.801	0.760	2.233
200	2.388	28.393	0.955	3.116
500	0.757	9.559	0.504	1.152
1000	0.419	1.182	0.379	0.532

Table 2-7. Noise and Ripple Specifications (continued)

FREQ (kHZ)	Noise Specification		Ripple Specification	
	1.8V(μV/√Hz)	1.2V (μV/√Hz)[1]	1.8V(mVpp)	1.2V (mVpp)[1]
2000	0.179	1.256	0.153	0.561
5000	0.0798	0.667	0.079	0.297
10000	0.0178	0.104	0.017	0.046

(1) 1.2V noise or ripple specification is only for power optimized supply configurations. For BOM optimized topology 1.2V noise or ripple specification is not applicable.

Note

- Same 1.8V noise or ripple specification is applicable for the 1.8V supply in the BOM optimized topology
- For latest information on noise and ripple spec please refer to IWRL6432 data sheet.

To keep the ripple introduced by the switching below the specifications, a second stage LC filter is deployed at the output of the DC-DC regulator in the design. However, if PFM mode of switching is used, the lower frequency (in kHz scale) ripple can pass through the filter and enter into the system, violating the above specifications. Therefore, forced PWM switching mode is recommended where the pulse width is fixed across the whole time of operation. This keeps the switching frequency fixed and the harmonics can be easily filtered out in the second stage filters.

If overall system power consumption needs to be optimized in device's deep sleep conditions where typically light load conditions are followed, auto mode of switching can be enabled. In this mode, depending on light load conditions PFM mode of switching is enabled to reduce power consumption of the DC regulator. Auto mode and forced PWM mode of switching can be altered using the MODE pin of the DC regulator. The MODE pin of the DC-DC regulator can be controlled by the device through a GPIO in a way that the DCDC regulator switches between auto mode and forced PWM mode depending on the device's deep sleep entry and exit. To get more detail on this please refer to *Enabling PFM Mode for DCDC Converter*.

2.4.4.1.2 Importance of Spread Spectrum Clocking

Due to the periodicity of the switching signals, energy concentrates in one particular frequency and also in odd harmonics. This energy is radiated and therefore this is where a potential EMI issue arises. Radiated emission potentially causes emission failures. Conducted switching frequency causes issue is meeting ripple or noise spec and potentially cause ghost objects. Spread spectrum clocking (SSC) is a way to reduce both of the radiated and conducted emissions.

SSC is the variation of the frequency of a clock signal in a controlled way. In the frequency domain, the SSC reduces the peak amplitude of a clock signal by shifting the frequency. In other words, the energy of the clock is spread across small bandwidth with in the switching frequency.

Apart from this there is another reason for requiring SSC. The IF bandwidth of the IWRL6432 is 5MHz. The maximum switching frequency of the DCDC regulator is 4MHz. This means at least one harmonic of the switching frequency is going to fall inside the IF band. For this, the switching frequency needs to be as high as possible so that not more than one harmonic falls within the IF bandwidth. SSC is also required to spread the energy of that one harmonic falling inside the IF bandwidth to reduce the impact of the same.

Table 2-8 compares the device requirements for the 1.8V rail with TPS6285020M features.

Table 2-8. IWRL6432 1.8V Rail Requirements and Supporting Features of TPS6285020M

IWRL6432 Requirements for 1.8V Rail	TPS6285020M Features
Peak current requirement of 1.4A	2A output current (continuous)
Low quiescent current	15uA quiescent current
Forced PWM mode	Forced PWM or PFM/PWM operation using MODE
Spread spectrum clocking	Enable or disable spread spectrum clocking (SSC) feature
Higher Switching Frequency (3.5MHz - 4MHz)	Adjustable switching frequency: 1.8MHz to 4MHz
PGOOD feature	Power-good output with window comparator
High efficiency	>90% efficiency

Also, the TPS6285020M addresses minimum T_{ON} requirement for 5V input 1.2V output at 3.3MHz switching with SSC on.

The device has two control pins that determine the device operation mode. Following are the functionality and on-board configurations for the respective pins.

MODE or SYNC: When MODE or SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. When set high, the device operates in forced PWM mode.

On-board configuration: Pulled up to VCC to enable forced PWM mode.

COMP or FSET: This pin allows to set three different parameters.

1. Internal compensation settings for the control loop (two settings available)
2. The switching frequency in PWM mode from 1.8MHz to 4MHz
3. Enable or disable spread spectrum clocking (SSC)

A resistor from COMP or FSET to GND changes the compensation, the switching frequency and the SSC control.

On-board configuration: An 18kΩ resistor is connected from COMP or FSET to GND. This value of the resistor sets the device in the following configuration

1. Switching frequency set to 3.3MHz
2. Spread spectrum clocking (SSC) enabled
3. Compensation setting 2 for best transient response.

Note

1. A second stage LC filter is required at the DCDC output to match the noise and ripple specifications and to avoid conducted switching frequency related issues.
2. If switching frequency of the DC regulator is higher than the IF bandwidth (5MHz), the filter can be avoided.

2.4.4.2 3.3V Low Dropout Regulator

3.3V power supply is required to source the IO voltage of the device. The IO voltage can be configured to be 1.8V as well. In that case this source is not required.

The TLV75533P is TI's ultra-small, low quiescent current, low-dropout regulator (LDO) that sources 500mA with good line and load transient performance. This low dropout (LDO) has been used to source the 3.3V in this reference design.

The 3.3V is used to supply the device IOs. The current requirement from the 3.3V rail can go up to 90mA. For the low current demand on this rail, an LDO has been used instead of DCDC regulator. This further reduces the BOM cost. The following are a few selective features of the TLV75533PDRVR:

- Low IQ: 25µA (typical)
- Low dropout: 238mV (maximum) at 500mA (3.3V OUTPUT)
- Output accuracy: 1%
- PSRR: 46dB at 100kHz
- Active output discharge
- 2mm × 2mm package size

2.4.4.3 FLASH Memory

A QSPI flash memory is used to store the application image for the device.

The reference design uses the MX25R1635FZUIH0, a low cost and low power 16-MBIT flash memory that supports a wide range of input voltage of 1.65V-3.6V to support both of the 3.3V and 1.8V IO voltages of the reference design.

Table 2-9 compares the IWRL6432 device requirements for the flash memory and the supporting features of the MX25R1635F.

Table 2-9. IWRL6432 Device Requirements for the Flash Memory and the Supporting Features of MX25R1635FZUIH0

IWRL6432 Device Requirements for the Flash Memory	MX25R1635F Features
Clock frequency greater than or equal to 80MHz	Clock frequency 80MHz
Quad Enable (QE) bit for enabling QSPI data lines	Status register bit 6 is QE bit. Needs to be set to 1.
Supports SFDP command	Serial Flash Discoverable Parameters (SFDP) mode support
Wide input voltage range	1.65V-3.6V operation voltage
Low power consumption	Ultra Low Power Consumption

The reference design supports two different IO supply voltages of 3.3V and 1.8V. The wide range of input voltage support of the MX25U1632FZUI02 gives the reference design flexibility to perform in both the 3.3V and 1.8V power modes without need of replacement of the flash memory.

For specific use cases, where wide input voltage range is not required and the device only needs to be operated in 1.8V IO, MX25U1632FZUI02, operating in 1.65V to 2.0V can be used.

The Quad Enable (QE) bit of the status register (bit 6) needs be set to logic 1 to make the system function in four I/O mode. The value of QE bit in the status register can be written through write status register (WRSR) instruction.

Note

1. Refer to *Flash Variants Supported by the mmWave Sensor* for the flash variant compatibility.
2. Proper pull up is required for D2, D3 and CS lines.
3. If the data line lengths are larger (more than 4000mils), source termination resistors needs to be placed accordingly.

2.4.4.4 Crystal

The reference design uses Murata's XRCGE series 40MHz low cost, small size crystal as clock source. The part number for the crystal is XRCGE40M000FBAABR0. Following are some of the features of the crystal:

- Frequency 40.0000MHz
- ± 15ppm frequency tolerance
- Load capacitance 8pF
- ESR 50Ohms
- Size 2.0mm x 1.6mm

The following are the IWRL6432 device requirements for the crystal:

Table 2-10. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_P	Parallel resonance crystal frequency		40		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	–40		105	°C
Frequency tolerance	Crystal frequency tolerance[1] [2] [3]	–200		200	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
(3) Crystal tolerance affects radar sensor accuracy.

3 System Design Theory

3.1 Antenna Specification

3.1.1 Antenna Requirements

The reference design uses a single element patch antennas. For the 1D antenna variant, the maximum antenna region width is less than 3mm (Figure 2-3) and for the 2D antenna variant the maximum antenna region width is less than 5.5mm (Figure 2-2).

The smaller antenna width fulfills the antenna size requirements for the reference design.

3.1.2 Antenna Orientation

The antenna patches are oriented at an angle of 60° with respect to the vertical axis. The orientation has been optimized considering the isolation between adjacent antennas and the azimuth radiation. More rotation from the vertical axis results in better azimuth radiation, but increases antenna coupling. A 60° rotation provides an optimum trade off between antenna coupling and azimuth radiation.

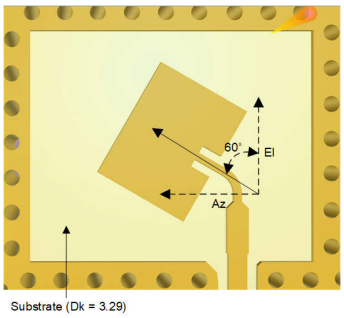


Figure 3-1. Antenna Orientation

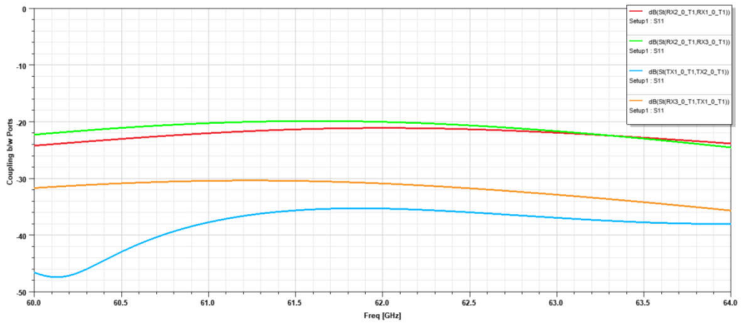


Figure 3-2. Isolation Between Antennas - 2D Antenna

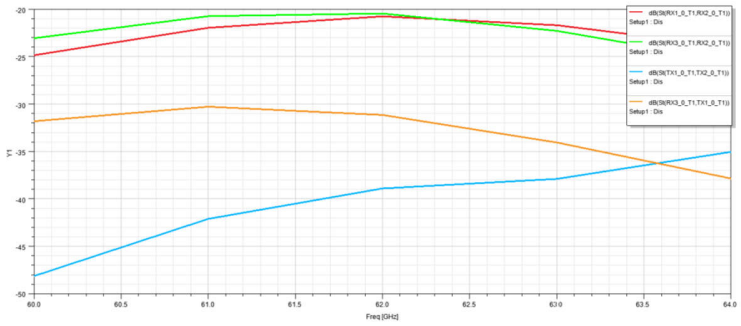


Figure 3-3. Isolation Between Antennas - 1D Antenna

Figure 3-1 shows the antenna patch orientation. The same antenna orientation has been considered for all the RX and TX antennas of both 1D and 2D antenna variants. With a larger component of power radiated along azimuth plane, the antenna yields a better performance in the azimuth plane. For the targeted application profile that includes presence detection, motion detection, vital sign monitoring etc., a better performance in the azimuth plane is anticipated.

Figure 3-2 shows the isolation between adjacent antennas, for example, RX1-RX2, RX2-RX3, RX3-TX1, and TX1-TX2. A minimum isolation of -20dB exists between the adjacent antennas given a rotation of 60°.

3.1.3 Bandwidth and Return Loss

Both reference design antenna variants see a -8dB bandwidth of 3.5GHz and a -10dB bandwidth of 3GHz. Figure 3-4 and Figure 3-5 display the return loss plot (in dB) across frequency (in GHz).

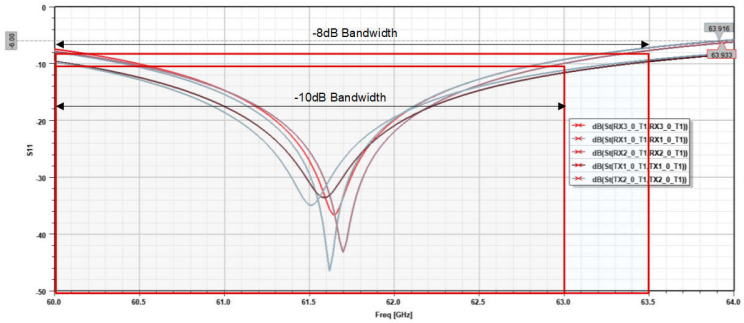


Figure 3-4. S11 Plot for 2D Antenna Variant

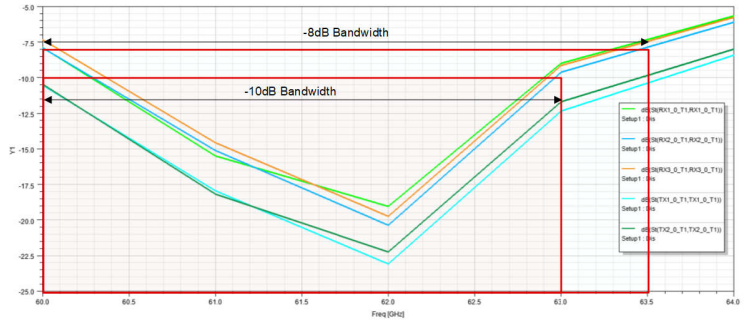
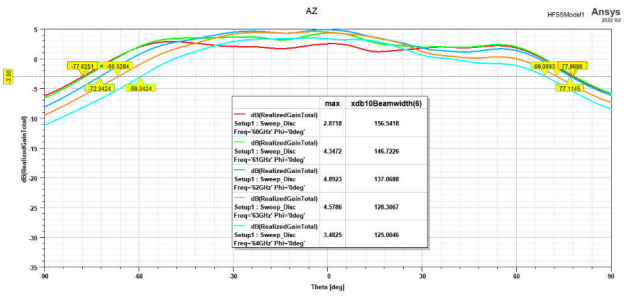


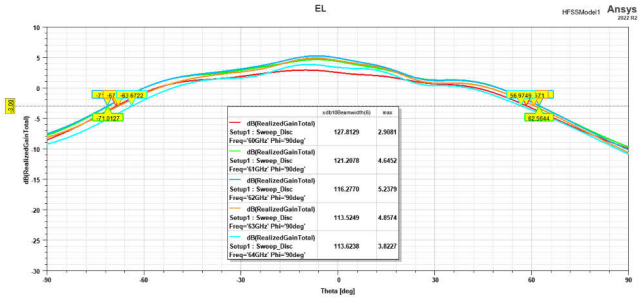
Figure 3-5. S11 Plot for 1D Antenna Variant

3.1.4 Antenna Gain Plots

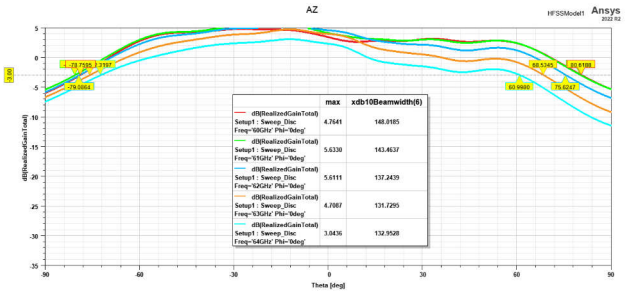
This section outlines the gain plots for all the three RXs and two TXs for both 1D and 2D antenna variants.



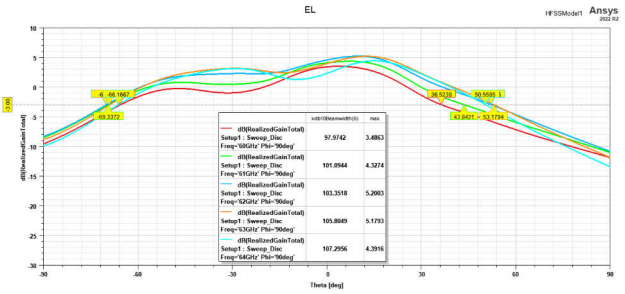
Realized Gain: RX1 (Azimuth plane)



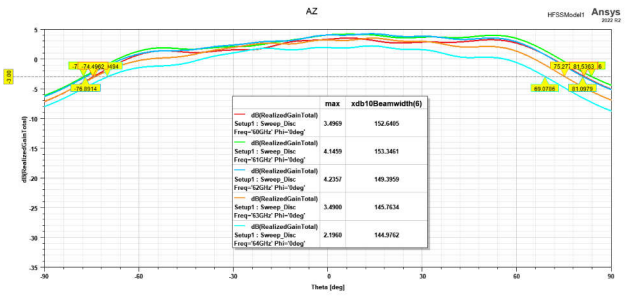
Realized Gain: RX1 (Elevation plane)



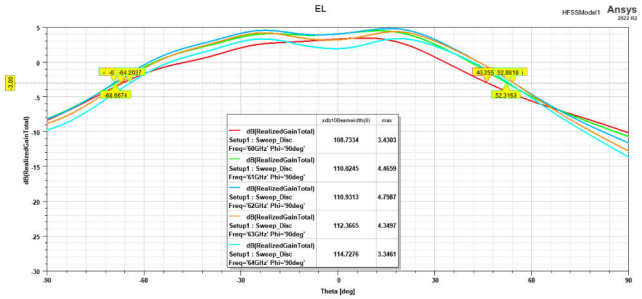
Realized Gain: RX2 (Azimuth plane)



Realized Gain: RX2 (Elevation plane)

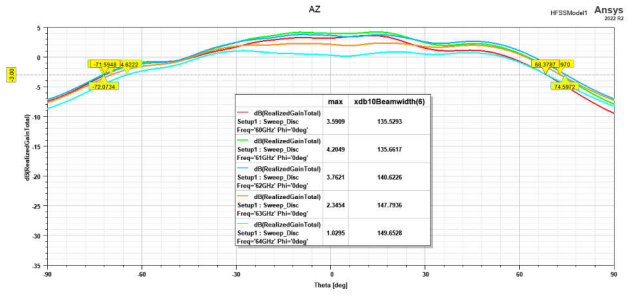


Realized Gain: RX3 (Azimuth plane)

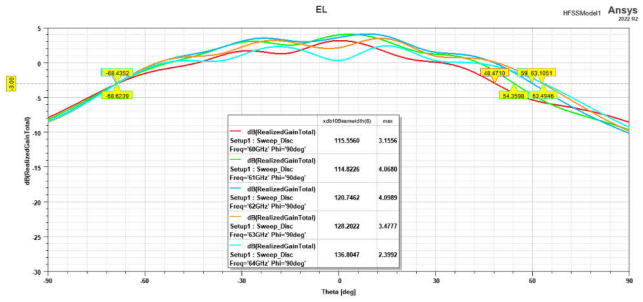


Realized Gain: RX3 (Elevation plane)

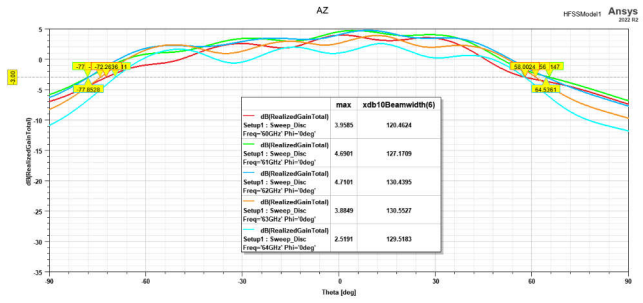
Figure 3-6. Realized Gain Plot for RX Antennas - 2D Antenna Variant



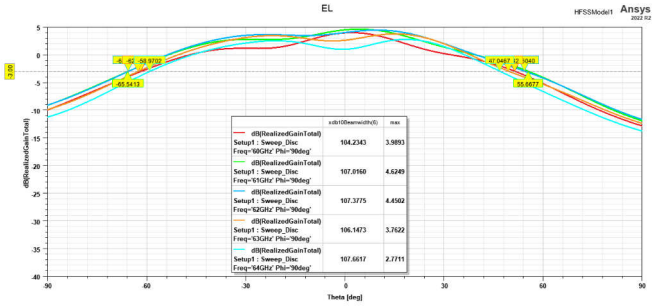
Realized Gain: TX1 (Azimuth plane)



Realized Gain: TX1 (Elevation plane)



Realized Gain: TX2 (Azimuth plane)



Realized Gain: TX2 (Elevation plane)

Figure 3-7. Realized Gain Plot for TX Antennas - 2D Antenna Variant

Realized Gain Plot for RX Antennas - 1D Antenna Variant

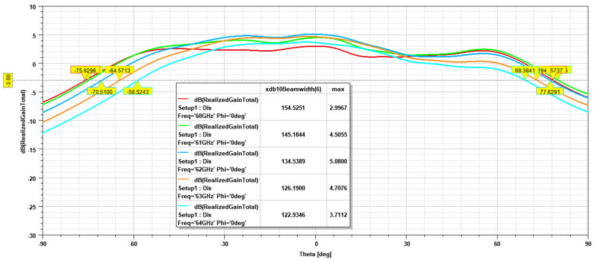


Figure 3-8. Realized Gain: Rx1 (Azimuth Plane)

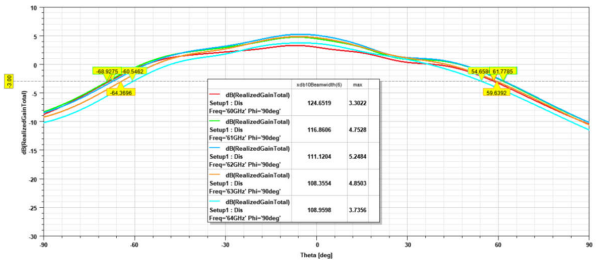


Figure 3-9. Realized Gain: Rx1 (Elevation Plane)

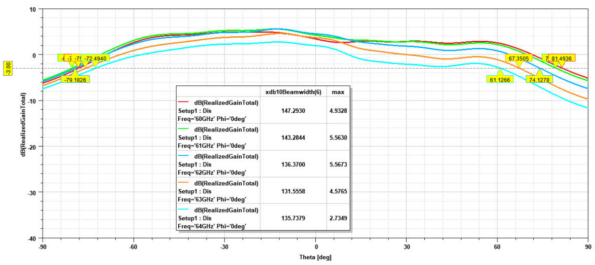


Figure 3-10. Realized Gain: Rx2 (Azimuth Plane)

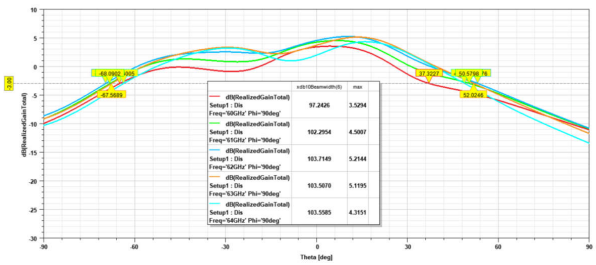


Figure 3-11. Realized Gain: Rx2 (Elevation Plane)

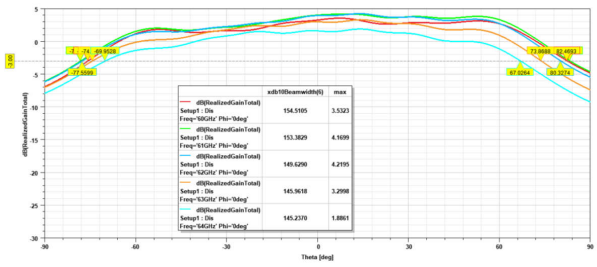


Figure 3-12. Realized Gain: Rx3 (Azimuth Plane)

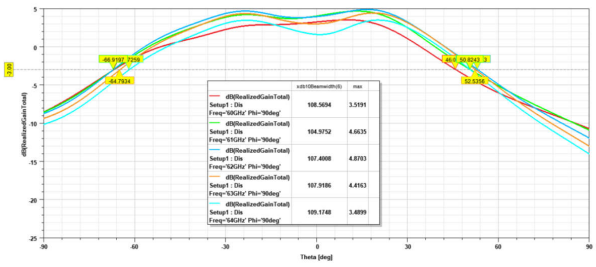


Figure 3-13. Realized Gain: Rx3 (Elevation Plane)

Realized gain plots for TX antennas - 1D antenna variant

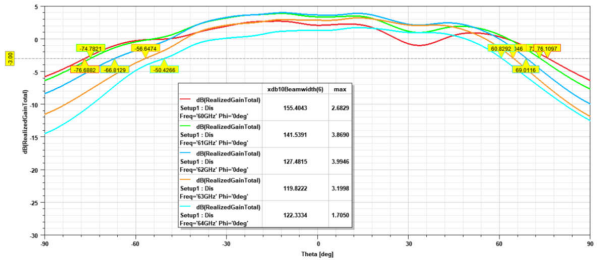


Figure 3-14. Realized Gain: Tx1 (Azimuth Plane)

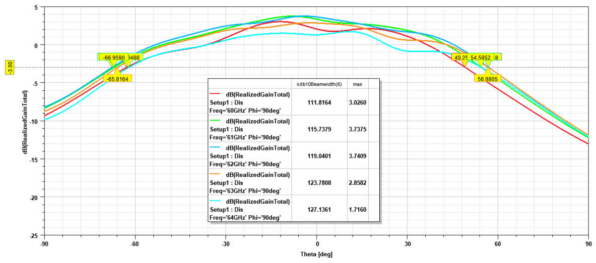


Figure 3-15. Realized Gain: Tx1 (Elevation Plane)

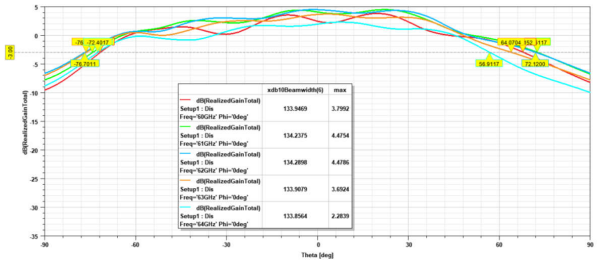


Figure 3-16. Realized Gain: Tx2 (Azimuth Plane)

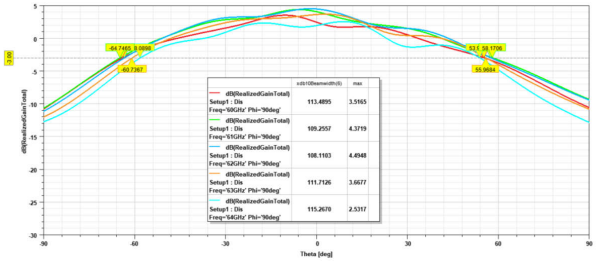


Figure 3-17. Realized Gain: Tx2 (Elevation Plane)

3.2 Antenna Array

The reference design uses a single-element patch antenna for the three receiver and two transmitter antennas. The antenna array has been defined in a way that the angular resolution is maximized in azimuth plane. As previously mentioned, this reference design has two variants, a 1D and a 2D sensing variant. This is achieved by changing the location of one of the TX antennas in relation to the other.

3.2.1 2D Antenna Array With 3D Detection Capability

The first variant has one Tx antenna placed λ/2 below the other TX antenna in the elevation plane, as shown in Figure 3-18. This antenna geometry has a two line, six element virtual antenna array, with six elements in the azimuth plane and two elements on the elevation plane as shown in Figure 3-19. This antenna variant is capable of 3-dimension detection: the azimuth, elevation and distance.

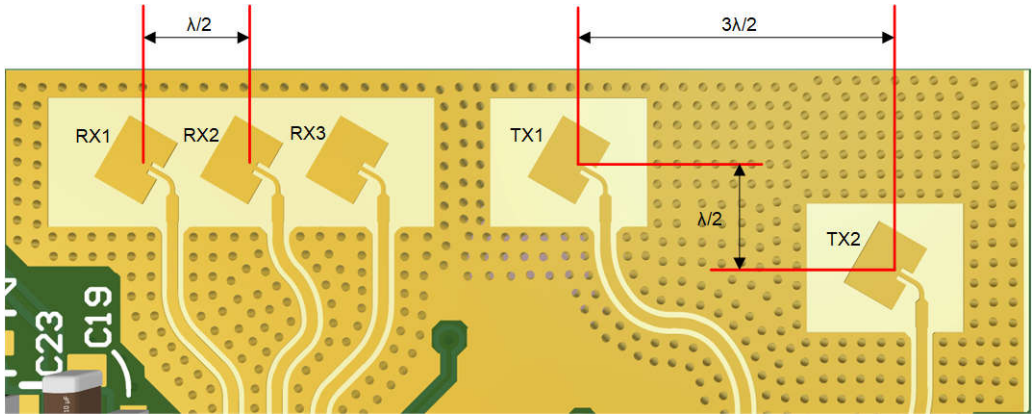


Figure 3-18. 2D Antenna Patch Array Geometry

Figure 3-19 shows the geometry of the virtual antenna array with each index depicting multiplication factor for λ/2. Position 0, 1, and 2 represents placement of virtual antenna originated from combination of all 3 Rx (Rx1, Rx2, Rx3) and Tx1. Position 3, 4, and 5 represents placement of virtual antenna originated from combination of all 3 Rx (Rx1, Rx2, Rx3) and Tx2.

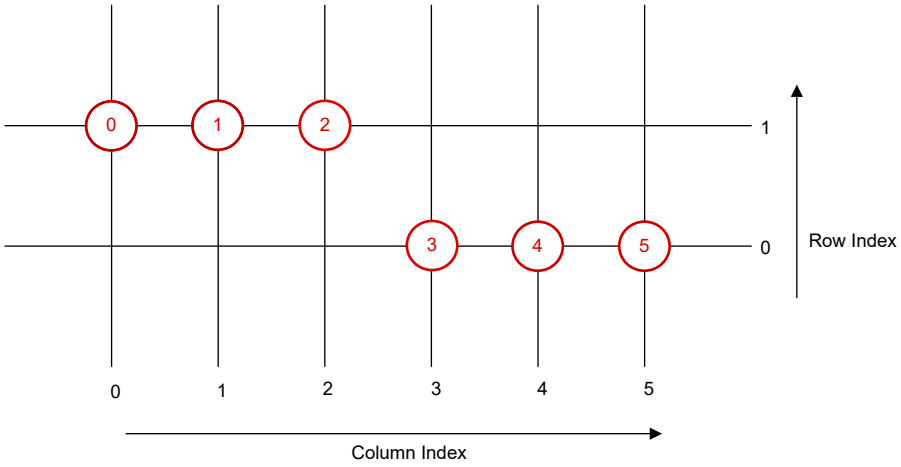


Figure 3-19. 2D Antenna - Virtual Array

The virtual antenna forms a two dimensional array with six elements in the azimuth and two elements in the elevation. The six elements in the azimuth direction, like the 1D antenna variant, yields an angular resolution of 19 degrees across azimuth. However, the 2D antenna variant having two elements in the elevation direction, unlike the 1D antenna variant, yields an angular resolution of 58 degrees across elevation. This enables the 2D antenna variant of the reference design.

3.2.2 1D Antenna Array With 2D Detection Capability

The 1D antenna variant has all the Tx and Rx antennas in one single line. Two Tx antennas separated by 3λ/2, three Rx antennas, all separated by λ/2 as shown in Figure 3-20. This geometry generates a single line six element virtual array. Although in azimuth direction the virtual array has six elements, in elevation direction the array has one element as shown in Figure 3-21, resulting in a 2-dimension detection capability for the antenna variant in only azimuth plane. This means that targets cannot be localized in the elevation and cannot be resolvable in the elevation. That objects still in the FOV can all be projected into the 2D space.

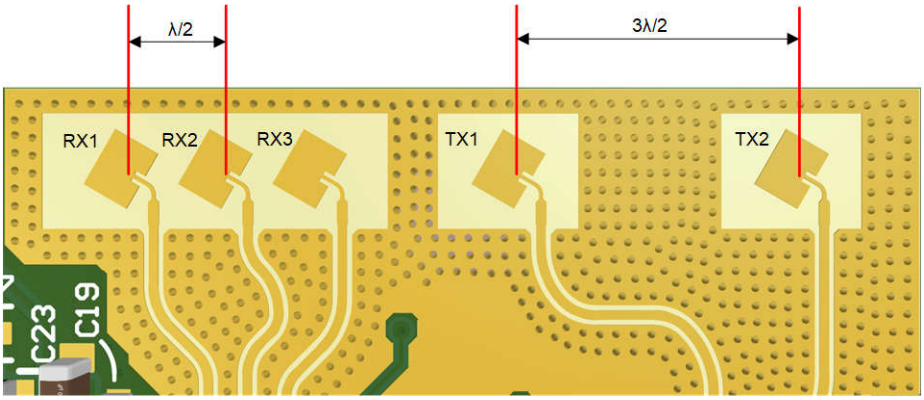


Figure 3-20. 1D Antenna Patch Array Geometry

Figure 3-21 shows the geometry of the virtual antenna array with each index depicting spacing factor of λ/2. Position 0, 1, and 2 represents placement of virtual antenna originated from combination of all 3 Rx (Rx1, Rx2, Rx3) and Tx1. Position 3, 4, and 5 represents placement of virtual antenna originated from combination of all 3 Rx (Rx1, Rx2, Rx3) and Tx2.

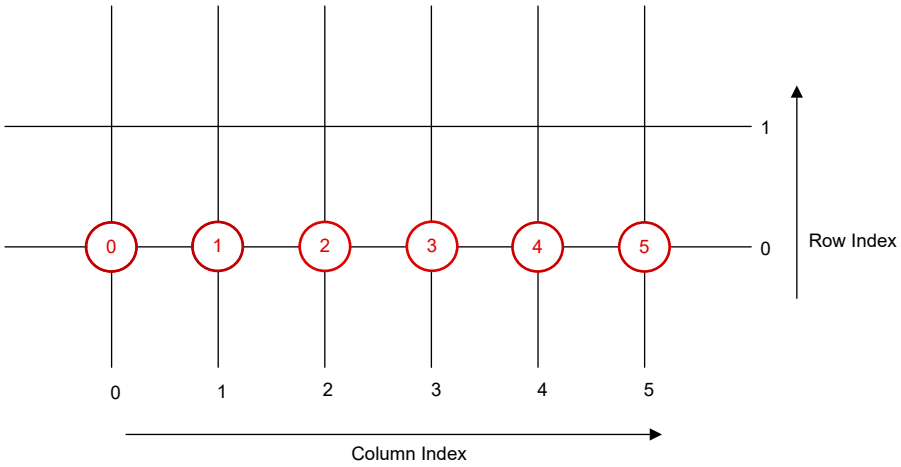


Figure 3-21. 1D Antenna - Virtual Array

The virtual antenna forms a single line with six elements. Six elements in azimuth direction yields an angular resolution of 19 degrees. Although the 1D antenna has poor angular resolution in the elevation direction, reason having a 2D detection capability in the azimuth direction only.

3.3 PCB

The reference design uses a 4-layer stack-up for the PCB. The stack-up is extremely critical for antenna performance. This section elaborates on the existing stack up and a couple of layout related cost reduction techniques implied.

Figure 3-22 shows the stack-up details of the PCB.

Lyr	Lyr Type	Image	Foil Wt	Thk (mm)	Cu Thk (mm)	Er	Generic Name	Construction		Material Family	TG	
tsmp				0.020		3.9						
1	Sig		0.5	0.127	0.040	3.26	0.5OZ +plating Core 5mil 1/0.5 oz RTF	2X1067		FR408HR	185	
2	Mix		1		0.031							
				0.258		4.25	Prepreg	2116		370HR	170	
						4.25	Prepreg	2116		370HR	170	
3	Mix		1	1.016	0.031	4.4	Core 40mil 1/0.5 oz RTF	5x7628		370HR	170	
4	Sig		0.5		0.040		0.5OZ +plating					
bsmp				0.020		3.9						
		Over Solder mask on plating		1.583								

Figure 3-22. PCB Stack-Up

The antenna resides on the top layer (Lyr 1) of the PCB. This layer has FR408HR dielectric material. Below are a few critical properties of the dielectric:

1. The dielectric has 2 x 1067 (dual ply) spread glass construction. This structure helps reducing the glass weave effect that helps reducing losses.
2. Thickness of the dielectric is 5mils (127um). This thickness value is adjusted for impedance matching.
3. The Dk value of the dielectric is 3.3
4. This is core material.

Note

- The dielectric thickness must not be altered as this can cause impedance mismatch and more reflection of the radiated power.
- Pre-preg material must not be used for the antenna layer. For the layers in between other than antenna, pre-preg can be used.

Grounded coplanar waveguide (GCPW) transmission lines have been used to carry the RF signals to the antenna. Below are some critical considerations for the antenna layer and the ground layer followed by the same:

1. Finished copper thickness on the antenna layer is 40um.
2. Ground plane (below the antenna plane, Layer 2) thickness is 1oz (0.5oz can also be used if 1oz is not available).
3. PCB surface finish is OSP or immersion silver.

Note

ENIG surface finish is NOT recommended as this can potentially cause higher insertion losses for the mmWave frequency range.

The overall PCB thickness of the reference design is 1.6mm.

Note

We recommend using the TI stack-up as is. If a different stack-up is desired, 3D EM solvers are recommended and antenna optimization needs to be done.

Following are some of the techniques implied to reduce the cost of PCB design:

3.3.1 Via-in-Pad Elimination

Via-in-pad is completely eliminated and dog bone fanout is chosen for BGA fanout. This activity reduces cost of PCB fabrication as compared to via in pad and via filling, plating process. Figure 3-23 shows the cutout image of the layout portraying the BGA fanout:

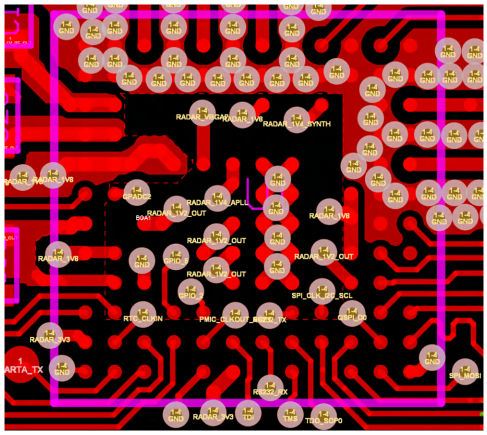


Figure 3-23. No Via-in-Pad for BGA Fanout

3.3.2 Micro-Via Process Elimination

The package to PCB transition for the reference design is performed without via-on the-pad, micro-via and blind-via. All the vias in the reference design are through-hole vias. This activity reduces the PCB design cost. Figure 3-24 shows a clip from the layout with through-hole vias. All other vias are also through-hole (1-4) vias.

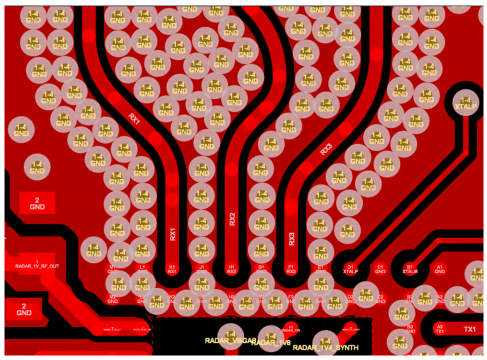


Figure 3-24. Through Hole Vias (From Layer-1 to Layer-4)

With these two activities, the overall cost of the PCB has been significantly reduced for the reference design.

3.4 Configuration Parameters

Once the core of the IWRL6432 is programmed with the application specific binaries, the front end needs to be configured by sending a configuration file with specific commands. Details about each of these commands can be found inside the MMWAVE-L-SDK. In this section, a few specific commands have been discussed that varies with different antenna designs.

3.4.1 Antenna Geometry

As discussed in Section 3.2, different spatial positioning of the Tx and Rx antennas can produce different virtual antenna arrays. The relative position of these virtual antenna elements are necessary for determining the angle of arrival of the target objects. For this reason, the internal processing chain of the radar device needs to have the virtual antenna geometry information to provide angle information about the detection space.

This particular information, in a certain format, can be fed to the processing chain with the configuration file. There is a specific field in the configuration file called *antGeometryCfg*, where the antenna geometry information can be stated. Following is the format for the inputs of this command and an example of *antGeometryCfg* entries for the two antenna configurations associated with this reference design.

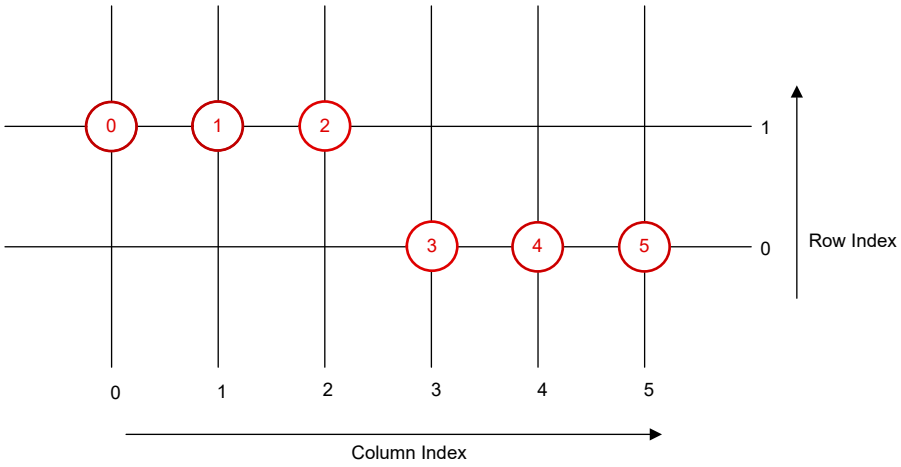


Figure 3-25. Virtual Antenna Index for IWRL6432FCCSP Reference Design 2D Antenna Variant

Antenna geometry command for 2D antenna variant: **antGeometryCfg 1 0 1 1 1 2 0 3 0 4 0 5 2.418 2.418**

This line can be pasted in the configuration file.

Example configuration for motion detect:

```
sensorStop 0
antGeometryCfg 1 0 1 1 1 2 0 3 0 4 0 5 2.418 2.418
channelCfg 7 3 0
chirpComnCfg 8 0 0 256 4 28 0
chirpTimingCfg 6 63 0 75 60
frameCfg 2 0 200 64 250 0
guiMonitor 2 1 0 0 0 1 0 0 0 0 0
sigProcChainCfg 32 2 1 0 4 4 0 15
cfarCfg 2 8 4 3 0 12.0 0 0.5 0 1 1 1
aoaFovCfg -60 60 -40 40
rangeSelCfg 0.1 12.0
clutterRemoval 1
compRangeBiasAndRxChanPhase 0.0 1.00000 0.00000 -1.00000 0.00000 1.00000 0.00000 -1.00000 0.00000
1.00000 0.00000 -1.00000 0.00000
adcDataSource 0
adcLogging 0
lowPowerCfg 1
factoryCalibCfg 1 0 40 0 0x1ff000
mpdBoundaryBox 1 0 1.48 0 1.95 0 3
mpdBoundaryBox 2 0 1.48 1.95 3.9 0 3
mpdBoundaryBox 3 -1.48 0 0 1.95 0 3
mpdBoundaryBox 4 -1.48 0 1.95 3.9 0 3
sensorPosition 0 0 1.44 0 0
minorStateCfg 5 4 40 8 4 30 8 8
majorStateCfg 4 2 30 10 8 80 4 4
clusterCfg 1 0.5 2
baudRate 1250000
sensorStart 0 0 0 0
```

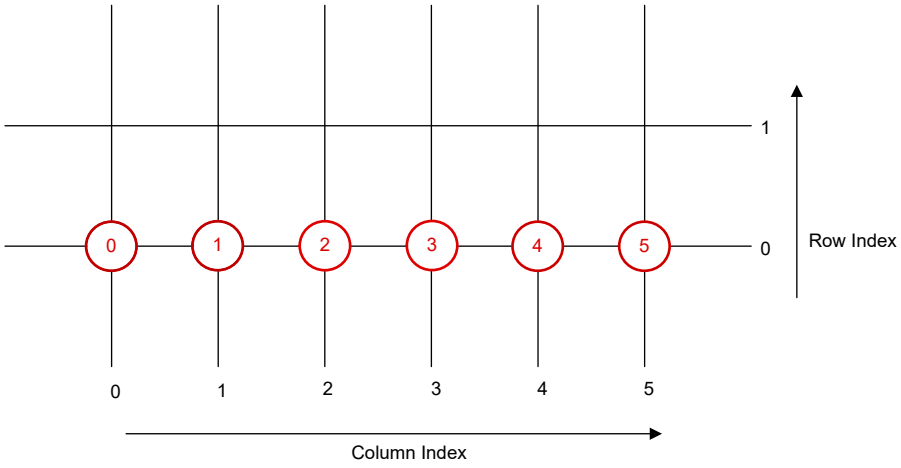


Figure 3-26. Virtual Antenna Index for IWRL6432FCCSP Reference Design 1D Antenna Variant

Antenna geometry command for 1D antenna variant: **antGeometryCfg 0 0 0 1 0 2 0 3 0 4 0 5 2.418 2.418**

This line can be pasted in the configuration file.

Example configuration for motion detect:

sensorStop 0

antGeometryCfg 0 0 0 1 0 2 0 3 0 4 0 5 2.418 2.418

channelCfg 7 3 0

chirpComnCfg 8 0 0 256 4 28 0

chirpTimingCfg 6 63 0 75 60

frameCfg 2 0 200 64 250 0

guiMonitor 2 1 0 0 0 1 0 0 0 0 0

sigProcChainCfg 32 2 1 0 4 4 0 15

cfarCfg 2 8 4 3 0 12.0 0 0.5 0 1 1 1

aoaFovCfg -60 60 -40 40

rangeSelCfg 0.1 12.0

clutterRemoval 1

compRangeBiasAndRxChanPhase 0.0 1.00000 0.00000 -1.00000 0.00000 1.00000 0.00000 -1.00000 0.00000 1.00000 0.00000 -1.00000 0.00000

adcDataSource 0

adcLogging 0

lowPowerCfg 1

factoryCalibCfg 1 0 40 0 0x1ff000

mpdBoundaryBox 1 0 1.48 0 1.95 0 3

mpdBoundaryBox 2 0 1.48 1.95 3.9 0 3

mpdBoundaryBox 3 -1.48 0 0 1.95 0 3

mpdBoundaryBox 4 -1.48 0 1.95 3.9 0 3

sensorPosition 0 0 1.44 0 0

minorStateCfg 5 4 40 8 4 30 8 8

majorStateCfg 4 2 30 10 8 80 4 4

clusterCfg 1 0.5 2

baudRate 1250000

sensorStart 0 0 0 0

Note

Respective command line is necessary to add within any configuration, before sending the same to device, otherwise the angle of arrival calculated by the processing chain can be erroneous.

There are in total, 14 entries in the command *antGeometryCfg*. The first 12 entries specify the spatial position of the virtual antennas sequentially, according to the respective row index and column index, shown in Figure 3-26. For example, consider the first two entries that define position of virtual antenna 0. For 2D antenna variant, row and column index for virtual antenna 0 are "1" and "0", whereas for 1D antenna variant, row and column index for virtual antenna 0 are "0" and "0". Both the cases are reflected in the first two entries of the respective *antGeometryCfg* commands. In the same way the spatial positions of each of the other five virtual antennas are entered afterward in the following set of entries.

The last 2 entries define the unit length in the virtual antenna array space, for example, the antenna spacing between azimuth columns and antenna spacing between elevation rows, in mm. In this case, the antenna spacing for both the directions are equal to λ/2, which is 2.418mm, where λ (wavelength) is computed based on 62GHz as the center frequency of the chirp configuration.

3.4.2 Range and Phase Compensation

The range bias and phase error needs to be compensated for different antenna designs using the command *compRangeBiasAndRxChanPhase*. There are default values incorporated in the demo configurations present in the MMWAVE-L-SDK.

If the antennas are flipped, the amplitude and phase compensation API needs to be used to correct the phase. The procedure for this is elaborated in the MMWAVE-L-SDK.

3.4.3 Chirp Configuration

The chirp properties can be altered depending on the application requirement using the different commands in the configuration file. A few determining factors for a particular chirp profile are: maximum detection distance requirement, power consumption, performance. For more information on chirp configuration please refer to Programming Chirp Parameters in TI Radar Devices and MIMO Radar

This section shows examples of chirp profile in two aspects, one with 10 meters and 15 meters human detection and another with high performance and low power consumption.

Note

These chirp profiles are tested in certain environmental conditions. Therefore, performance can vary depending on differences in environmental conditions.

Table 3-1. Chirp Configuration for 10m and 15m Human Detection

PARAMETER	10 meters	15 meters
ADC sampling rate (MHz)	8	12.5
Number of ADC samples	256	256
Ramp end time (µs)	37	90
Idle time in (µs)	50	138
Number of skip samples	24	40
Frequency slope (MHz/µs)	25	40
Start frequency (GHz)	61.5	59.75
Number of chirps in a burst.	8	170
Burst periodicity (µs)	811	40000

Table 3-1. Chirp Configuration for 10m and 15m Human Detection (continued)

PARAMETER	10 meters	15 meters
Number of bursts per frame	1	1
Frame periodicity (ms)	250	200
Effective bandwidth (MHz)	768	819.2

Table 3-2. Chirp Configuration for Low Power and High Performance

PARAMETER	Low power	High performance
No. of Rx antenna enabled	3	3
No. of Tx antenna enabled	1	2
ADC sampling rate (MHz)	8.3	12.5
Number of ADC samples	64	256
MIMO mode	TDM	BPM
Ramp end time (µs)	12	90
Idle time in (µs)	18	138
Number of skip samples	25	40
Frequency slope (MHz/µs)	60	40
Start frequency (GHz)	61	59.75
Number of chirps in a burst.	2	170
Burst periodicity (µs)	180	40000
Number of bursts per frame	1	1
Frame periodicity (ms)	1000	200
Effective bandwidth (MHz)	460.8	819.2
Power Consumption (mW)	1.5	254

Chirp configuration is subject to optimization. The parameters can be further optimized based on use case requirements.

3.5 Schematic and Layout Design Conditions

This section describes a number of schematic and layout conditions. For additional details, refer to the design checklist.

3.5.1 Internal LDO Output Decoupling Capacitor and Layout Conditions for BOM Optimized Topology

This section depicts the recommended values of de-coupling capacitors and range of allowable parasitic inductance and resistance in particular sections of the output path for the internal LDOs. Like all low dropout regulators, the internal LDO requires an output capacitor connected between OUTPUT and GND to stabilize the internal control loop. The minimum and maximum values of the capacitor captured in Table 3-3 to Table 3-6. The tables include variation of a given capacitor due to DC bias, tolerance and temperature variation.

Note

1. If the parasitic values are not kept within the specified range, performance of the device can degrade.
2. Typical values of de-coupling capacitors are recommended for use. Any capacitance value taken near the edge of the range can degrade the performance. The working range of the chosen capacitor can not exceed the specified range.

Refer to *IWRL6432 Single-Chip 57- to 64GHz Industrial Radar Sensor* data sheet for latest information on the maximum allowed parasitic values.

3.5.1.1 Single-Capacitor Rail

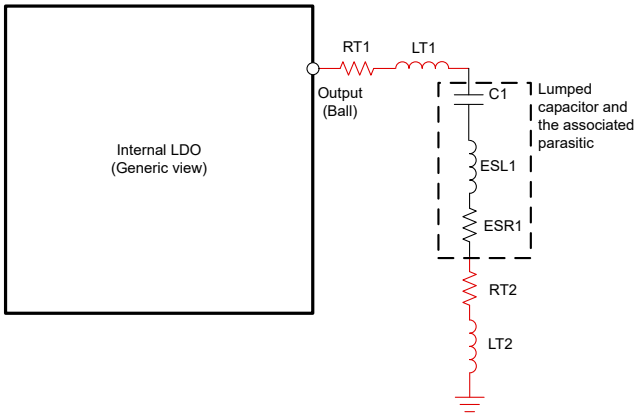


Figure 3-27. Parasitic Offered by Different Portions of the Output Path (for one Capacitor)

The 1.2V digital LDO requires one decoupling capacitor with a typical value of 4.7uF. The recommendation is to use X7R type capacitors which has a lower variation across temperature. The parasitic offered by different portions of the output path is illustrated in Figure 3-27. *RT1* and *RT2* are parasitic resistances offered by the ball to capacitor lead trace and the ground trace respectively. Similarly, *LT1* and *LT2* are parasitic inductance offered by the ball to capacitor lead trace and the ground trace respectively. *ESL1* and *ESR1* are the effective series inductance and resistances of the decoupling capacitor. Table 3-3 gives the minimum, maximum and typical values of the capacitance and the parasitic.

Note

These constraints are not applicable for other single capacitor LDOs such as APLL and SYNTH.

3.5.1.1.1 1.2V Digital LDO

Ball name: VDD

Table 3-3. 1.2V Dig LDO Output

	Min	Typ	Max	Unit
Recommended value of C	3.6	4.7	5.2	uF
Allowed output parasitic inductance Lp [1]	1	1.5	2	nH
Allowed output parasitic resistance Rp [2]	15	20	35	mΩ

(1) Lp = LT1 + ESL1 + LT2
(2) Rp = RT1 + ESR1 + RT2

3.5.1.2 Two-Capacitor Rail

1.2V RF LDO, 1.2V SRAM LDO and 1.0V RF LDO require two decoupling capacitors with typical values of 10uF and 2.2uF.

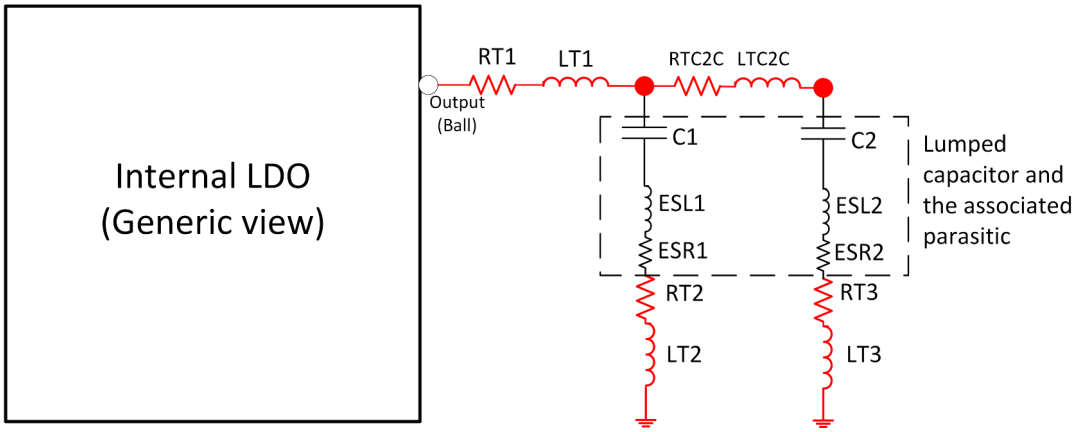


Figure 3-28. Parasitic Offered by Different Portion of the Output Path (for two Capacitors)

The parasitic offered by different portions of the output path is illustrated in Figure 3-28. As shown in the image, the output path can be divided into four portions:

- **Ball to first capacitor:** *RT1* and *LT1* are the parasitic resistance and inductance offered by the ball to the first capacitor lead.
- **Along the first capacitor:** *ESL1* and *ESR1* are the effective series inductance and resistance of the first decoupling capacitor. *RT2* and *LT2* are the ground trace resistance and inductance respectively of the first capacitor ground trace.
- **First capacitor lead to second capacitor lead:** *RTC2C* and *LTC2C* are the resistance and inductance of the trace between two capacitors.
- **Along the second capacitor:** *ESL2* and *ESR2* are the effective series inductance and resistance of the second decoupling capacitor. *RT3* and *LT3* are the ground trace resistance and inductance respectively of the second capacitor ground trace.

Note

Both the capacitors are recommended to be placed close to the respective ball.

3.5.1.2.1 1.2V RF LDO

Ball name: VDDA_12RF

Table 3-4. 1.2V RF LDO Output

		Min	Typ	Max	Unit
Recommended value of C	C1	4.9	10.0	11.0	uF
	C2	1.3	2.2	2.4	uF
Allowed output parasitic inductance	Ball to 1st Capacitor lead (LT1)	0.3		0.6	nH
	Along 1st Capacitor (ESL1 + LT2)	0.4		0.7	
	Between two Capacitor leads (LTC2C)	0.1		0.3	
	Along the 2nd Capacitor (ESL2 + LT3)	0.4		0.7	
Allowed output parasitic resistance	Ball to 1st Capacitor lead (RT1)	1		5	mΩ
	Along 1st Capacitor (ESR1 + RT2)	15		25	
	Between two Capacitor leads (RTC2C)	1		5	
	Along the 2nd Capacitor (ESR2 + RT3)	15		25	

3.5.1.3 1.2V SRAM LDO

Ball name: VDD_SRAM

Table 3-5. 1.2V SRAM LDO Output

		Min	Typ	Max	Unit
Recommended value of C	C1	4.9	10.0	11.0	uF
	C2	1.3	2.2	2.4	uF
Allowed output parasitic inductance	Ball to 1st Capacitor lead (LT1)	0.5		1.0	nH
	Along 1st Capacitor (ESL1 + LT2)	1.0		1.5	
	Between two Capacitor leads (LTC2C)	0.5		1.0	
	Along the 2nd Capacitor (ESL2 + LT3)	1.0		1.5	
Allowed output parasitic resistance	Ball to 1st Capacitor lead (RT1)			1	mOhm
	Along 1st Capacitor (ESR1 + RT2)	15		35	
	Between two Capacitor leads (RTC2C)			1	
	Along the 2nd Capacitor (ESR2 + RT3)	15		35	

3.5.1.4 1.0V RF LDO

Ball name: VDDA_10RF

Table 3-6. 1.0V RF LDO Output

		Min	Typ	Max	Unit
Recommended value of C	C1	4.9	10.0	11.0	uF
	C2	1.3	2.2	2.4	uF
Allowed output parasitic inductance	Ball to 1st Capacitor lead (LT1)	0.3	0.3	0.6	nH
	Along 1st Capacitor (ESL1 + LT2)	0.3		1.0	
	Between two Capacitor leads (LTC2C)	0.1		0.3	
	Along the 2nd Capacitor (ESL2 + LT3)	0.3		1.0	
Allowed output parasitic resistance	Ball to 1st Capacitor lead (RT1)	1		5	mOhm
	Along 1st Capacitor (ESR1 + RT2)	15		25	
	Between two Capacitor leads (RTC2C)	1		5	
	Along the 2nd Capacitor (ESR2 + RT3)	15		25	

3.5.2 Best and non-Best Layout Practices

This section focuses some layout practices that can affect the overall radar performance.

3.5.2.1 Decoupling Capacitor Placement

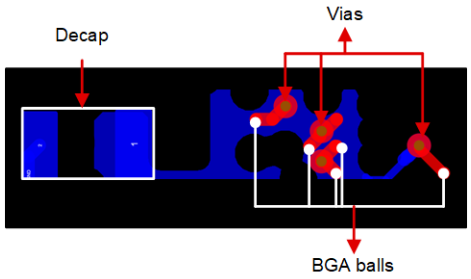


Figure 3-29. Decoupling Capacitor Placement: Non-Best Practice

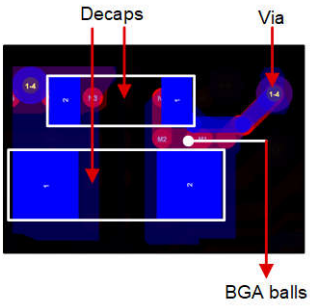


Figure 3-30. Decoupling Capacitor Placement: Best Practice

On-chip LDOs require external capacitors for dominant pole compensation. For this, the capacitor placement and the output path traces become PCB design constraint dependent. The parasitic components contributed by the output path play a vital role in determining the system stability. In the previous section we have listed specific parasitic inductance and resistance values for each of the high bandwidth sensitive LDOs to make sure the stability of the power supplies. Here we are going to observe an example of good and bad practices while designing the PCB layout.

Figure 3-29 shows a design where the decap is placed far from the respective LDO-output BGA-balls. Considering the length of the complete trace connecting the balls to the capacitor lead by adding:

1. The trace connecting the BGA balls to the respective vias in the top layer (traces marked in red are on the top layer of the PCB)
2. Via length
3. The trace connecting the vias to the capacitor lead (traces marked in blue are in the bottom layer of the PCB), we get a very long path. The combined parasitic of such long path can potentially alter the parasitic spec provided in data sheet, which can affect the LDO system stability.

Figure 3-30 shows a design where the capacitor is places very close to the BGA balls. Considering the possibilities of system instability involved with the previous example, this design is much better as the parasitic values are within the data sheet spec.

3.5.2.2 Ground Return Path

The recommendation is to follow this design practice for all the on-chip LDO outputs to maintain shortest forward path.

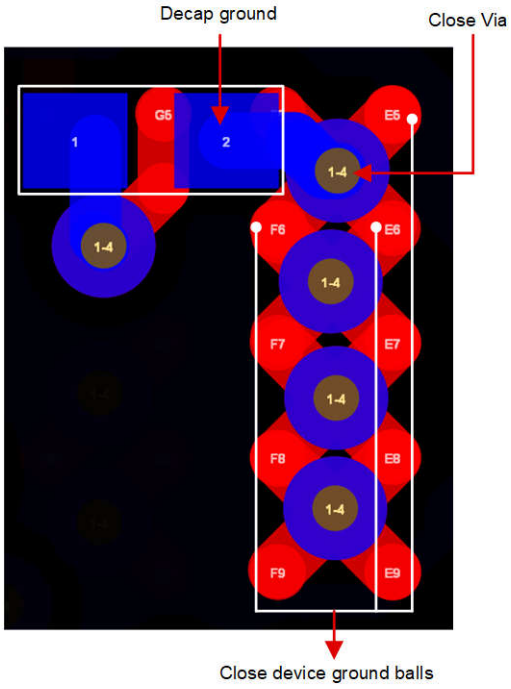


Figure 3-31. Ground Return Path

An output path that can potentially act as a source of out-of-spec parasitic values consists of two elements:

1. The forward path, that connects the BGA balls to the capacitor lead
2. the ground return path that connects the capacitor ground to the device ground to close the loop. Figure 3-31 is a good example of ground return path.

As we can see in Figure 3-31, the decap ground is connected to a via which is placed very close to the ground lead of the capacitor. Further, the device ground is also very close to the via. This provides the shortest ground return path for the signal.

3.5.2.3 Trace Width of High Current Carrying Traces

Follow this design practice for all the on-chip LDO outputs to maintain shortest ground return path.

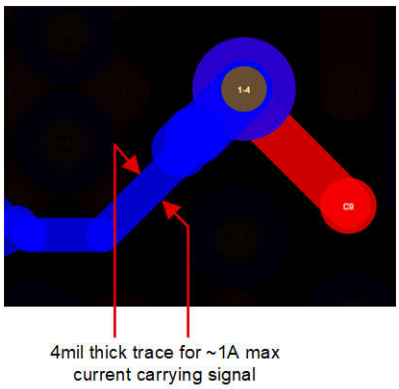


Figure 3-32. Trace width: Non-Best Practice

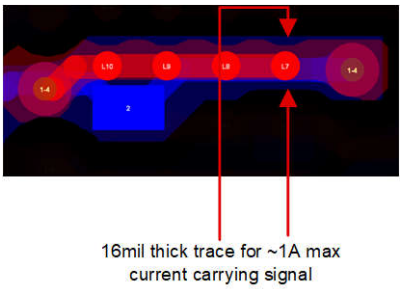


Figure 3-33. Trace Width: Best Practice

The PCB trace width must be sufficient to support the max current requirement of the respective signal. The following are examples of good and bad design practices for a trace carrying a high current signal.

Figure 3-32 shows a trace of width 4mils for a signal that can carry a max. of 1A current. This trace can not support this much of a max current.

Figure 3-33 shows a trace of width 16mils for a signal that can carry a max of 1A current. This is a good design as the trace is thick enough to support this current.

Consider the max current and selecting the trace thickness accordingly. Usually 12-15mils thick trace is enough to carry 1A max current.

3.5.2.4 Ground Plane Split

Have ground planes with no splits. Figure 3-34 shows a continuous ground plane (2nd layer) with no splits.

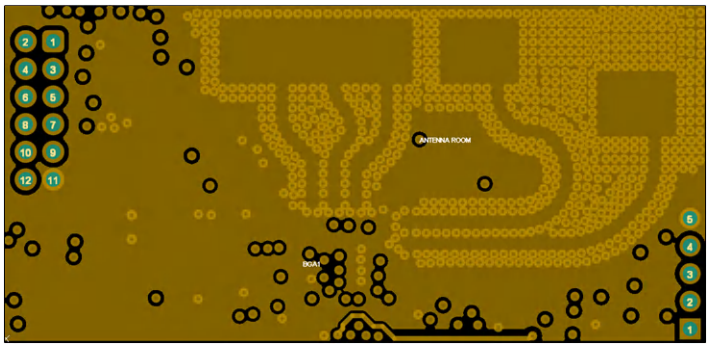


Figure 3-34. Ground Plane: No Split

4 Link Budget

The maximum range at which a human can be detected is computed by the link budget discussed below, which is a function of the detection SNR, radar cross-section of the object, RF performance of the radar device, antenna gains, and the chirp parameters. The maximum detection range can be changed based on application requirements by altering these parameters. For more details on this, please refer to the MMWAVE-L-SDK.

Table 4-1. Link Budget - Selected Parameters

Parameters	Values	Unit
Transmitted signal power (max)	10	dBm
Transmitter/Receiver antenna gain	5	dBi
Noise figure of the receiver	11	dB
Radar cross section	1	m^2
Total system loss	5	dB
Required detection SNR	9	dB
Total virtual antennas	6	-
Chirp time	25.6	us
Chirp repetition period	300	us
Number of chirps per frame	32	-
Valid bandwidth	486	MHz
Maximum detection range based on SNR	28.78	m

5 Hardware, Software, Testing Requirements and Test Results

This section elaborates on testing of the reference design and procedures involved in connecting the reference design with host PC.

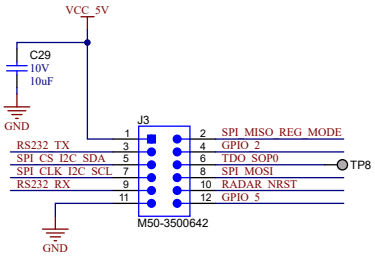


Figure 5-1. 12-Pin Connector

Table 5-1. IWRL6432FCCSP Reference Design Pinouts

Pin No.	Pin name	Functionality
1	VCC_5V	5V power supply
2	SPI_MISO_REG_MODE	SPI MISO signal
3	RS232_TX	UART B (RS232) Tx
4	GPIO_2	GPIO
5	SPI_CS_I2C_SDA	SPI chip select/SDA of I2C
6	TDO_SOP0	SOP0 control
7	SPI_CLK_I2C_SCL	SPI clock/SCL of I2C
8	SPI_MOSI	SPI MISO signal
9	RS232_RX	UART B (RS232) Rx
10	RADAR_NRST	NRESET control pin
11	GPIO_5	GPIO
12	GND	Ground

Along with the power supply and communication interfaces, special care needs to be taken so that the SOP0 is properly asserted (logic 0 for flashing mode, logic 1 (on board pull up) for functional mode) and NRESET is asserted after the power and SOP lines are stable before initiating radar operations.

5.1 Hardware Requirements

This section discusses the procedure to connect the reference design with a host PC used to validate and test the reference design.

The reference design communicates to the outside world with UART, SPI, and I2C interfaces. A UART interface is used to establish communication between the reference design and a host PC. To do this, a USB to UART converter is required. The following are a few USB to UART converters that have been used for testing:

1. MSP-EXP432E401Y - XDS110 based launchpad
2. LP-XDS110ET - XDS110 based launchpad
3. FT232RL - FTDI based USB to UART bridge

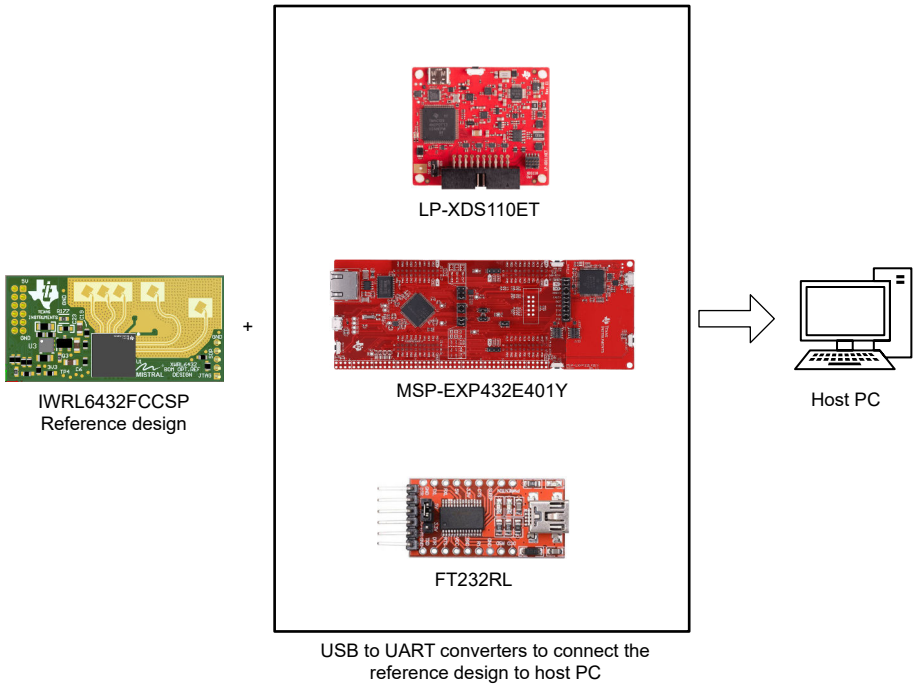


Figure 5-2. Reference Design Connection to Host PC

Any of the three USB to UART converters can be used to establish communication between the reference design and a host PC.

The reference design uses 1.27mm pitch pins to reduce the form factor. However, 2.54mm pitch jumpers are needed to connect to most USB to UART adapters. Because of this, to connect with the USB bridges, a pitch converter DR127D254P20F has been used. Below image depicts the same:

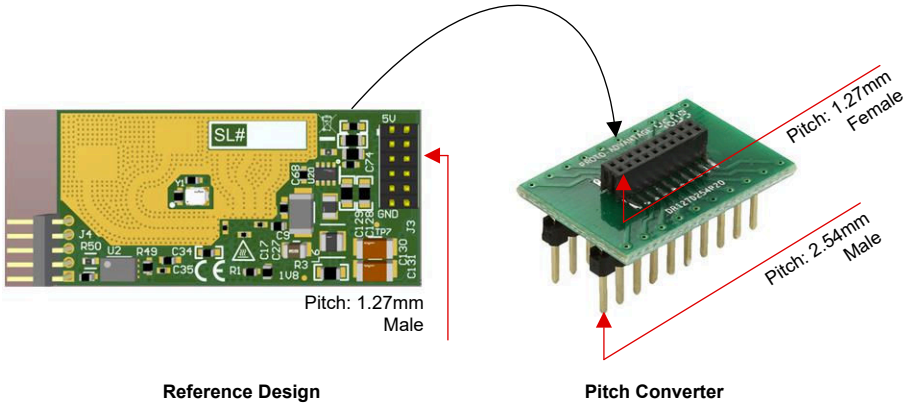


Figure 5-3. Use of Pitch Converter

In this procedure, the reference design is mated to the pitch converter and 2.54mm pitch male headers from the other side of the pitch converter has been used to make the connection. Following are few cautionary items that have been taken care of while establishing the connection:

5.1.1 Connection to the USB to UART Bridges

In this connection jumper wires are used that:

1. Support the maximum peak current requirement for the power pins (5V), for example 200-300mA.
2. Are of smaller and equal length without introducing large DCR to compromise data transfer speeds to lose information.
3. Has small IR drop and Inductance to prevent ringing on supply and GND.

5.1.2 USB Cable to Connect to Host PC

USB cables of length 1m (or less) has been used. Longer cable can impact timing relation to baudrate due to parasitic of cable.

5.1.3 The Rx-Tx Attribution of RS232

The Rx-Tx consideration varies with different USB to UART bridges. If the connection is not established between host PC and the reference design, the Rx-Tx pins can be swapped and the connection can be re-established.

5.2 Software Requirements

The reference design was programed using Uniflash. Algorithms implemented in Matlab were used to post process the captured raw data. The pedestrian detection testings were performed using the MMWAVE-L-SDK.

5.3 Test Scenarios

Four sets of tests have been demonstrated here:

1. 15m pedestrian detection
2. Measured antenna radiation pattern
3. Angle error across FoV
4. Angular resolution

5.4 Test Results

5.4.1 Human Detection at 15 Meters in Boresight

In an open space the sensor was placed for the test. The chirp configuration used for this test is elaborated in Section 3.4.3.

Figure 5-4. 15 Meter Pedestrian Detection

5.4.2 Antenna Radiation Plots

Antenna radiation pattern and angle error across FoV have been processed in matlab with the raw data collected from anechoic chamber.

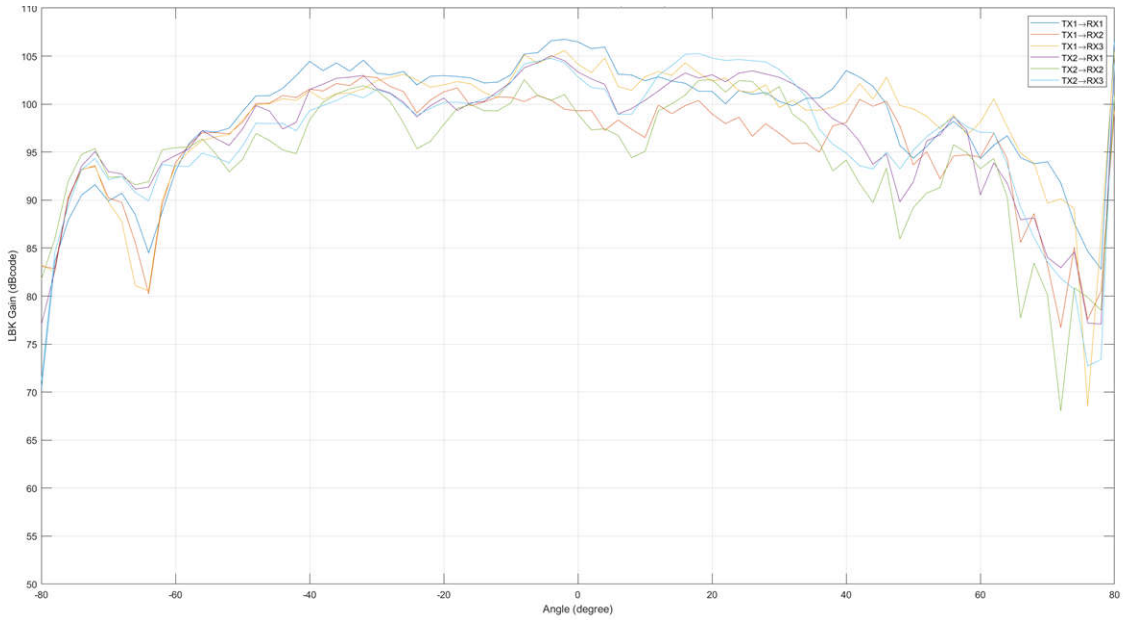


Figure 5-5. Measured Radiation Pattern - 2D Antenna (Azimuth)

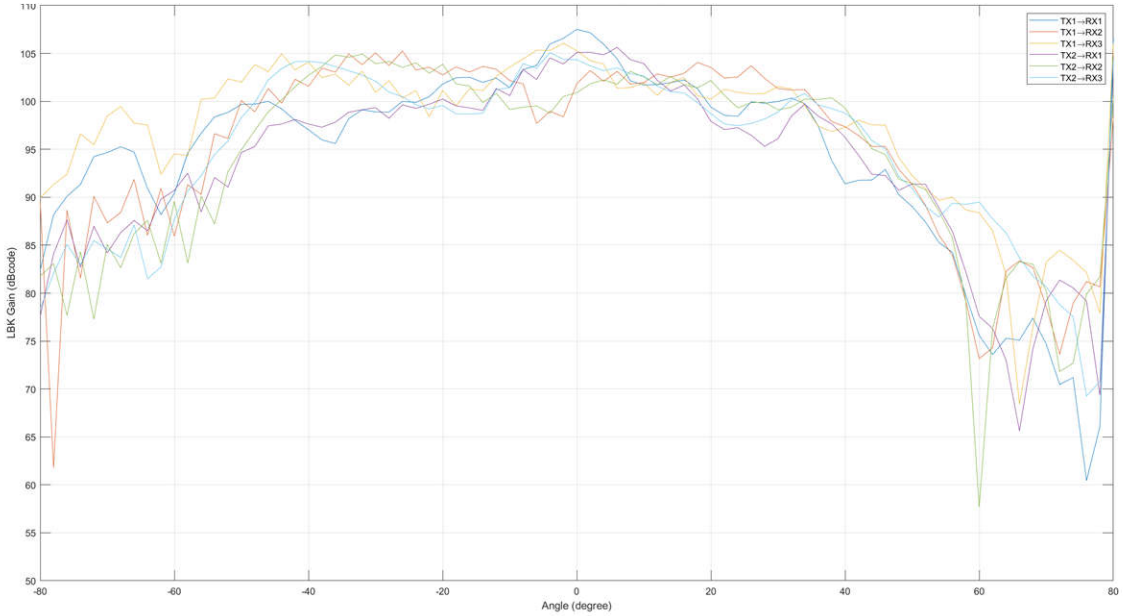


Figure 5-6. Measured Radiation Pattern - 2D Antenna (Elevation)

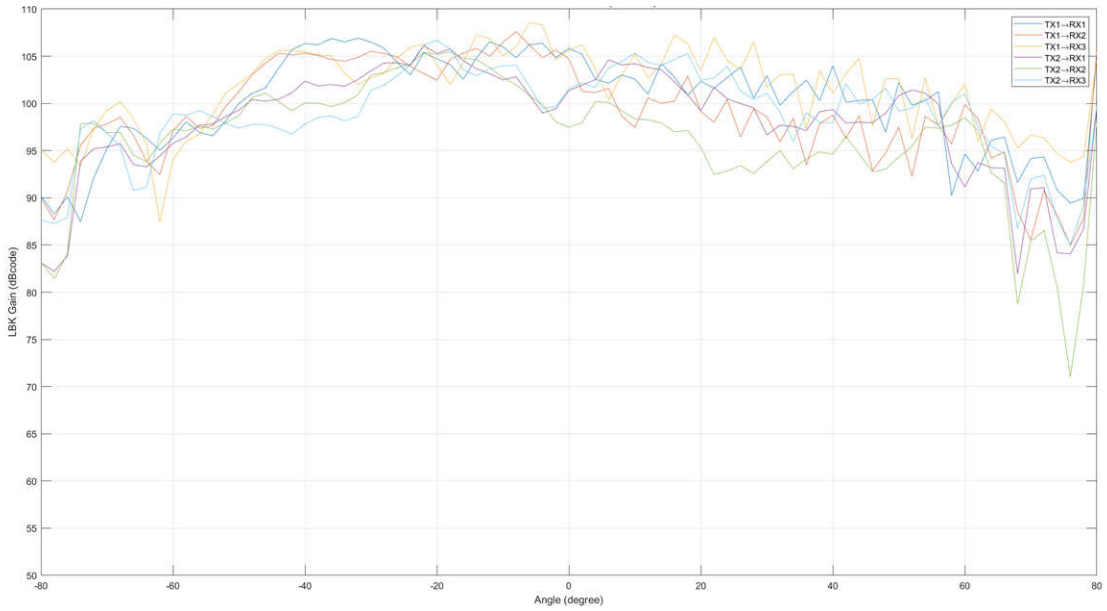


Figure 5-7. Measured Radiation Pattern - 1D Antenna (Azimuth)

5.4.3 Angle Estimation Accuracy in Azimuth Plane

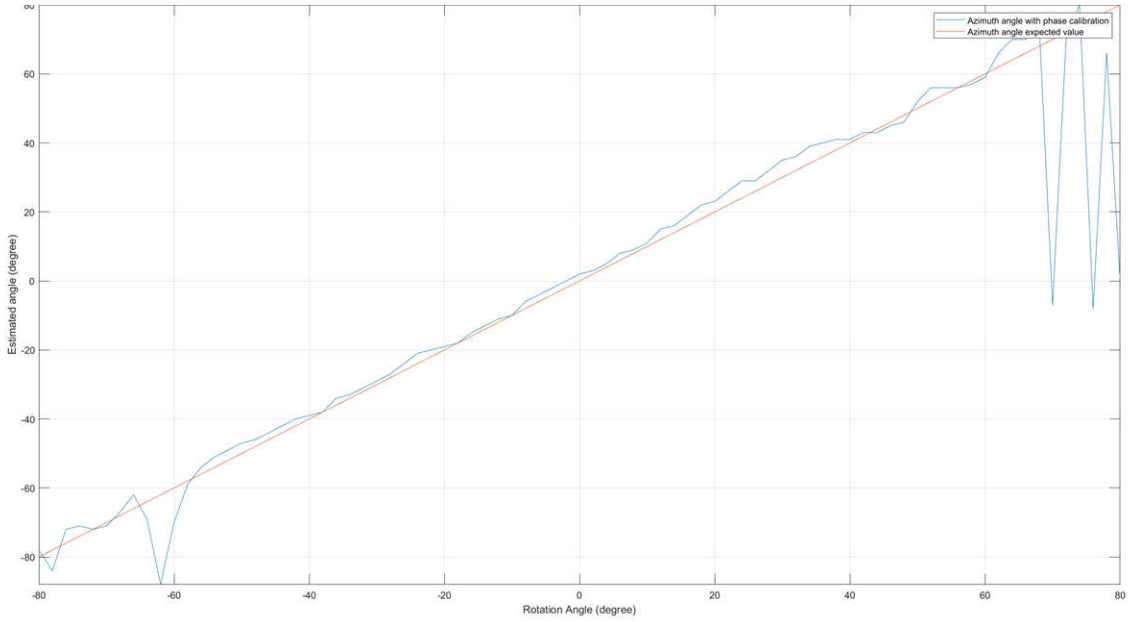


Figure 5-8. Azimuth Angle Estimation

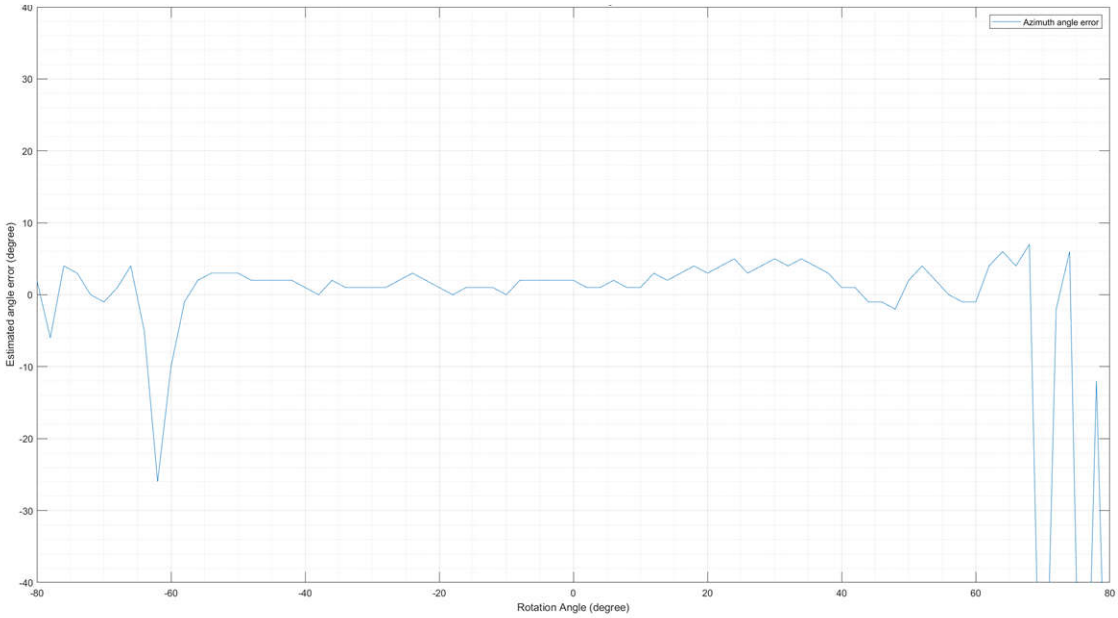


Figure 5-9. Azimuth Angle Estimation Error

5.4.4 Angle Resolution

Theoretical angular resolution in azimuth plane for 6-antenna elements is 19°. In this test, two people at a 20° angle with respect to the sensor are tested and two distinct peaks in the angle plot have been observed.

This measurement is done with the 2D antenna variant. The distance of the target human beings from the sensor is 3 meters with 1 meter mutual distance that creates around a 20° angle with respect to the sensor. Two peaks have been observed 21° apart that correspond to the target human beings.

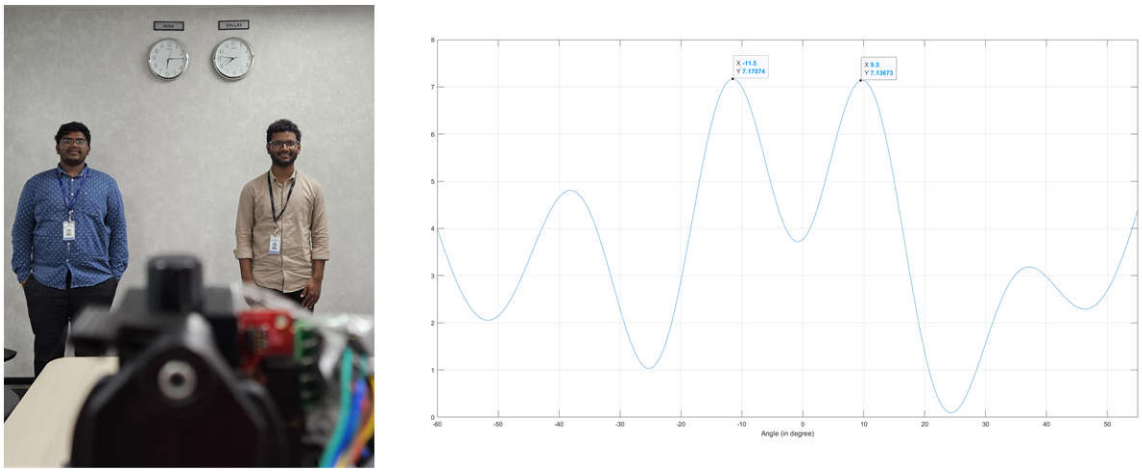


Figure 5-10. Angle Resolution Test

6 Design and Documentation Support

6.1 Design Files

6.1.1 Schematics

To download the schematics, see the design files at TIDEP-01033.

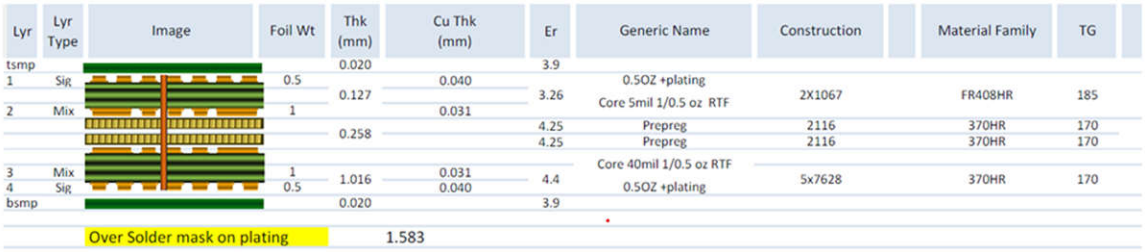
6.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDEP-01033.

6.1.3 PCB Layout Recommendations

Some of the important layout recommendations have been discussed in Section 3.5.

6.1.3.1 Layout Prints



More on the stack-up has been discussed in Section 3.3.

Figure 6-1. PCB Stack-up Used for the Reference Design

6.2 Tools and Software

Tools

CCS Studio	Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. The tool comprises a suite of tools used to develop and debug embedded applications. Code Composer Studio is available for download across Windows®, Linux®, and macOS® desktops. The tool can also be used in the cloud by visiting the TI Developer Zone.

Software

Uniflash	UniFlash is a software tool for programming on-chip flash on TI microcontrollers and wireless connectivity devices and on-board flash for TI processors. UniFlash provides both graphical and command-line interfaces.

6.3 Documentation Support

1. Texas Instruments, *IWRL6432 Single-Chip 57- to 64GHz Industrial Radar Sensor* data sheet

6.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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