Design Guide: TIDA-010976

52s Wireless Battery Management Unit Reference Design for Energy Storage System

Description

This reference design provides a 52s Wireless Battery Management Unit (wBMU) for energy storage systems with high cell-voltage accuracy. The wBMU passes voltage and temperature data from each cell to the host controller in real-time, using wireless communication technology. The design overcomes challenges in wired battery management system (BMS) architecture by avoiding cumbersome manufacturing processes, reducing frequent maintenance needs, and minimizing failure rates of connectors and harnesses. Wireless communication reduces the number of required cables and connectors, lowering system weight and costs.

Resources

TIDA-010976	Design Folder
BQ78706, CC2662R-Q1, LM5168	Product Folder
TMUX1308, TPS3436-Q1, LSF0204	Product Folder
TMP61, TPS71533	Product Folder

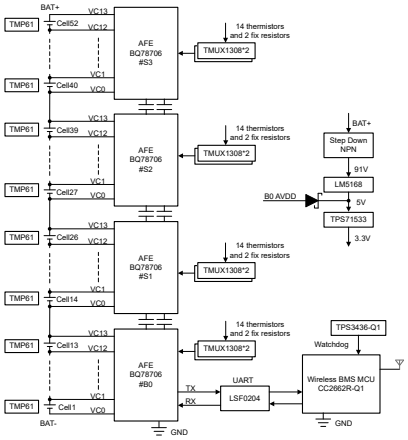
Ask the TI E2E™ support experts

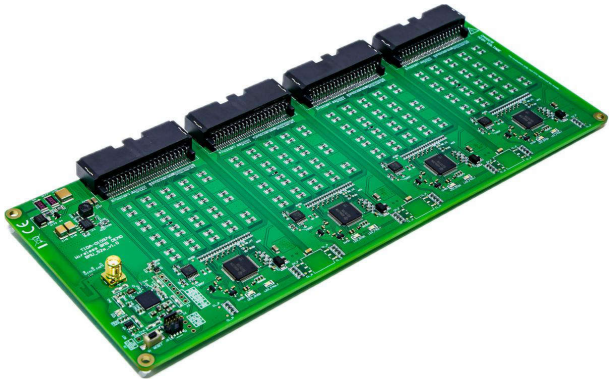
Features

- ±2.4mV voltage accuracy at 2V < cell voltage < 4V, –40°C to 125°C without calibration
- Full cell-temperature sensing with multiplexer (MUX)
- Robust wireless communication with functional safety-rated protocol
- Robust and programmable battery cell and pack protection
- 32µA current consumption in keep-alive mode
- Compatible with bus bar or no bus bar connection

Applications

- ESS – Wireless battery management system (wBMS)
- Battery backup unit (BBU)





1 System Description

Energy storage systems (ESS) play an important role in renewable energy applications. Depending on the system voltage, capacity, and usage. ESS can be divided into three different categories: residential ESS, commercial and industrial ESS, and grid ESS. Commercial and industrial, and grid ESS contain several racks that each contain several packs in a stack. Residential ESS only contains packs.

Battery pack which consists of battery cells in a series and parallel connection manner is a basic module comprising the ESS. Because of the weight limit and longer endurance needs, the battery cell chemistry is shifting from Lead-acid to Li-ion, Li-polymer, or Li-ion phosphate (LiFePO4) types. These battery chemistries are good in both volumetric and gravimetric energy density. While these battery chemistries provide high energy density and thereby lower volume and weight as an advantage, these battery products are associated with safety concerns and have a need for more accurate and complicated monitoring and protections. Therefore, the pack current, cell temperature, and each cell voltage must be monitored in a timely manner in case of unusual situations. The battery pack must be protected against all these situations. Good measurement accuracy is always required, especially the cell voltage, pack current, and cell temperature. Precision is necessary for accurate protections and battery pack state of charge (SoC) calculations. This is especially true for LiFePO4 battery pack applications because of the flat voltage. Another important feature for battery-powered applications is the current consumption, especially when in ship mode or standby mode. Lower current consumption saves more energy and gives longer storage time without overdischarging the battery.

A battery management unit (BMU) is a board that monitors the voltage and temperature of each battery cell in the pack for a complete lifecycle. High measurement accuracy for voltage and temperature monitoring is required for the BMU. BMU can communicate through wired or wireless methods back to the rack-level controller battery control unit (BCU) to deliver battery pack data for safety and charging management.

In a wired BMS design, controller area network (CAN) and daisy chain are traditionally and widely used for robustness of communication. A CAN structure controller needs a microcontroller unit (MCU), a digital isolator, and an isolated power module to operate the CAN communication function. Compared with the CAN interface, only a couple of isolation transformers are needed in the BMU based on daisy chain communication. Thus, a daisy chain design shows an advantage in cost over a CAN especially in high-capacity battery pack applications since cost is a concern for a CAN structure in large-capacity BESS which consist of many BMU nodes and CAN interface devices. Insulation requirements also raise cost because the reinforced insulation required between the BMU and BCU communication interface necessitates a digital isolator and isolated power module.

The wireless BMS (wBMS) design uses a wireless interface to transmit universal asynchronous receiver-transmitter (UART) data from the battery monitor in BMU to the host MCU in BCU through a wireless transceiver device. The biggest differences between wired and wireless designs is wBMS replaces the communication cables, connector and isolation components with a wireless MCU on each BMU.

This design focuses on energy storage system application and can be used in other high-voltage battery pack applications like server battery back-up unit. The wireless BMS MCU CC2662R-Q1 is used for the robust wireless communication between BMUs based on TI self-developed wireless BMS protocol operating in the 2.4GHz frequency band. Each BMU has four BQ78706 devices (battery monitor, balancer, and integrated hardware protector) to monitor each cell voltage, the temperature of a 52s battery pack, and to protect the pack against situations that include cell overvoltage, cell undervoltage, and overtemperature. The onboard communication between BQ78706 devices uses capacitor-isolated daisy chain. The design contains eight TMUX1308 devices for a general-purpose input/output (GPIO) expansion ratio of 8:1 to measure up to 52s cells. The design uses an internal cell balancing (CB) to get 100mA balancing current per cell channel.

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the system block diagram.

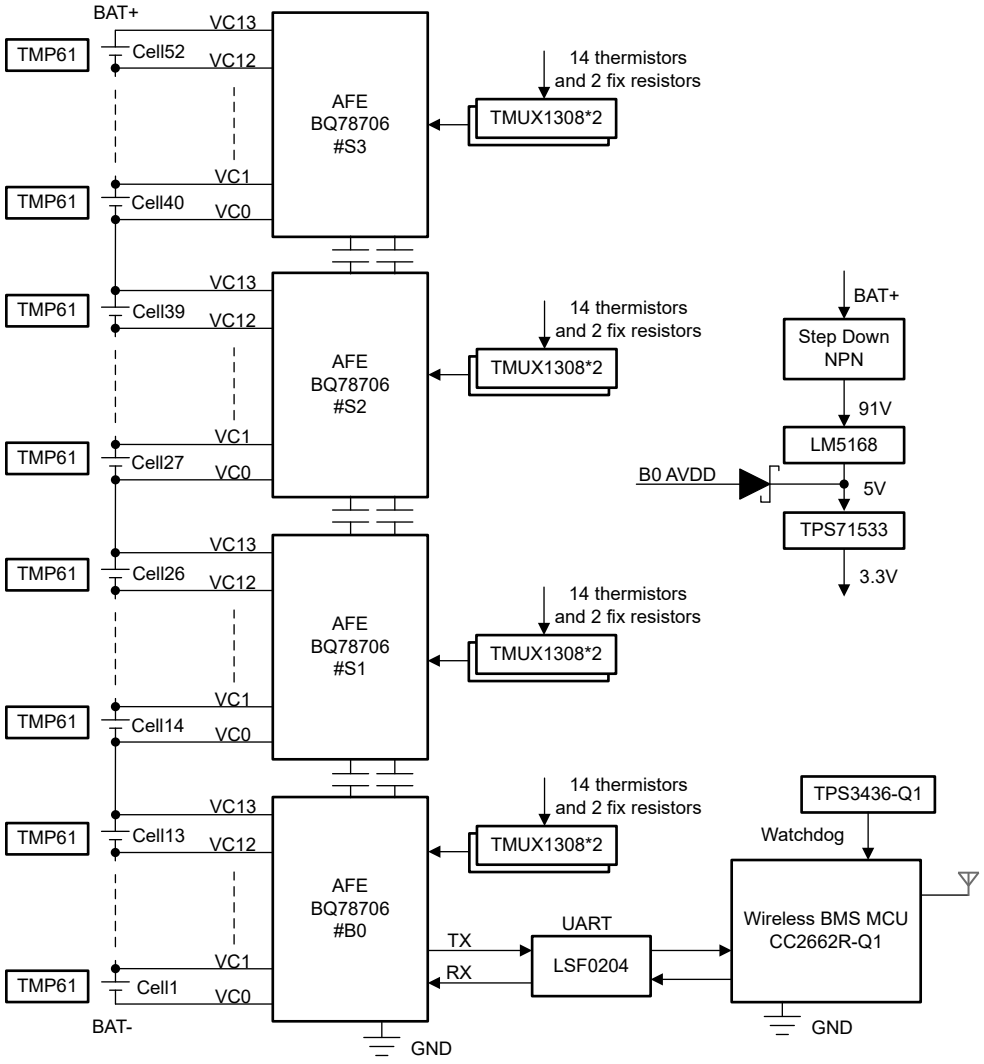


Figure 2-1. wBMU Block Diagram

The design uses wBMS MCU CC2662R-Q1 to enable the wireless communication between BMU. This wBMS MCU is Systems-on-Chip (SoC) that integrate a radio frequency (RF) physical layer and user-programmable MCU core that can implement communication protocol stacks and application software (SW). The protocol is self-developed, proprietary wireless BMS protocol based on *Bluetooth*® Low Energy technology operating in the 2.4GHz frequency band.

The design uses four BQ78706 devices to monitor each cell voltage, monitor the temperature of a 52-cell battery pack, and to protect the pack against all unusual situations, including cell overvoltage, cell undervoltage, and overtemperature. In Figure 2-1, the top BQ78706 device is the BQ78706#S3 and the bottom BQ78706 device is the BQ78706#B0. The forward daisy-chain communication direction is from the BQ78706#B0 device to the BQ78706#S1 device.

Each BQ78706 has 11 GPIO pins for temperature sensing and 14 VC pins for voltage sensing. To monitor the temperatures for all the VC channels with fewer GPIO pins, two TMUX1308 multiplexers are used. The multiplexers expand temperature-sensing capabilities of one BQ78706 from 11 channels to 18 channels, which includes14 MUX-related thermistors, 2 constant resistors, and 4 independent thermistors.

To run diagnostics for the TMUX1308 to prevent the MUX from failure mode, one channel of each TMUX1308 is connected to a constant resistor. This constant resistor is out of the range of thermistors which enable a plausibility check. This diagnostic method can show if the MUX is stuck on a specific channel or reporting voltages corresponding to incorrect channels.

The AVDD pin on the BQ78706 is used to supply power to the TMUX1308. Since AVDD can be configured as off state by shorting RX to AVDD, AVDD can enable a low shutdown current with no leakage current to external MUX devices. When BQ78706 is waked, then AVDD supplies all the external loads with 20mA capacity which is enough for MUX or other devices. #B0 is different. The AVDD need be configured as on to enable UART when #B0 is shutdown so the TMUX1308 of #B0 is powered by the output of LM5168.

To avoid the supply current difference of different BQ78706 devices, this design build an onboard power rail to power the wBMS MCU rather than use #B0 AVDD. A 120V input, 0.3A, ultra-low I_Q synchronous buck DC/DC converter LM5168 with a low I_Q is used as a pre-regulator. A discrete step-down circuit is added before LM5168 because the 52s battery pack voltage can exceed 120V.

The internal passive cell balancing resistors can support up to 100mA of balancing current per channel. An odd and even cell balancing can be used to achieve an average 50mA balancing current.

A ±1%, 10kΩ linear thermistor with positive temperature coefficient TMP61 is utilized to monitor the cell temperature and is measured by the BQ78706 device.

2.2 Design Considerations

2.2.1 Wireless Hardware Configurations

The *CC13xx/CC26xx Hardware Configuration and PCB Design Considerations* application note provides design guidelines for the CC2662R-Q1 RF front-end, schematic, PCB, and antenna. Use the *Crystal Oscillator and Crystal Selection for the CC13xx, CC26xx, CC23xx, and CC27xx Family of Wireless MCUs* application note as a reference for crystal selection.

This design uses a single-ended RF front-end configuration for low current consumption and less component count. A balun is used to transform the signal from balanced (differential) to unbalanced (single-ended). Figure 2-2 shows the configuration. RF components are recommended be 0201(imperial) size components as this allows for the component pads to better match the 50Ω RF traces which reduces discontinuities and which helps reduce insertion loss.

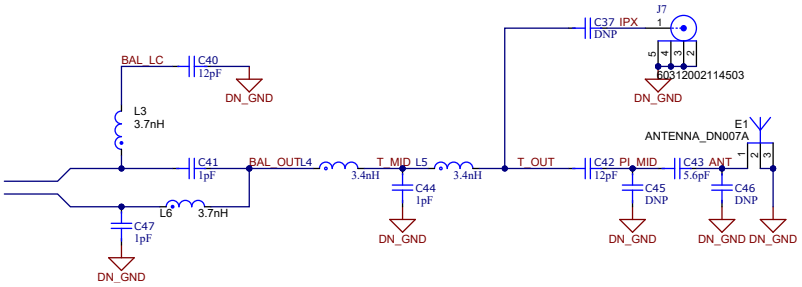


Figure 2-2. RF Front End

For antenna selection, see the antenna selection guides: *Antenna Selection Quick Guide* and a comprehensive *Antenna Selection Guide*.

Including an antenna matching network is always advised, so the designer can tune and reduce the mismatch losses of the antenna. For a single-band antenna, the recommendation is to always include a pi-match network prior to the antenna, see Figure 2-3. Only two of the three footprints (or components) are required. The impedance of the antenna determines if footprint (or component) ANT1 or ANT3 is used. ANT2 is always used and even if the antenna is an excellent match, then this can just be set as a 5.6pF capacitor in this design.

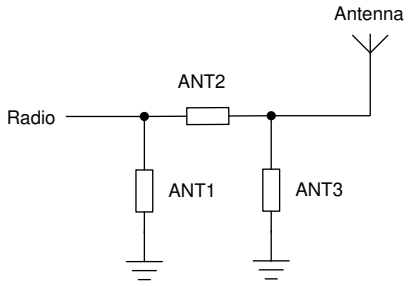


Figure 2-3. Recommended Antenna PI-Match Network for Single-Band Antennas

This design selects the 2.4GHz inverted F antenna for wBMS communication. The *2.4GHz Inverted F Antenna* application note shows the measurements results of this antenna. An SMA test port is also included for the initial bring up and aids in output power verification.

2.2.2 Auxiliary Power Strategy

Configure the #B0 AVDD as *on* to enable UART when #B0 is in shutdown mode. In theory, #B0 AVDD can be used to power the wBMS MCU, level shifter, and multiplexer but this configuration increases the current consumption of #B0. To avoid this, the design built an onboard power rail to power the wBMS MCU rather than use #B0 AVDD. Figure 2-4 shows the strategy for this design.

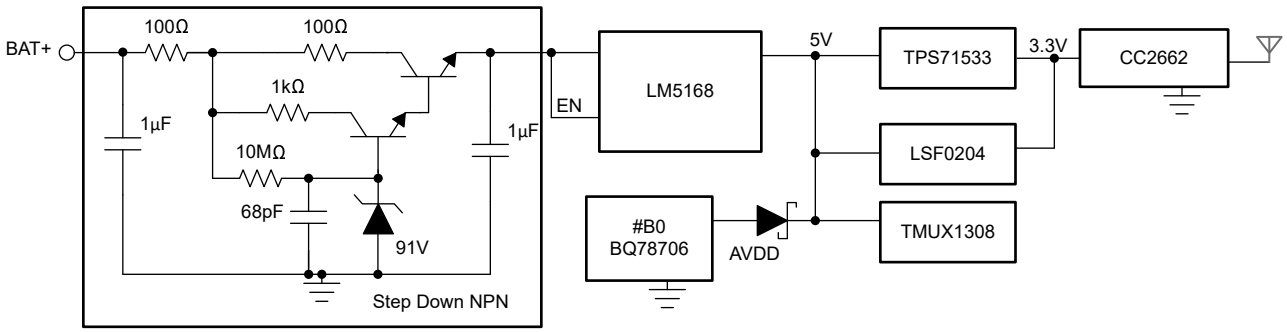


Figure 2-4. Auxiliary Power Strategy

The low-voltage ESS power strategy has a 120V input, 0.3A, ultra-low I_Q synchronous buck DC/DC converter LM5168P with a low I_Q 50mA LDO TPS71533 as the main power source, giving the system better efficiency and thermal performance than LDOs only.

A discrete step-down circuit is added before DC/DC because the 52s battery pack voltage can exceed 120V. Two NPN transistors are used in the step-down circuit to increase the DC current gain to lower the quiescent current. #B0 AVDD is connected to the output of DC/DC for redundancy. The CC2662R-Q1 is powered by #B0 AVDD if the LM5168 or step-down NPN circuit is failed. Set the LM5168 output voltage slightly above 5V, allowing the Schottky diodes to be reversed under normal operating conditions.

The auxiliary power rail can eliminate the current difference caused by the extra load on #B0 AVDD, but the power rail adds extra devices which create more complexity and cost. Figure 2-5 shows a low-cost alternative configuration.

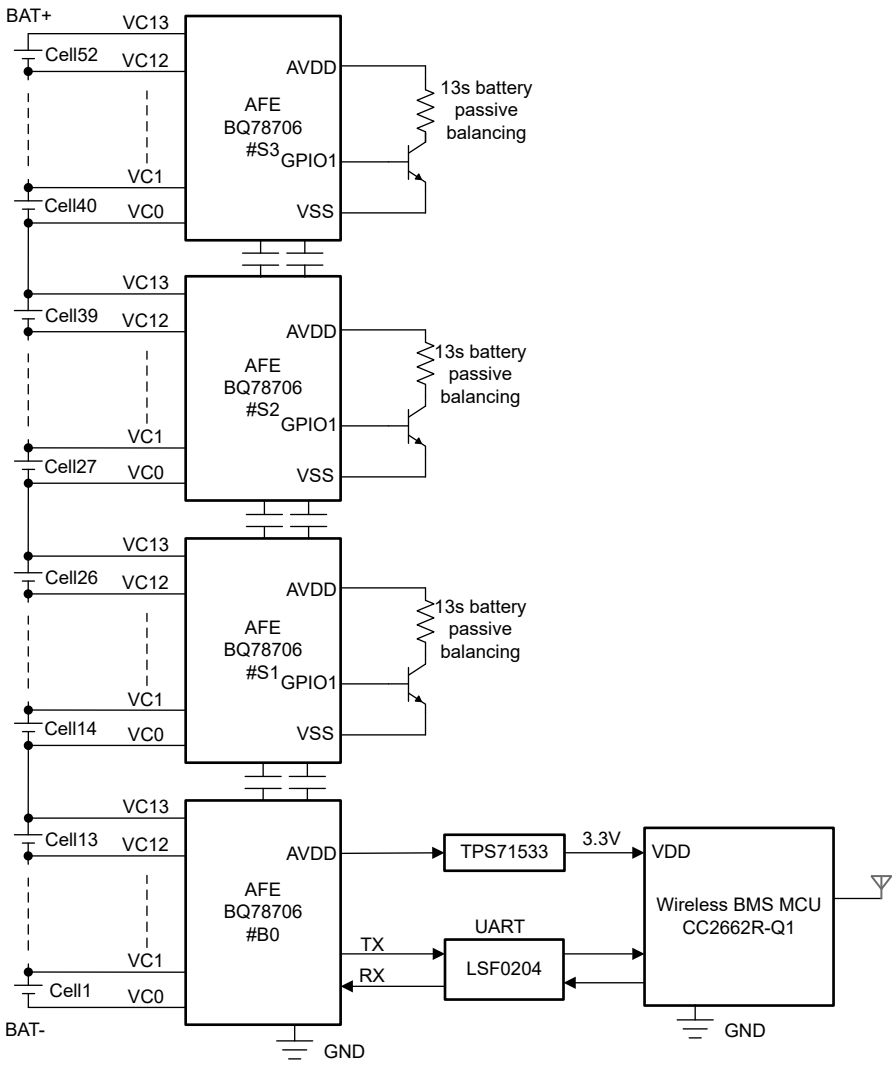


Figure 2-5. Low-Cost Power Strategy Option

BQ78706 AVDD allows a maximum 20mA external load, so the CC2662R-Q1, which only requires about 10mA peak supply current, can be powered directly from the AVDD. Three dummy resistive loads, controlled by the BQ78706 GPIO, are added to balance the current consumption.

2.2.3 Thermistor Multiplexer

Figure 2-6 shows the strategy of reading all thermistors and cell voltages. Two TMUX1308 devices are used to multiplex 14 thermistors and 2 constant resistors TS_R1 and TS_R2 to one BQ78706. The BQ78706 uses three GPIOs (GPIO9, GPIO10, and GPIO11) to address the 8 thermistor channels of the TMUX1308 and 2 GPIOs (GPIO7 and GPIO8) to read the common output pin from 2 TMUX1308 devices. This means 5 GPIOs can measure 16 thermistors.

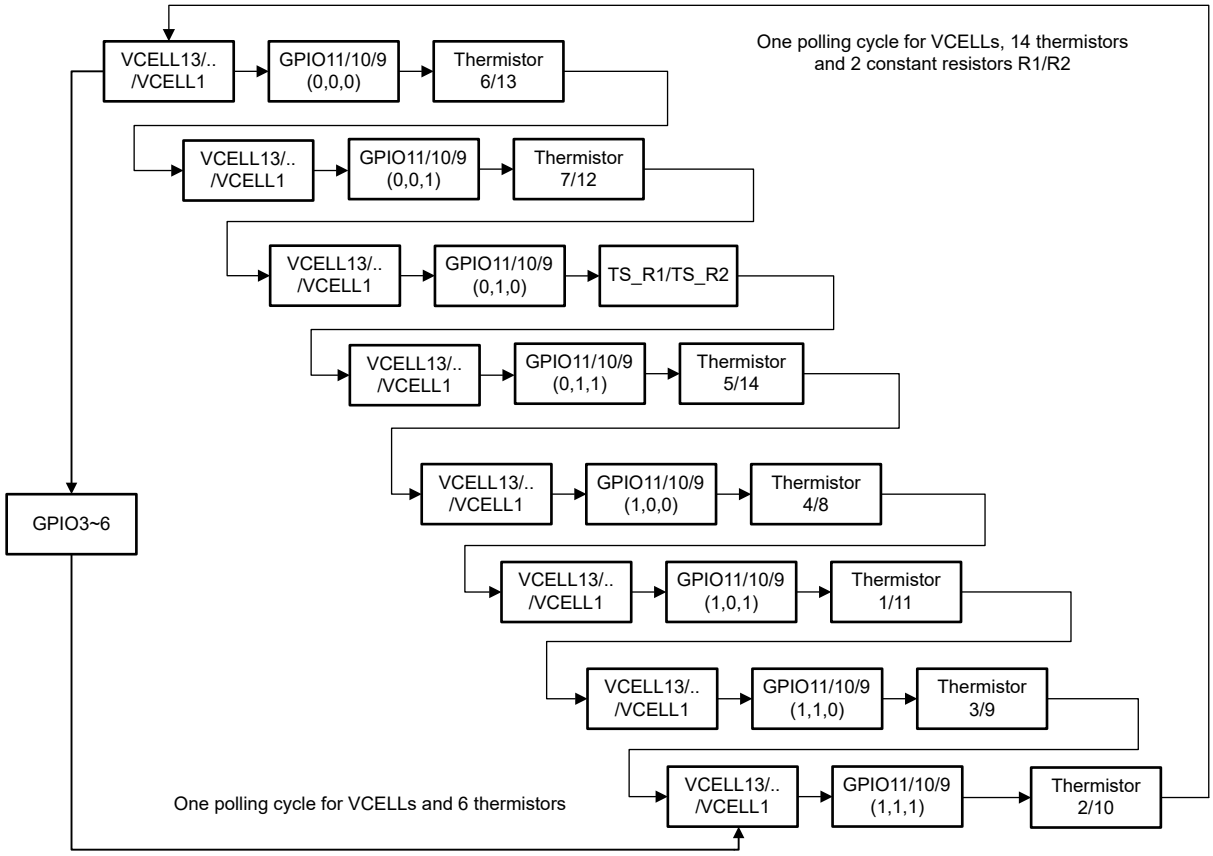


Figure 2-6. Multiplexer Control Logic

Although the number of thermistors can easily be increased using the TMUX1308 or a different multiplexer, the system still needs an efficient switching strategy to connect all thermistors in a safe time defined by regulation.

The loop of thermistor switching consists of a broadcast write to all the stacked BQ78706 GPIO9 to GPIO11 and a broadcast read of the GPIO7 and GPIO8 configured as ADC and OTUT inputs (ratiometric). The design needs 8 loops to read the temperature data from 14 thermistors and 2 constant resistors.

If the BESS rack voltage is 1500V, and one rack consists of 416 pieces of battery cells in series, then use 8 BMUs (32 BQ78706 devices) to monitor all the battery cells. Performing one loop to read temperature data from the stacked BQ78706 devices takes a longer time, which is likely to meet GBT34131-2023 standards (1s reading interval for all the thermistors).

2.2.4 Cell Balancing

Figure 2-7 shows the cell balancing circuit.

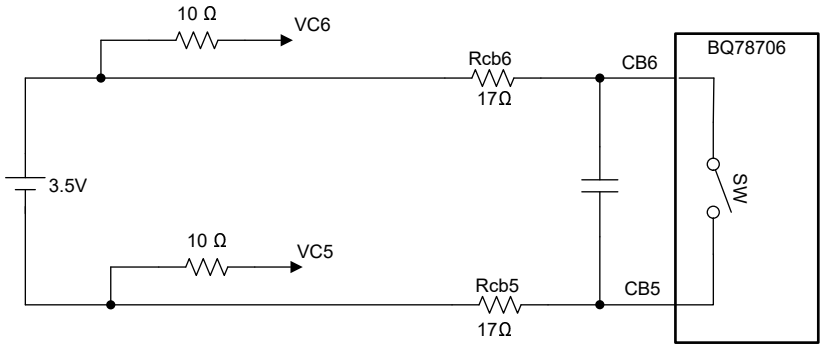


Figure 2-7. Cell Balancing Circuit

The design uses an internal field-effect transistor (FET) to achieve a 100mA balancing current. Assuming the given condition: an initial CB voltage of 3.5V, the final CB voltage is 3.3V. To achieve 100mA balancing current while the CB voltage is 3.5V; Rcb6 = Rcb5 = 17Ω is used.

2.3 Highlighted Products

2.3.1 CC2662R-Q1

The CC2662R-Q1 SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4F system CPU, which runs the application and the higher layers of the Wireless BMS protocol stack.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

The highlighted features of this device include:

- Support for *TI's SimpleLink™ wireless BMS (WBMS) protocol* for robust, low latency, and high throughput communication
- Functional Safety Quality-Managed classification including TI quality-managed development process and forthcoming functional safety FIT rate calculation, FMEDA, and functional-safety documentation
- AEC-Q100 qualified for Grade 2 temperature range (–40°C to +105°C) and is offered in a 7mm × 7mm VQFN package with wettable flanks
- Low standby current of 0.94µA with full RAM retention
- Excellent radio link budget of 97dBm

2.3.2 BQ78706

The BQ78706 provides high-accuracy cell voltage measurements for up to 14s battery modules in high-voltage battery management systems in energy storage systems (ESS), battery back-up unit (BBU), and portable power stations (PPS). This device has a state-of-the-art ADC architecture-measurement system meeting stringent safety requirements. With the daisy-chain isolated by transformer (or capacitor), the device is designed for centralized or distributed architectures in residential, commercial, or grid-scale energy storage systems.

2.3.3 TMUX1308

The TMUX1308-Q1 and TMUX1309-Q1 devices are general purpose complementary metal-oxide semiconductor (CMOS) multiplexers (MUX). The TMUX1308-Q1 is an 8:1, 1-channel (single-ended) MUX, while the TMUX1309-Q1 is a 4:1, 2-channel (differential) MUX. The devices support bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from GND to VDD.

The TMUX13xx-Q1 devices have an internal injection current control feature which eliminates the need for external diode and resistor networks typically used to protect the switch and keep the input signals within the supply voltage. The internal injection current control circuitry allows signals on disabled signal paths to exceed the supply voltage without affecting the signal of the enabled signal path. Additionally, the TMUX13xx-Q1 devices do not have an internal diode path to the supply pin, which eliminates the risk of damaging components connected to the supply pin or providing unintended power to the supply rail.

All logic inputs have 1.8V logic-compatible thresholds, providing both transistor-transistor logic (TTL) and CMOS logic compatibility when operating with a valid supply voltage. Fail-safe logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

2.3.4 LM5168

The LM5169 and LM5168 synchronous buck converters are designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components. A minimum controllable on time of 50ns facilitates large step-down conversion ratios, enabling the direct step-down from a 48V nominal input to low-voltage rails for reduced system complexity and design cost. The LM516x operates during input voltage dips as low as 6V, at nearly 100% duty cycle if needed, making the device an excellent choice for a wide input supply range industrial and high cell count battery pack applications. With integrated high-side and low-side power MOSFETs, the LM5169 delivers up to 0.65A of output current and the LM5168 delivers up to 0.3A of output current. A constant on-time (COT) control architecture provides nearly constant switching frequency with excellent load and line transient response. The LM516x is available in FPWM or auto mode versions.

FPWM mode provides forced CCM operation across the entire load range supporting isolated fly-buck converter applications. Auto mode enables ultra-low I_Q and diode emulation mode operation for high light-load efficiency.

2.3.5 TMP61

The *Thermistor Design Tool* offers the complete resistance versus temperature table (R-T table) computation and other helpful methods to derive temperature and example C-code.

The TMP61 linear thermistor offers linearity and consistent sensitivity across temperature to enable simple and accurate methods for temperature conversion. The low power consumption and a small thermal mass of the device minimize self-heating.

With built-in fail-safe behaviors at high temperatures and powerful immunity to environmental variation, these devices are designed for a long lifetime of high performance. The small size of the TMP6 series also allows for close placement to heat sources and quick response times.

Take advantage of benefits over NTC thermistors such as no extra linearization circuitry, minimized calibration, less resistance tolerance variation, larger sensitivity at high temperatures, and simplified conversion methods to save time and memory.

The TMP61 is currently available in a 0402 X1SON package, a 0603 SOT-5X3 package, and a 2-pin through-hole TO-92S package.

3 Hardware, Software, Testing Requirements, and Test Results

The key performances of this design are tested in a TI lab. This section describes the end equipment used and the test processes and results. Table 3-1 describes the hardware connections for the design board.

Table 3-1. Battery Connector J1_*n* (*n* = B0, S1, S2, S3)

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J1_*n* – 21	GND	System ground
J1_*n* – 1	TS1	Positive terminal of thermistor1
J1_*n* – 22	TS2	Positive terminal of thermistor2
J1_*n* – 2	TS3	Positive terminal of thermistor3
J1_*n* – 23	TS4	Positive terminal of thermistor4
J1_*n* – 3	TS5	Positive terminal of thermistor5
J1_*n* – 24	TS6	Positive terminal of thermistor6
J1_*n* – 4	TS7	Positive terminal of thermistor7
J1_*n* – 5	TS8	Positive terminal of thermistor8
J1_*n* – 25	GND	System ground
J1_*n* – 26	TS9	Positive terminal of thermistor9
J1_*n* – 6	TS10	Positive terminal of thermistor10
J1_*n* – 27	TS11	Positive terminal of thermistor11
J1_*n* – 7	TS12	Positive terminal of thermistor12
J1_*n* – 28	TS13	Positive terminal of thermistor13
J1_*n* – 8	TS14	Positive terminal of thermistor14
J1_*n* – 30	Module_N	BQ78706 ground
J1_*n* – 10	CELL0	Negative terminal of CELL1
J1_*n* – 31	CELL1	Positive terminal of CELL1
J1_*n* – 11	CELL2	Positive terminal of CELL2
J1_*n* – 32	CELL3	Positive terminal of CELL3
J1_*n* – 12	CELL4	Positive terminal of CELL4
J1_*n* – 33	CELL5	Positive terminal of CELL5
J1_*n* – 13	CELL6	Positive terminal of CELL6
J1_*n* – 34	CELL7	Positive terminal of CELL7
J1_*n* – 14	CELL8	Positive terminal of CELL8
J1_*n* – 35	CELL9	Positive terminal of CELL9
J1_*n* – 36	CELL10	Positive terminal of CELL10
J1_*n* – 16	CELL11	Positive terminal of CELL11
J1_*n* – 37	CELL12	Positive terminal of CELL12
J1_*n* – 17	CELL13	Positive terminal of CELL13
J1_*n* – 38	CELL14	Positive terminal of CELL14
J1_*n* – 18	CELL15	Positive terminal of CELL15
J1_*n* – 39	CELL16	Positive terminal of CELL16
J1_*n* – 19	CELL17	Positive terminal of CELL17
J1_*n* – 40	CELL18	Positive terminal of CELL18
J1_*n* – 20	Module_P	BQ78706 power
J1_*n* – 15	CELL_BB	Bus bar terminal

Table 3-2 provides the JTAG connections to wireless MCU.

Table 3-2. JTAG Connections

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J5–1	3V3_CC	3.3V power
J5–2	TMS	JTAG TMS port
J5–3,5,9	GND	Ground
J5–4	TCK	JTAG TCK port
J5–6	TDO	JTAG TDO port
J5–8	TDI	JTAG TDI port
J5–10	RST_CC	CC2662R-Q1 reset signal

3.1 Hardware Requirements

Table 3-3 summarizes the equipment used for testing.

Table 3-3. Test Equipment Summary

EQUIPMENT	MODEL OR DESCRIPTION
Multimeter	Agilent® 34401A
DC power supply	Agilent® 6030A
Debugger	LP-XDS110ET
Logic Analyzer	Kingst® LA5016

3.2 Software Requirements

This design requires the software development environment. This section contains the steps using the Code Composer Studio™ with wireless BMS SDK.

Use the following download links to access the software:

- CCSTUDIO: Code Composer Studio integrated development environment (IDE)
- SysConfig: System configuration tool
- Wireless BMS SDK:SIMPLELINK-WBMS-SDK

Once installation is complete, open CCSTUDIO and create a new workspace for importing the project. Before loading the software, the entire flash of all the CC2662R-Q1 devices needs be erased using TI's UNIFLASH software or another tool, including all protected sectors. This step is essential.

Read the wireless BMS user guide under the SDK folder before running the network.

3.3 Test Setup

Use the following procedures before running this design board. The design is constructed as 52s pack configurations. To simulate the 1500V battery rack configuration, eight design boards need to be stacked to support 416s battery cells that are simulated by resistor ladders powered by a DC source. The LAUNCHXL-CC26X2R1 development kit acts as a wireless main (WM) node to transfer commands from the serial port tool to the wireless command and then to the wireless device (WD) nodes.

Figure 3-1 shows the test setup for 1500V battery rack. During the tests, neither the design board nor CC2662R-Q1 device is shielded with wireless headphone and mouse working nearby as 2.4GHz interference.

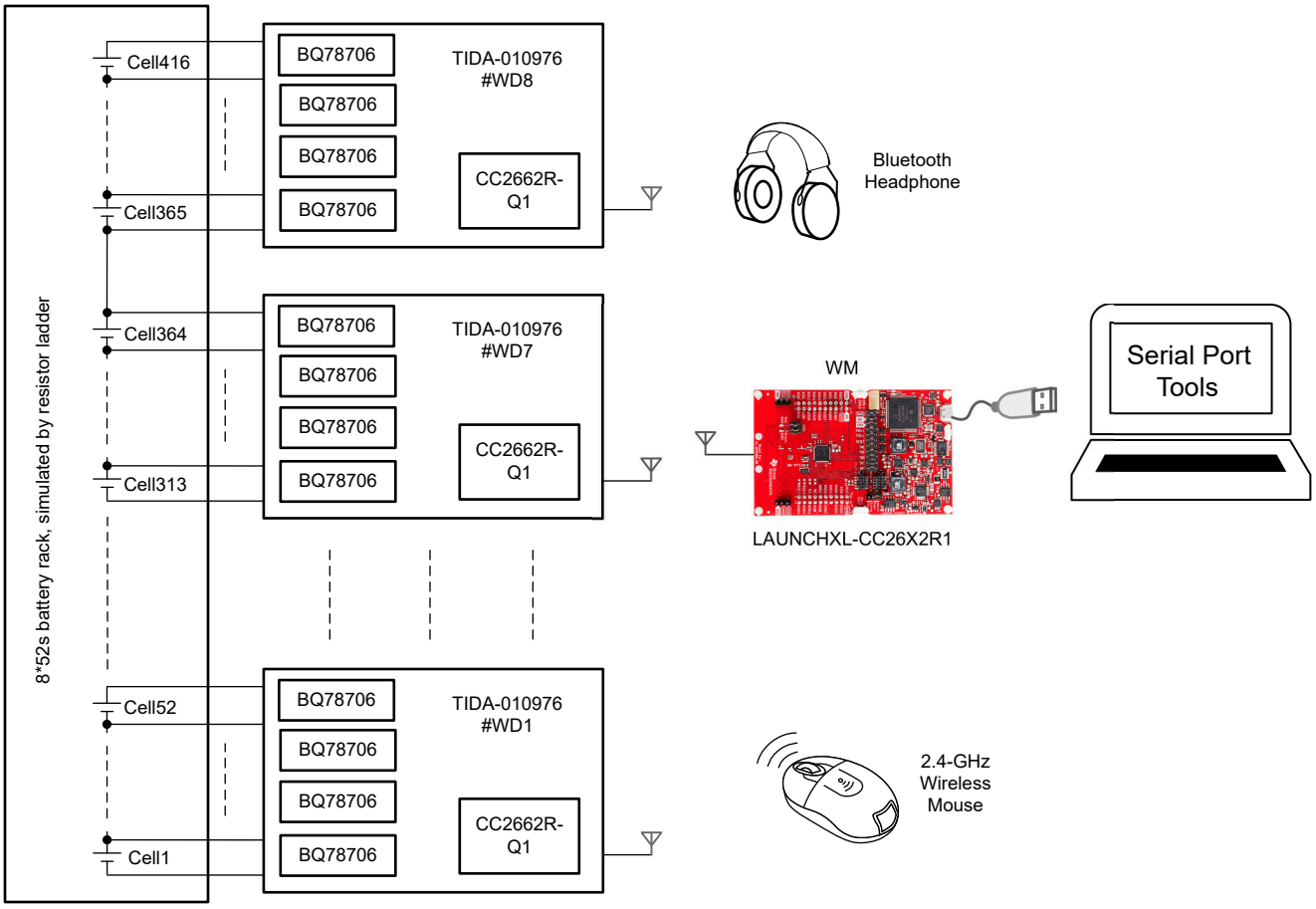


Figure 3-1. Test Setup for 1500V Battery Rack

3.4 Test Results

3.4.1 Network Performance

3.4.1.1 Network Initiation

The project level definition *Manual_network_start mode* is defined for WM and WD nodes. This allows host microcontroller to set network configurations manually.

The WM node utilizes TI's uNPI for serial communication with a host microcontroller. The uNPI frame format consists of the following fields:

- Start of Frame (SOF): Always 0xFE
- Length Field: Length in little-endian format (LSB first)
- Command Type: Type of command being sent
  - 0x3A: Synchronous Request
  - 0x5A: Asynchronous Request|Indication
  - ox7A: Synchronous Response
- Command ID: Opcode of the command being sent. Follow the detailed commands from the *Command Reference* section in wBMS user guide.
- Payload: Payload of variable length determined by length field
- Frame Check Sequence (FCS): Calculated by performing an XOR on each byte of the frame in the order sent or received on the bus. The SOF byte is always excluded from the FCS calculation.

Table 3-4. Host Packet Format

START BYTE	PAYLOAD LENGTH (LSB)	PAYLOAD LENGTH (MSB)	COMMAND TYPE	COMMAND ID	PAYLOAD	CHECKSUM
1B	1B	1B	1B	1B	Variable	1B
0xFE	0x01	0x00	0x3A	0x08	0x00	0x33

After loading the software, a serial port tool is used for testing. The following commands are sent from serial port tool to WM to bring up the network:

1. Reset WM node
2. Set network operation mode of the MAC
3. Set network main configurations
4. Set network joining mode to selective join or non-selective join
5. Set device configuration for selective joining if set selective join mode
6. Start network

About step 5, the MAC address of WD nodes are read by the FLASH-PROGRAMMER-2 tool. This design uses volatile operation mode and selective join mode for testing.

3.4.1.2 Network Latency

This design tests the latency of a host microcontroller sending commands to WM responding to the data. This includes the latencies involved in the UART interface between the host microcontroller and the WM node and the wBMS communication frame between WM and WD nodes.

The BQ78706 receives read/write commands from the host microcontroller forwarded by the WM node. The WM node broadcasts (or unicasts) the request to one or more WD nodes, which forward the command to the BQ78706. The BQ78706 processes the request and returns a response wrapped in a packet with data specific to each WD node. Each WD node receives the response from the BQ78706 and transmits the response back to the WM node. Delivering the request from the host microcontroller to the WM node and getting a response back typically takes 1–2 wBMS communication frames. The frame period depends on the number of WD nodes and the network configurations.

- The best case is 1 frame, if the WM node receives the host command right before frame starts
- The worst case is 2 frames, if the WM node receives the host command after the frame starts, as the WM node needs to wait for the next frame
- If there is a retransmission, then an extra frame needs to be added

The parameters in Table 3-5 are used for the latency tests.

Table 3-5. Network Configurations

ATTRIBUTE	LENGTH (B)	DATA	DESCRIPTION
networkID	2	0xDDDD	Network ID for the network
numULSlots	1	0x08	Number of devices in the network
ulSlotTime	1	90	Uplink slot duration in units of 16µs
dlSlotTime	2	310	Downlink slot duration in units of 16µs
minPNWDevices	1	=numULSlots	Minimum number of devices for Partial Network (PNW)
maxRetries	1	03	Maximum number of retries to send a data frame
keepAliveInt	1	17	Keep-alive interval
ul2dlTime	1	40	Uplink to downlink turn around time in units of 16µs
NumSkipRxInt(Reserved)	1	3	Number of skipped keep-alive intervals
DenyList	5	0xFFFFFFFF	Deny list of channel hopping sequence. Note: Make sure the number of data channels is ≥ 15

To test the latency, a broadcast voltage and GPIO read command with 168 bytes payload is sent from the serial port tool every 100ms. 168B bytes can include 52s cell voltage data and 8 GPIOs voltage data that are connected to the output of the thermistor multiplexer. The UART baud rate is 921600 bit/s.

Figure 3-2 shows the result without retransmission. The tested total latency is 39.2ms which means the WM node received the command after the frame started. The theoretical shortest length is 24.1ms.

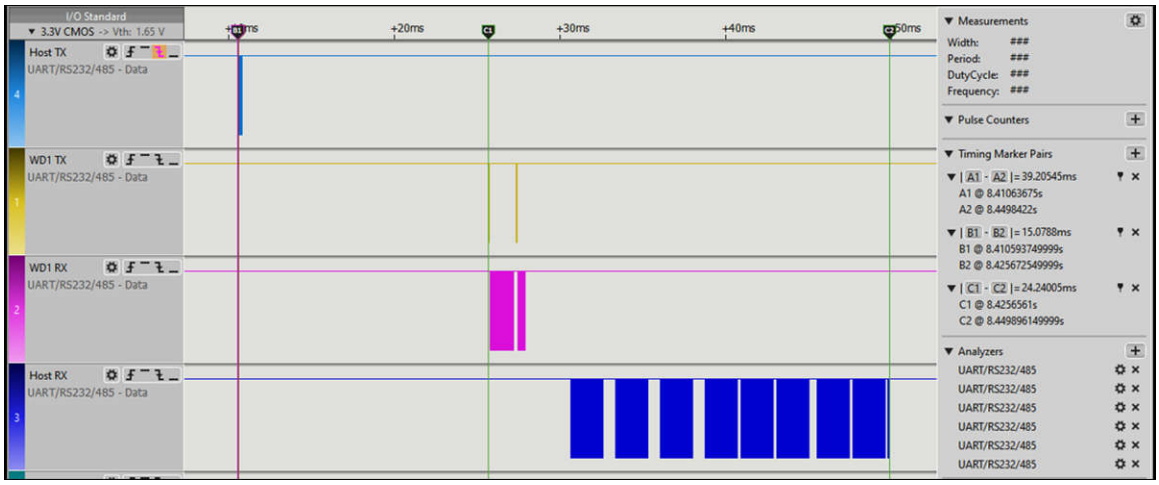


Figure 3-2. 168B Reading Latency Without Retransmission

To reliably deliver a packet, WM node retransmits a packet if the node does not receive an acknowledgment (ack) from the WD nodes. Figure 3-3 shows the result with 3 retransmissions. The tested total latency is 88ms which means the WM node received the command after the frame started. The theoretical shortest length is 72.9ms. Even with 3 retransmissions, the 416s cell voltage and 64 GPIO reading interval is less than 100ms.

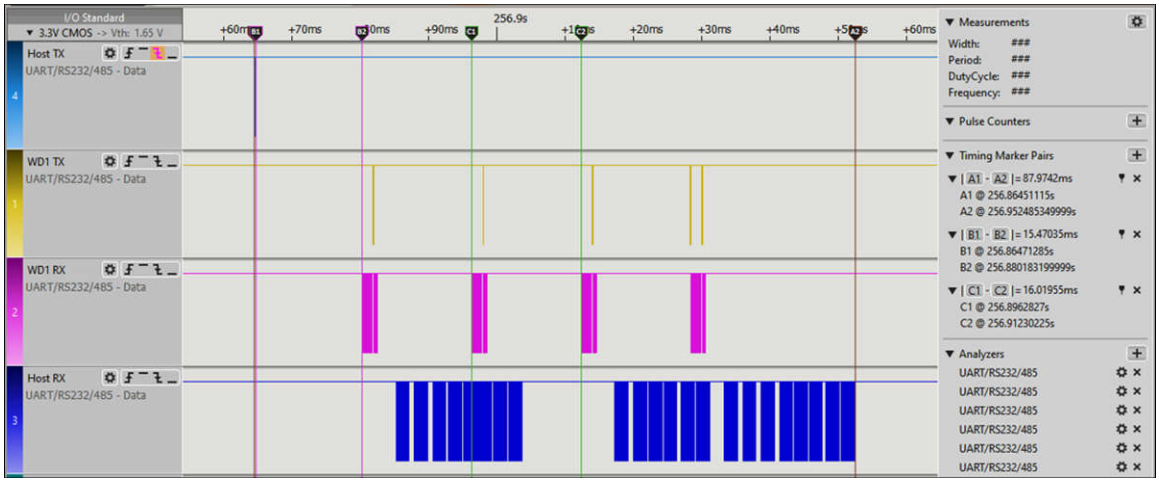


Figure 3-3. 168B Reading Latency With 3 Retransmissions

If more GPIO voltages need to be read every 100ms, the uplink and downlink slot duration need be extended for robust wireless communication. See the *configuring superframe and timing* section in wBMS user guide.

3.4.1.3 PDR, PS

To test the robustness of the wireless BMS network, measure the two network key performance indicator (KPI) parameters. The definitions are as follows:

1. *Path Stability (PS):* Path stability is the percentage of first time successfully received packets at each WD node divided by the total number of packets transmitted by the WM node.
   a. *Metric:* PS > 85%
   b. *Note:* Number of packets must be > 10000
2. *Packet Delivery Rate (PDR):* PDR is the percentage of packets successfully received at each WD node divided by the total number of packets transmitted by the WM node. This includes retransmissions needed within the 100ms interval.
   a. *Metric:* PDR > 99.9%
   b. *Note:* Number of packets must be > 10000

The three KPI are calculated from the data read by the statistic commands in the wBMS SDK. Calculate PDR of the node n using Equation 1.

$$\mathrm{PDR} = 1 - \frac{\mathrm{NumRxMissedPackets_n}}{\mathrm{NumTxSuccessPackets}} \tag{1}$$

where

- n is the number of WD nodes

Calculate PS of node n using Equation 1.

$$\mathrm{PS_n} = 1 - \frac{Sum(\mathrm{Retry_{1-3}})}{\mathrm{NumTxActualPackets}} \tag{2}$$

where

- *NumTxActualPackets* is calculated based on *NumTxSuccessPackets* plus the maximum number of retries for all WD nodes during each transmission
- *NumTxActualPackets* indicates the actual number of TX packets sent from RF physical layer

The PS and PDR test results of 30000 packets is shown in Table 3-6. The test results show good network robustness of this setup for 416s cells.

Table 3-6. PS and PDR Test Results

NODE	WD0	WD1	WD2	WD3	WD4	WD5	WD6	WD7
NumTxSuccessPackets	30001							
NumTxActualPackets	33095							
NumRxMissedPackets	0	0	0	0	0	0	0	1
Retry	225	710	560	643	465	341	609	1396
PDR	100%	100%	100%	100%	100%	100%	100%	99.997%
PS	99.320%	97.855%	98.308%	98.057%	98.595%	98.970%	98.160%	95.782%

3.4.1.4 Low-Power Mode

Wireless BMS protocol offers the ability to put the network into a keep-alive mode which is a low-power mode to minimize power consumption. In keep-alive mode, the WM node and WD nodes communicate intermittently at every specific interval specified by the configured amount of wBMS communication frames until the WM node resumes normal operation. The WD nodes can put BQ78706 into sleep or shutdown mode autonomously when entering keep-alive mode and wake up the BQ78706 immediately after exiting keep-alive mode.

With the configuration of this design, Figure 3-4 shows the current consumption of 3.3V power rail in keep-alive mode. The *INA229_239EVM* and a 10Ω series resistor is used to test the current. The average current consumption of 3.3V power rail is around 70µA.

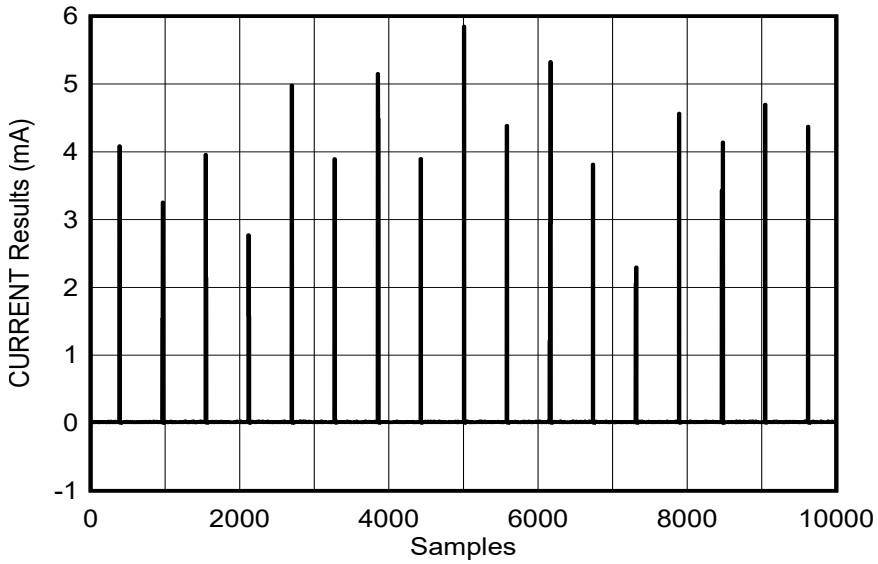


Figure 3-4. WD Node Power Consumption in Keep-Alive Mode

3.4.2 Cell Voltage Accuracy

This design *does not* do cell offset calibration to further improve the cell voltage accuracy since the BQ78706 already achieves ±2.4mV accuracy from –40°C to 125°C when using the LFP battery cell. The cell voltage accuracy is exactly the same with the BQ78706. Request the full BQ78706 data sheet Industrial 14-s stackable battery monitor, balancer and integrated protector compliant to ASIL-B to check the voltage accuracy specifications.

3.4.3 Temperature Sensing Using TMP61

Four TMP61 thermistors are used to verify the BMU temperature sensing function. This section focuses on how to use TMP61 to measuring the temperature with BQ78706.

In this design, GPIO3 to GPIO8 are configured as ADC and OTUT inputs (ratiometric). GPIO3 to GPIO6 are directly connected to TMP61 with 10kΩ pullup resistors. Using GPIO3 as an example, RT3 is the resistance of the TMP61 connected to GPIO3, RATIO3 is the GPIO3_RATIO reading data, R_{pull} is the 10kΩ pullup resistor, T3 is the temperature sensing by TMP61. Calculate RT3 using Equation 3.

$$\mathrm{RT3} = \frac{\mathrm{RATIO3}}{1 - \mathrm{RATIO3}} \times \mathrm{R_{pull}} \tag{3}$$

TMP61 provides the fourth order polynomial TMP. Calculate T3 using Equation 4.

$$\mathrm{T3} = \mathrm{A4} \times \mathrm{RT3}^4 + \mathrm{A3} \times \mathrm{RT3}^3 + \mathrm{A2} \times \mathrm{RT3}^2 + \mathrm{A1} \times \mathrm{RT3} + \mathrm{A0} \tag{4}$$

where

- A0 = –2.691712E+02, A1 = 5.062889E–02, A2 = –3.099051E–06, A3 = 1.153395E–10, A4 = –1.746912E-15

In the test, the BQ78706 GPIO3 reading data is 50.46%. The corresponding RT3 is 10185.71Ω. The temperature T3 is 28.1°C. To improve the temperature measurement accuracy of the TMP61, refer to the steps outlined in the *How to Achieve ±1°C Accuracy or Better Across Temperature With Low-Cost TMP6x Linear Thermistors* application note.

3.4.4 Thermistor Multiplexer Timing

The TMUX1308 is controlled by the command sent from WM. The test points for BQ78706#1 are found in Figure 3-5 including GPIO0, GPIO1, GPIO9, GPIO10, and GPIO11. The temperature sensing test software follows the steps in Figure 2-6.

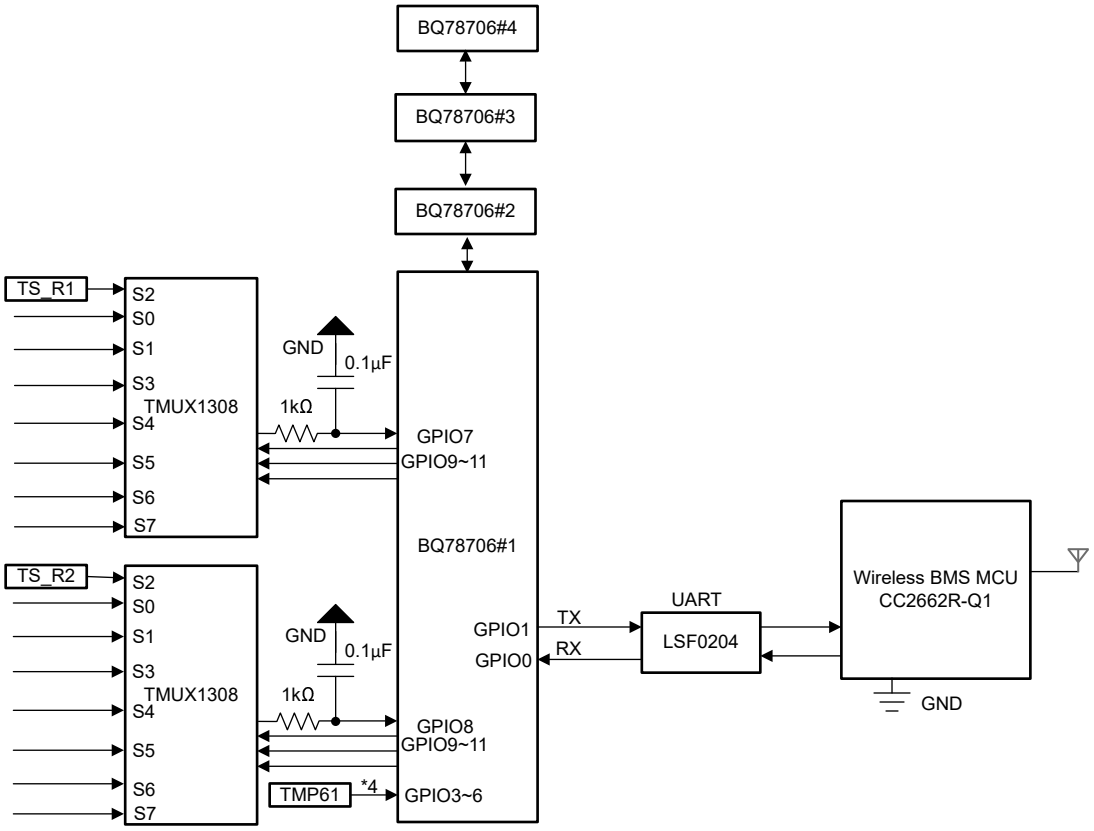


Figure 3-5. Test Setup for Temperature Sensing

Figure 3-6 shows the temperature sensing timings with MUX. This test is the polling cycle for 13 cell voltages, 14 thermistors, and 2 constant resistors.

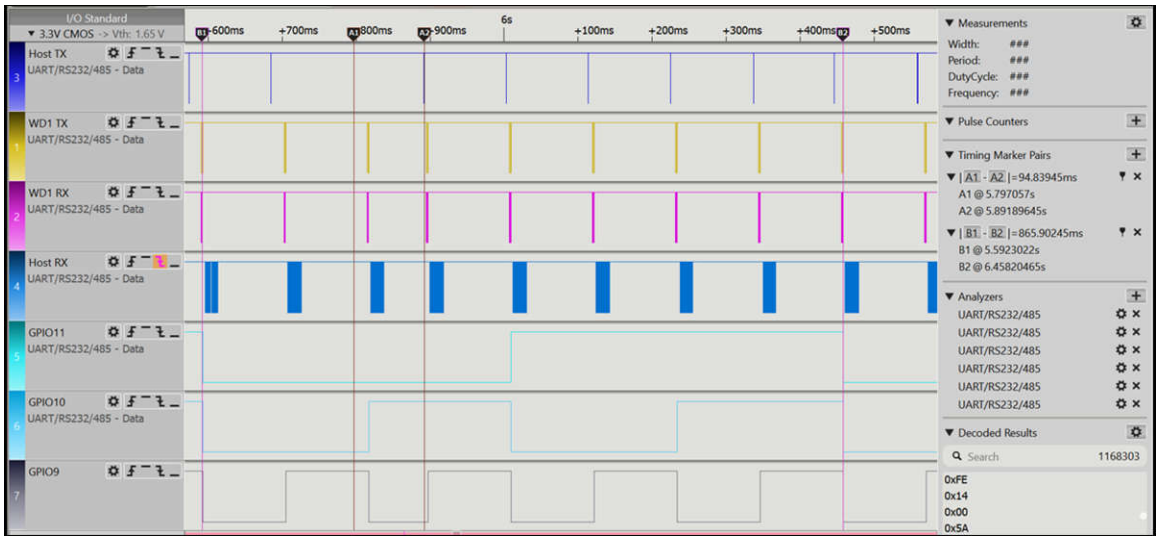


Figure 3-6. Temperature Sensing Timings With MUX

The test needs eight commands sent at 100ms interval to read all the thermistors. Each command contains a broadcast write to set TMUX1308 address lines and a broadcast read of 13 cell voltages, GPIO7 and GPIO8 ratios from all the 32 BQ78706 devices in the 8 WD nodes. The RS_R2 is connected in channel S2 and has a small resistance of 1kΩ that can be recognized by a ultra-low temperature reading. In Figure 3-5, eight steps transfer one by one and the duration from step 0 to step 7 is 865.9ms which is the maximum latency to read

all thermistors. To shorten the latency, the command needs to be sent with the interval less than 100ms. This process demonstrates that eight TMUX1308 status transfers work correctly.

Also, to avoid MUX settling transients that can affect the GPIO voltage measurement, the broadcast read needs to be sent before the broadcast write command that is used to set address lines. Then, the next broadcast read has steady GPIO voltages after the 100ms interval.

3.4.5 Current Consumption

Figure 3-7 shows the test setup for current consumption. Two working modes are tested including keep-alive mode and active mode. VSS line of #S1–3 BQ78706 and BAT line of #B0 BQ78706 are selected as a test point for current measurement to test the current consumption of each BQ78706. Also, the input and output current of power rail are tested to show the performance of the power rail. In both modes, the resistor ladder is powered by a DC source which is set to 63V and 150V to simulate the real cell. A 6.5 digit multimeter is used to measure the voltage across the series resistors. The multimeter is configured to slow mode and 10GΩ input resistor to have the best accuracy.

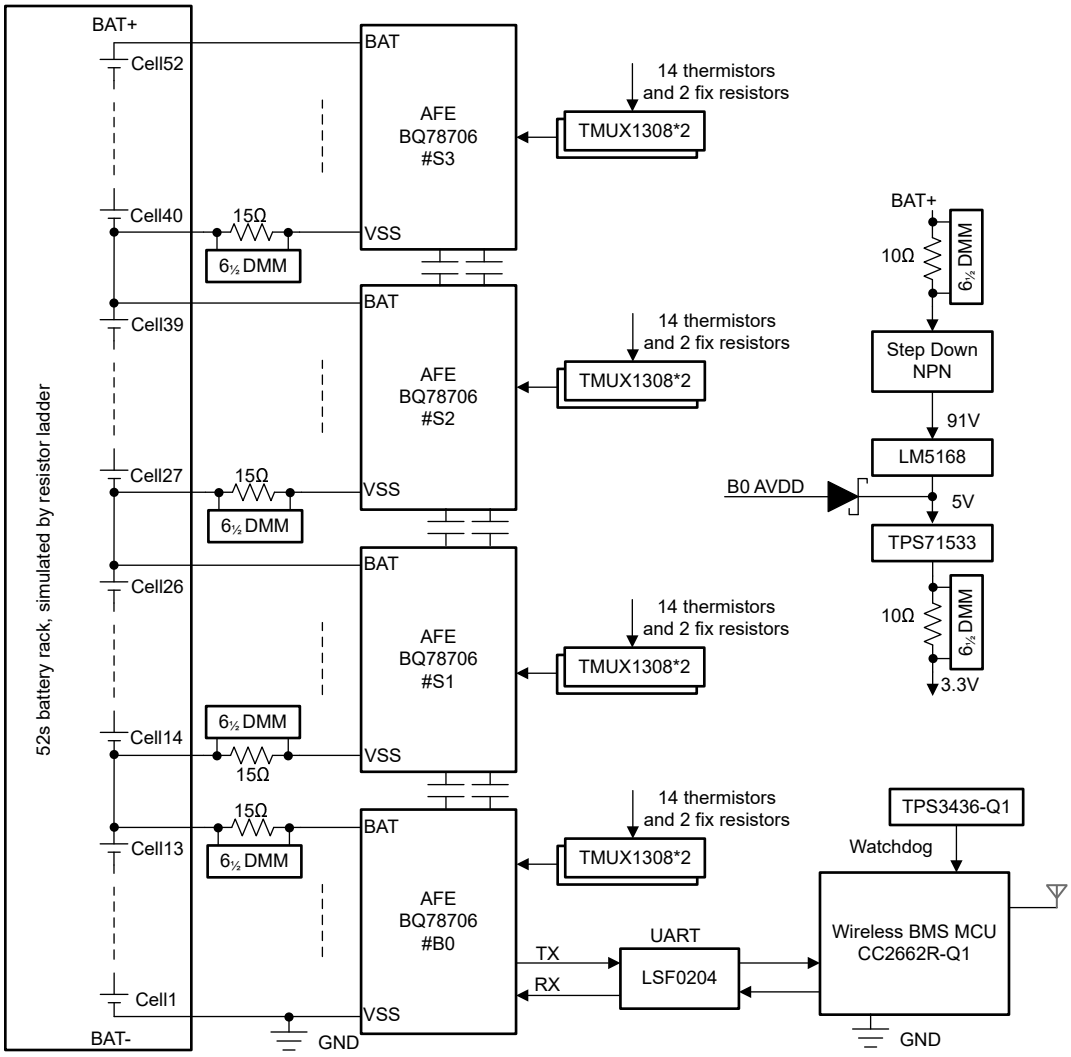


Figure 3-7. Test Setup for Current Consumption

In active mode, the WM sent a polling command with 168B payload from each WD node. In keep-alive mode, the BA78706 works in shutdown mode to minimize power consumption.

Table 3-7 shows the BMU current consumption test results.

Table 3-7. Current Consumption Test Results

INPUT VOLTAGE	TEST POINT	POWER RAIL INPUT	POWER RAIL OUTPUT	#B0	#S1	#S2	#S3
	WORKING MODE	AVG	AVG	AVG	AVG	AVG	AVG
63Vdc	Active	558.6µA	2.67mA	11.32mA	11.47mA	11.23mA	11.29mA
	Keep-alive	37.3µA	70.7µA	32.6µA	3.0µA	3.0µA	3.0µA
150Vdc	Active	274.2µA	2.67mA	11.35mA	11.49mA	11.24mA	11.32mA
	Keep-alive	32µA	70.6µA	32.0µA	3.5µA	3.3µA	3.2µA

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010976.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010976.

4.1.3 Layout Prints

To download the layer plots, see the design files at TIDA-010976.

4.2 Tools and Software

Tools

LM5169 Quick Start Calculator	LM5163 and LM5164 converter quickstart design tool
INA229_239EVM	INA229 and INA239 evaluation module
Thermistor Design Tool	TMP6-THERMISTOR-DESIGN

Software

CCSTUDIO	Code Composer Studio™ integrated development environment (IDE)
FLASH-PROGRAMMER-2	SmartRF Flash Programmer
UNIFLASH	UniFlash flash programming tool

4.3 Documentation Support

1. Texas Instruments, *CC13xx/CC26xx Hardware Configuration and PCB Design Considerations Application Note*
2. Texas Instruments, *Crystal Oscillator and Crystal Selection for the CC13xx, CC26xx, CC23xx, and CC27xx Family of Wireless MCUs Application Note*
3. Texas Instruments, *2.4GHz Inverted F Antenna Application Note*
4. Texas Instruments, *How to Achieve ±1°C Accuracy or Better Across Temperature With Low-Cost TMP6x Linear Thermistors Application Note*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

4.5 Trademarks

TI E2E™, SimpleLink™, and Code Composer Studio™ are trademarks of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
Arm® and Cortex® are registered trademarks of Arm Limited.
Agilent® is a registered trademark of Agilent Technologies Inc.
Kingst® is a registered trademark of Qingdao Kingst Electronics Co., Ltd.
All trademarks are the property of their respective owners.

5 About the Author

KIAN LIN, system engineer from the SEM Industrial Energy Infrastructure team, focuses on battery pack and energy storage system applications to address industrial battery pack design challenges.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265