Design Guide: TIDA-050095

48V–12V GaN-Enabled 2kW Four-Phase Buck Converter, One-Fourth Brick Power Module Reference Design

Description

This reference design is a 2kW, high-density, 48V to 12V closed-loop bus converter based on a four-phase buck for enterprise computing. The design achieves > 98% peak efficiency and 97.5% full load efficiency at 48V VIN. The design uses the LMG3100R017, one of TI's high-performance gallium nitride (GaN) power stage devices. The control circuitry uses the UCD3138A, a high-performance microcontroller in a 40-pin quad flat no-lead (QFN) package.

Resources

TIDA-050095	Design Folder
TIDA-050089	Design Folder
LMG3100R017	Product Folder
UCD3138A	Product Folder
TPSM365R6	Product Folder

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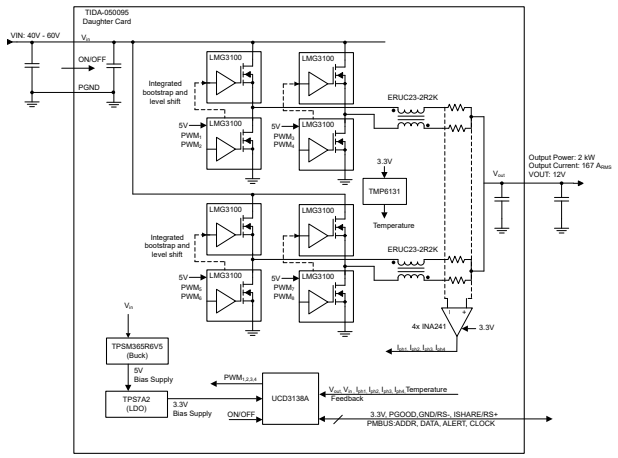
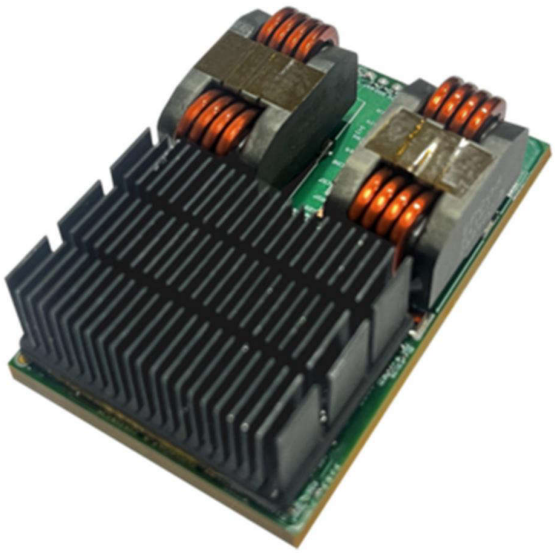
Features

- High power density with a high peak (98%+) and full load efficiency (97.5%)
- Transformer-less regulated topology
- Low bill of materials (BOM) cost
- Easy to implement in a chip-down design in quarter brick form factor (36.8mm × 58.4mm × 18mm)
- 12V–48V boost configurable
- PMBus® compatible

Applications

- Rack server motherboard
- High performance computing
- DC/DC modules
- Low-voltage battery system





1 System Description

Server power requirements increase with the proliferation of AI and increased data processing loads. The architecture shifts to a higher voltage for distribution, 48V, from 12V, to reduce I²R losses. This shift requires conversion of the 48V–12V levels on the motherboard to power the main controller multiphase power stage and peripherals, such as PCIe and HDD.

The buck converters are not efficient enough to achieve 98%+ peak efficiency due to hard-switching. However, TI GaN integrated power stages enable efficient 48V–12V conversion with a 2kW power output using a four-phase buck topology.

1.1 Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage	40V–60V DC
Output voltage	12V DC Regulated
Rated output power	2kW
Maximum output current	$167A_{RMS}$
Board Size (W × L × H)	36.8mm × 58.4mm × 18mm

1.1.1 General TI High Voltage Evaluation User Safety Guidelines

Always follow TI's set-up and application instructions, including the use of all interface components within the recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and the safety of those working around you. Contact TI's Product Information Center at http://support/ti./com for further information.

Note

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions can result in personal injury, property damage, or death due to electrical shock and/or burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed PCB (printed circuit board) assembly. It is intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise, and knowledge of electrical safety risks in development and application of high-voltage electrical circuits. Any other use or application is strictly prohibited by Texas Instruments. If you are not suitably qualified, you must immediately stop from further use of the HV EVM.

- **Work Area Safety:**
  - Maintain a clean and orderly work area.
  - Qualified observers must be present anytime circuits are energized.
  - Effective barriers and signage must be present in the area where the TI HV EVM and the interface electronics are energized; indicating operation of accessible high voltages can be present for the purpose of protecting inadvertent access.
  - All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50 VRMS/75 VDC must be electrically located within a protected Emergency Power Off (EPO) power strip.
  - Use a stable and non-conductive work surface.
  - Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
- **Electrical Safety:**
  - As a precautionary measure, a good engineering practice to assume that the entire EVM can have fully accessible and active high voltages.
  - De-energize the TI HV EVM and all the inputs, outputs, and electrical loads before performing any electrical or other diagnostic measurements. Confirm that TI HV EVM power has been safely de-energized.
  - After confirming the EVM is de-energized, proceed with the required electrical circuit configurations, wiring, measurement equipment hook-ups, and other application needs while still assuming the EVM circuit and measuring instruments are electrically live.
  - When EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or the electrical circuits as the EVM or the electrical circuits can be at high voltages capable of causing electrical shock hazard.

- **Personal Safety:**
  - Wear personal protective equipment like latex gloves and safety glasses with side shields, or protect the EVM from accidental touch in an adequate translucent plastic box with interlocks.
- **Limitation for Safe Use:**
  - EVMs are not to be used as all or part of a production unit.

1.1.1.1 Safety and Precautions

The EVM is designed for professionals who have received the appropriate technical training and is designed to operate from an AC power supply or a high-voltage DC supply. Read this user guide and the safety-related documents that come with the EVM package before operating this EVM.

CAUTION

Do not leave the EVM powered when unattended.

WARNING

Hot surface! Contact can cause burns. Do not touch!

WARNING

High Voltage! Electric shock is possible when connecting board to live wire. Board must be handled with care by a professional.
For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

2 System Overview

2.1 Block Diagram

The reference design uses the LMG3100R017, a small-size GaN field-effect transistor (FET), for a three-phase inverter. The LMG3100R017 integrates the driver and 80V GaN FET in a 6.5mm × 4mm QFN package. This package is optimized for extremely low gate loop and power loop impedance. The PCB offers mounting holes for a heat sink with the top-side cooled LMG3100R017 GaN-FET power modules. An integrated bootstrap diode reduces space for the high-side GaN-FET bias supply.

The control uses the UCD3138A, a digital power supply controller from Texas Instruments. The UCD3138A offers excellent levels of integration and performance in a single-chip solution. The UCD3138A has PMBus communication, which enables easy firmware upgrade and reporting. The design monitors each phase input current through a bidirectional current sense amplifier, the INA241. The 5V auxiliary supply uses an integrated buck module, the TPSM365R6, followed by a low-dropout (LDO) linear regulator to generate a 3.3V rail.

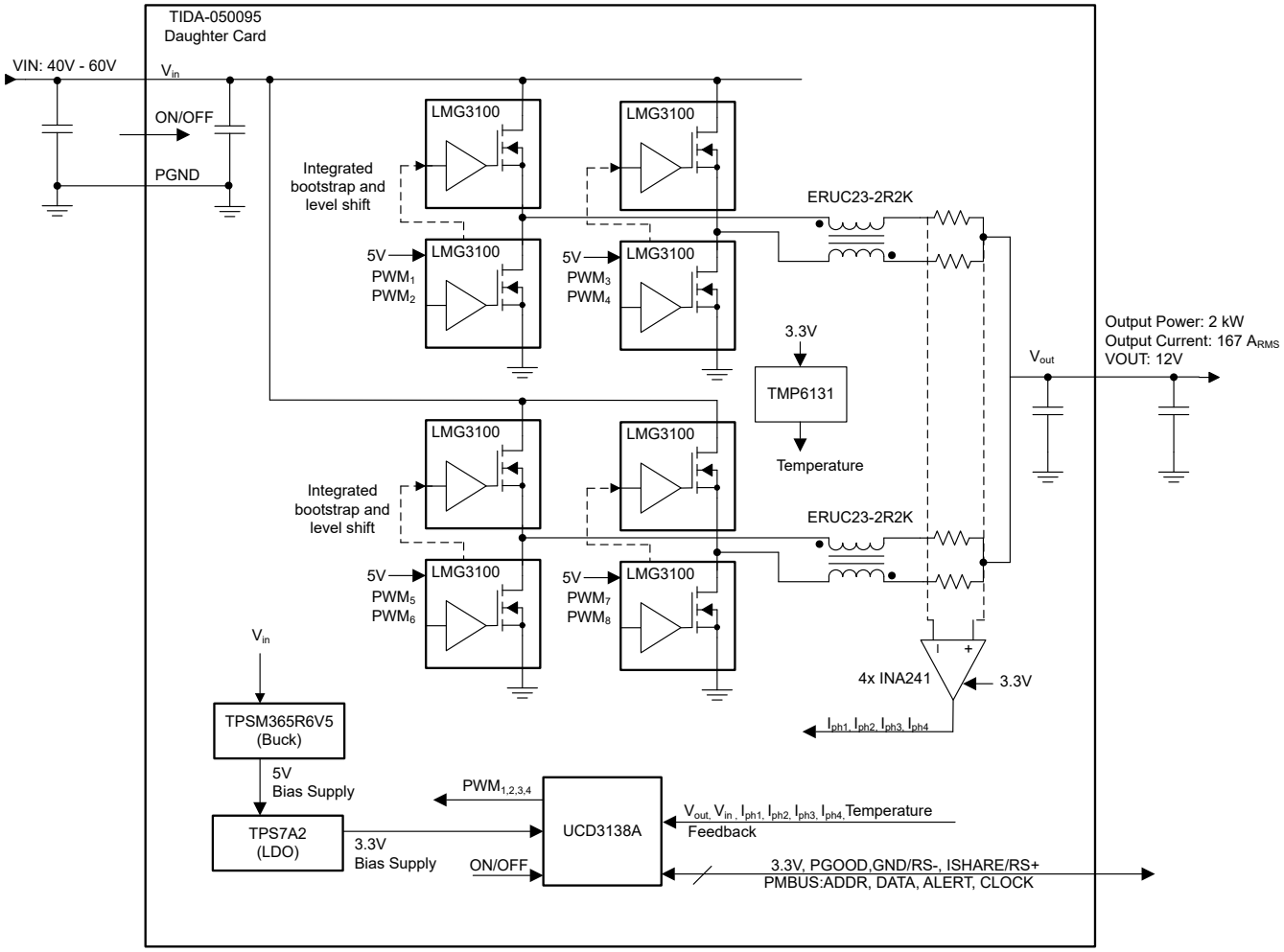


Figure 2-1. System Block Diagram

2.2 Design Considerations

To realize the 48V–12V conversion in a quarter-brick form factor (36.8mm × 58.4mm), component selection is crucial. This section describes the cognitive processing behind each part selection.

2.2.1 GaN Power Stage

TI GaN power stages play a crucial role in this size-competitive module space due to the integrated FET + driver and the capability of higher switching, which reduces passive size. To deliver power up to 2kW and meet >

98.1% efficiency at mid-load, a four-phase interleaved design is considered with 1.7mΩ $R_{DS(on)}$. The LMG3100 provides different $R_{DS(on)}$ variants in the same package, making it easy to tune the efficiency at different load and frequency conditions.

2.2.2 Inductor

To deliver 2kW total power, each phase inductor must support 42A current. The inductor must also support higher saturation current, depending on the inductor current ripple and derating. Choose a low-Direct Current Resistance (DCR) inductor to reduce conduction losses that affect full load efficiency. The inductor size is another constraint. Four inductors must fit within a 36.8mm dimension to achieve a streamlined power flow across a 58.4mm dimension.

The smallest catalog, single inductors with these ratings occupy a large board area. To address this issue, the design uses the ERUC23-2R2K coupled inductor from TDK®. In a coupled inductor, both phases share the same part of the core. Negative magnetic coupling between the two phases occurs, resulting in ripple cancellation. This provides an added benefit of ripple cancellation at the output due to multiphasing.

For higher power and higher saturation rating for peak power delivery, choose a lower inductance value with a smaller DCR. An increase in the switching frequency can be required to reduce the ripple and switching losses in GaN.

The coupled inductor design offers several benefits:

- Reduced current ripple: Magnetic coupling between phases enables significant ripple current cancellation, resulting in lower current ripple throughout the circuit.
- Increased efficiency: Lower ripple currents reduce I_{RMS} losses in GaN FETs, inductors, and PCB traces, helping improve converter efficiency overall.
- Faster transient response: Lower inductance can be used for the same ripple, meaning a coupled inductor design allows for faster response to load changes, often reducing the need for bulky output capacitors.
- Space and size savings: Using a single core for multiple windings means less board area and potentially smaller magnetics for the same current ratings.

2.2.3 Controller

The UCD3138A meets the following requirements:

- Intermediate bus converter (IBC) modules require precise control and fault protection and reporting to the main MCU using the PMBus protocol
- Detection of input undervoltage lockout (UVLO), output overvoltage protection (OVP), overcurrent protection (OCP), and overtemperature protection (OTP) faults
- Closed-loop design based on input current and output voltage sense
- Current sharing between different modules for paralleling modules
- Current balancing between phases is equally important, because current balancing provides even power loss and better efficiency

Although not all the features mentioned are implemented in this design, the hardware design is compatible with implementing these features through a firmware change.

2.2.4 Cooling

One of the major aspects of this design is to dissipate heat efficiently through a heat sink and fan. This design uses the Z35-12.7B heat sink from *Alpha Novatech*, which has approximately 2.2°C/W thermal resistance at 200 linear feet per minute (LFM) air flow. The design also uses a 1mm-thick thermal interface material (TIM) with 6W/m-K thermal conductivity. Using a thinner TIM can improve heat dissipation, provided there is enough distance between the heat sink and the LMG3100R017 exposed GaN die and capacitors for electrical isolation.

2.2.4.1 Heat Sink Placement

For good cooling through the top-side exposed GaN die, provide for the minimum distance from the GaN die to the heat sink. To achieve this, components closer to the LMG3100R017 must have a similar height to the LMG3100R017, allowing the thermal interface material (TIM) thickness to be minimized. Wherever the component height exceeds that of the LMG3100R017, add a groove to the heat sink to compensate for the difference.

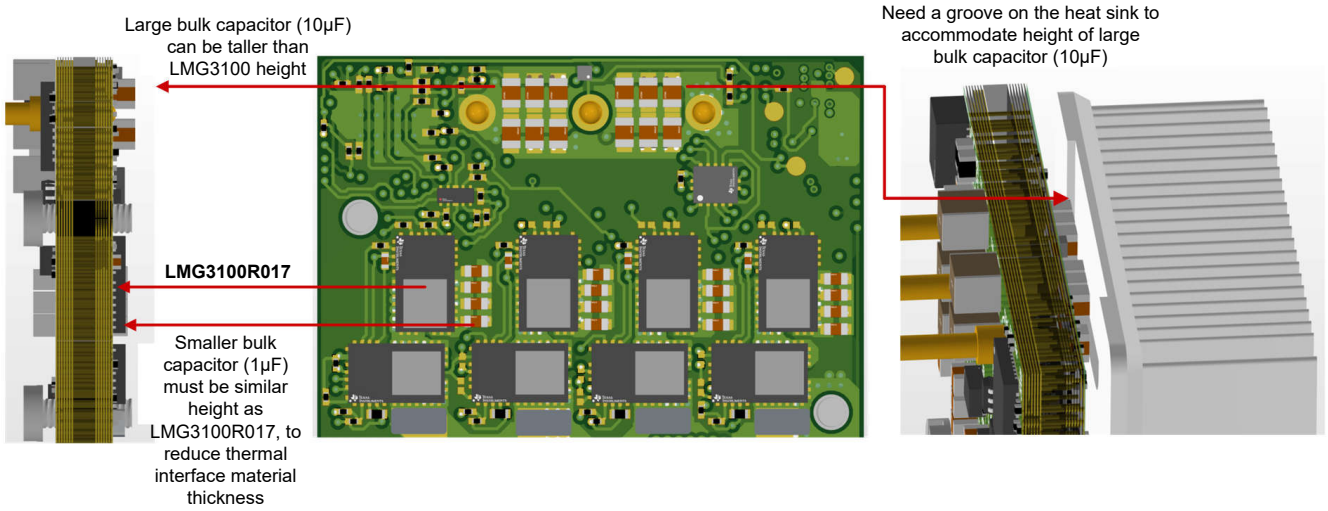


Figure 2-2. Capacitor Placement and Heat Sink Groove

2.2.4.2 Via Placement

In addition to top-side cooling with a heat sink, removing heat from the board is essential. To achieve this, use plated vias on pads to transfer current to inner layers and reduce overall thermal resistance. Make sure that sufficient vias are added to transfer current to multiple layers and minimize overall PCB copper loss.

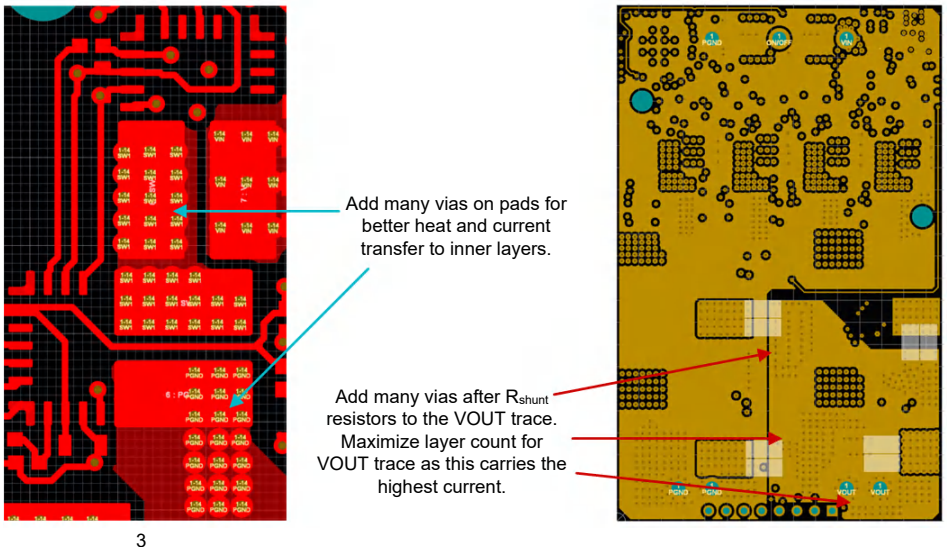


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Figure 2-3. Via Placement

2.2.4.3 Copper Block

At full load, the synchronous rectification (SR) FET carries a significant amount of current. Removing heat from the SR FET is essential to achieve better efficiency. The PGND copper can be exposed near the SRC pad of the low-side LMG3100R017. A small copper block, with the same height as the LMG3100R017, can be used and then attached to the heat sink.

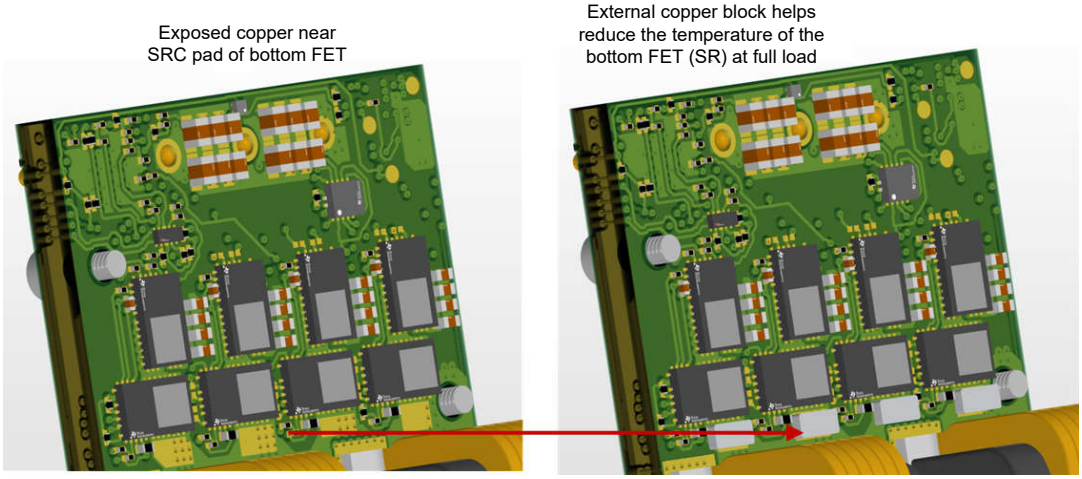

Figure 2-4. Copper Block Placement

2.3 Highlighted Products

The following highlighted products are used in this reference design. Key features for selecting the devices for this reference design are revealed in the following sections. Find more details of the highlighted devices in the respective product data sheet.

2.3.1 LMG3100R017

The LMG3100 device is a 100V, 97A Gallium Nitride (GaN) FET with integrated driver. The device consists of a 100V GaN FET driven by a high-frequency GaN-FET driver.Table 2-1 details the key features and benefits for this design.

Table 2-1. Key Features and Benefits of LMG3100R017 in TIDA-050089

FEATURE	BENEFIT
Integrated 1.7mΩ, 90V GaN FET for 97A operation	Low $R_{DS(on)}$ enables lower conduction loss is SR FET
Integrated GaN FET and GaN driver	Minimized package parasitic elements enable ultra-fast switching for reduced switching losses. Enables small design in quarter brick form factor
LMG3100 incorporates a high-side level shifter and bootstrap circuit	Two LMG3100 devices can be used to form a half bridge without needing an additional level shifter and bootstrap diode
Single 5V gate driver supply with bootstrap voltage clamping and undervoltage lockout	Easy power management. UVLO provides simultaneous shutdown of high-side and low-side GaN FET in case of gate driver undervoltage
LMG3100 optimized pinout	Easy PCB layout with minimum inductance for reduced switching losses
Two exposed GaN dies on top (SW and PGND)	Realize lower top thermal resistance. Accepts both sides cooling, enabling easy thermal design
LMG3100 provides different $R_{DS(on)}$ variants in same package	Easy to replace the devices in the case of efficiency tuning at mid-load and full-load

2.3.2 UCD3138A

The UCD3138A is a fully-programmable, power-optimized digital controller design that offers the benefits of a simple design to speed up time to market while maintaining ample ability to develop high-performing and well-differentiated power-supply designs. Along with the general purposes of a microcontroller, the device is built to include a configurable digital state machine optimized to meet the performance requirements of telecom and server isolated power applications. The controller features optimized digital hardware for implementing many cutting edge power management functions such as burst mode, ideal diode emulation, mode switching, synchronous rectification, and reduced constant current consumption. In summary, the UCD3138A addresses all key concerns such as high efficiency across the entire operating range, high degree of flexibility for various control schemes and topologies, high integration for increased power density, high reliability, and lowest overall system cost.

Other key features include:

- Digital control of up to three independent feedback loops
- Up to 16MHz error analog-to-digital converter (EADC)
- Up to eight high-resolution digital pulse width modulated (DPWM) outputs
- Fully-programmable, high-performance, 31.25MHz, 32-bit ARM7TDMI-S™ processor
- 14-channel, 12-bit, 267-kSPS general purpose ADC with integrated filters
- Communication peripherals (I²C/PMBus, UART)
- Configurable pulse width modulation (PWM) edge movement
- Configurable feedback control
- Configurable modulation methods
- Fast, automatic, and smooth mode switching
- High efficiency and light load management
- Soft start and stop with and without pre-bias
- Fast input voltage feed forward hardware
- Rich fault protection options
- Internal temperature sensor
- Timer capture with selectable input pins
- Up to five additional general purpose timers
- Built-in watchdog: brown-out detection (BOD) and power on reset (POR)
- Operating temperature: –40°C to 125°C

2.3.3 TPSM365R6V5

The TPSM365R6 is an easy-to-use, synchronous buck, DC-DC power module that operates from a 3V to 65V supply voltage. The device is intended for step-down conversions from 5V, 12V, 24V, and 48V supply rails. With an integrated power controller, inductor, and MOSFETs, the TPSM365R6 or TPSM365R3 delivers up to 600mA DC load current with high efficiency and ultra-low input quiescent current in a very small design size. Although designed for simple implementation, this device offers flexibility to optimize the usage according to the target application. Control-loop compensation is not required, reducing design time and external component count. The TPSM365Rx can operate over a wide range of switching frequencies and duty ratios. If the minimum ON-time or OFF-time cannot support the desired duty ratio, the switching frequency gets reduced automatically, maintaining the output voltage regulation. With the right internal loop compensation the system design time with the TPSM365Rx reduces significantly with minimal external components. In addition, the PGOOD output feature with built-in delayed release allows the elimination of the reset supervisor in many applications. With a programmable switching frequency from 200kHz to 2.2MHz using the RT pin or an external clock signal. These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for a simple layout, requiring few external components.

2.3.4 TMP61

The TMP61 is a positive temperature coefficient (PTC) linear silicon thermistor. The device behaves as a temperature-dependent resistor, and can be configured in a variety of ways to monitor temperature based on the system-level requirements. The TMP61 has a nominal resistance at 25°C of 10kΩ with ±1% maximum tolerance, a maximum operating voltage of 5.5V, and maximum supply current of 400µA. The benefits of this device include no extra linearity circuitry, minimized calibration, less resistance toleration variation, larger sensitivity at high temperatures, and simplified conversion methods to save time and memory in the processor. This device can be used in a variety of applications to monitor temperature close to a heat source with the very small DEC package option compatible with the typical 0402 footprint.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

- Base board with:
  - VIN input and VOUT output connector
  - Input and output capacitors
  - PMBus connector
  - Test points for VIN, VOUT measurement
  - 5V, 3.3V bias supply (to flash the code when VIN is not applied)
- Horizontal mount card:
  - Four-phase buck power stage with auxiliary power and controller
- USB-2-GPIO connector
- 100V, 60A programmable DC source
- 12V, 180A programmable DC load
- Air cooling fan

3.2 Software Requirements

- Code Composer Studio™ integrated development environment (IDE)
- Fusion Digital Power Design (Fusion GUI)

3.3 Test Setup

Complete the following steps for the test setup:

1. Insert the daughter card module into the base board.
2. Connect the 100V DC voltage source to the base board connector (J3-J4). Set the input voltage ranges from 40V to 60V with current limit as 60A.
3. Place the fan near the heat sink and turn the fan on.
4. Connect the programmable DC load (J2-J6).
5. Connect the PMBus adapter to J9 and upload the firmware to UCD3138A (optional).
6. Turn on the DC source and increase the constant current (CC) load up to 167A.

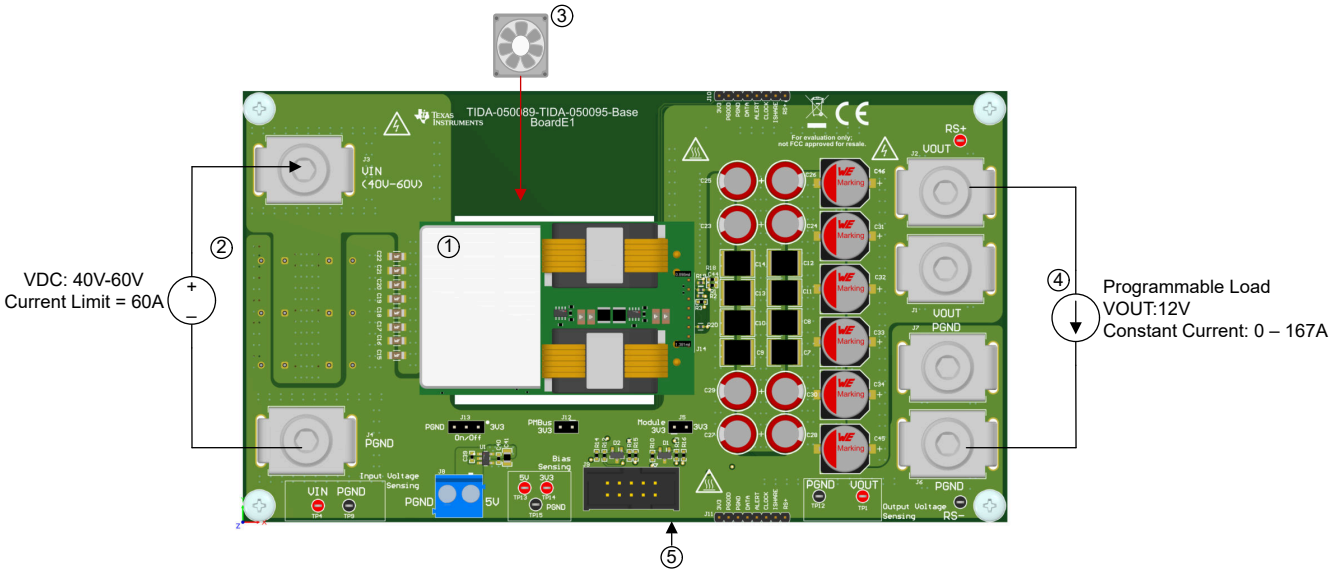

Figure 3-1. Test Setup

3.4 Test Results

The following test results show that for a 12V output, peak efficiency is about 98.15% at 970.4W output power and 48V input voltage. Peak efficiency for 54V input is 97.98% at mid-load and 97.38% at full load. These efficiency measurements include all bias supply requirements but exclude the output pin connector power loss.

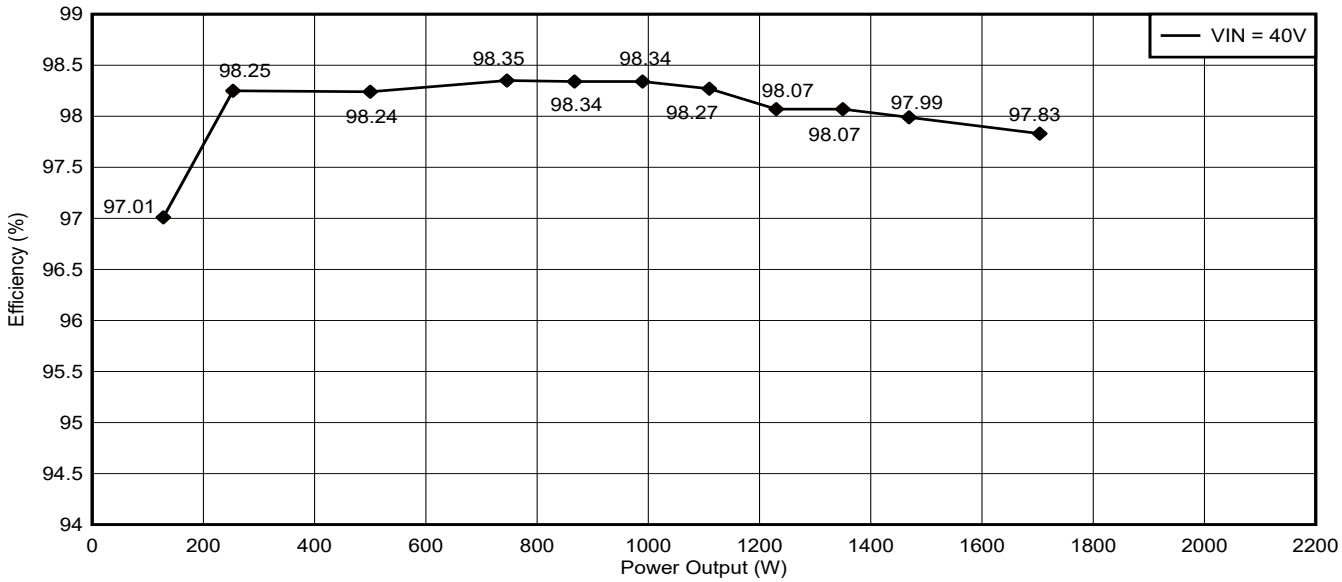

Figure 3-2. Efficiency at 40V VIN

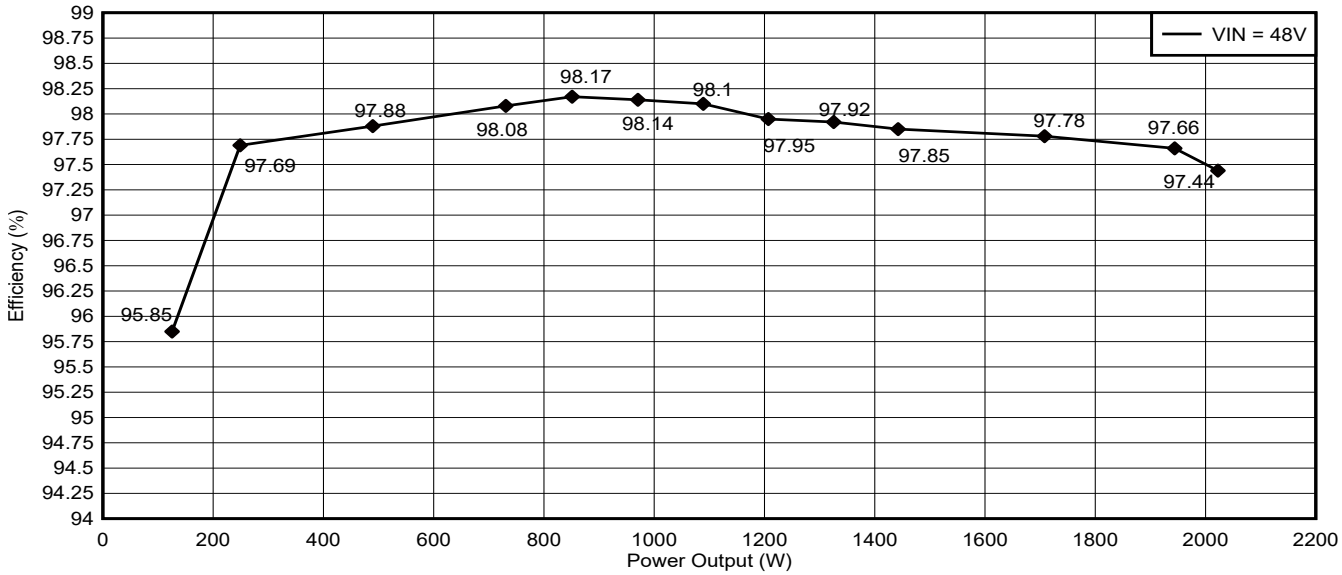

Figure 3-3. Efficiency at 48V VIN

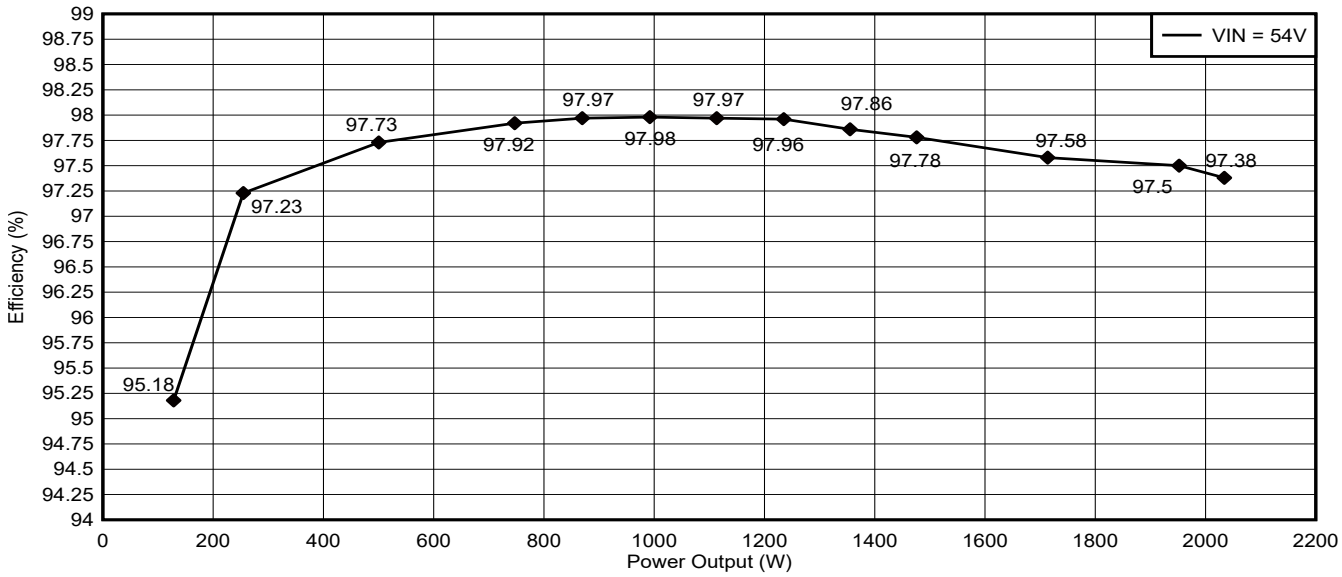

Figure 3-4. Efficiency at 54V VIN

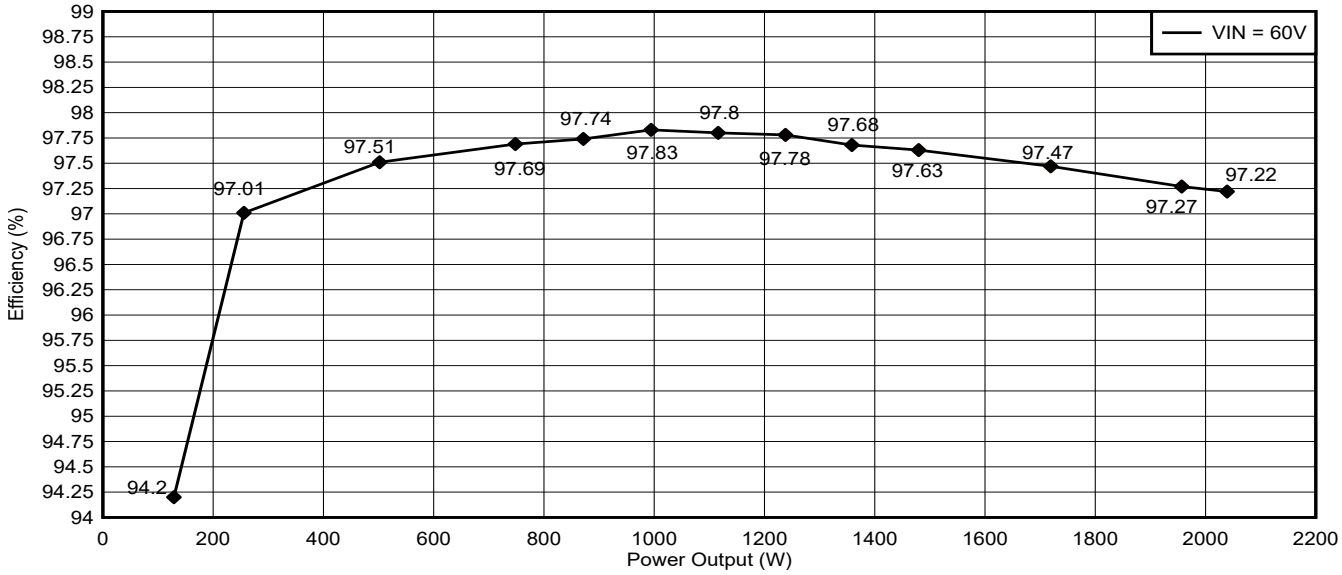

Figure 3-5. Efficiency at 60V VIN

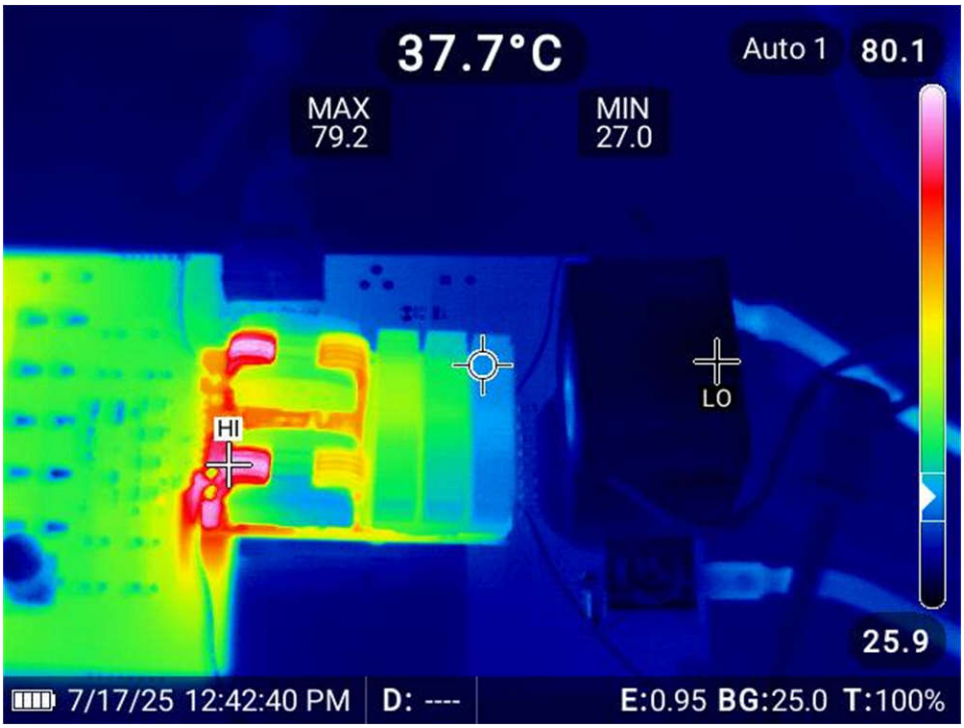

Figure 3-6. Thermal Capture (48V–12V, 2kW, 25°C Ambient, 41.2 Cubic Feet per Minute Airflow)

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050095.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050095.

4.1.3 PCB Layout Recommendations

4.1.3.1 Power Loop Optimization

Make sure the high-frequency current returns to the capacitor through the least inductive path possible. This reduces the peak voltage on the switch node during hard switching transitions. Place multiple capacitors close to the DRN pin of the high-side LMG3100R017 and use vias on the SRC pad of the low-side LMG3100R017 to complete the power loop through the immediate next layer (*Inner Layer 1*, see Figure 4-1). Additionally, add multiple higher value capacitors on the bottom layer to provide sufficient current and meet the transient ripple specifications.

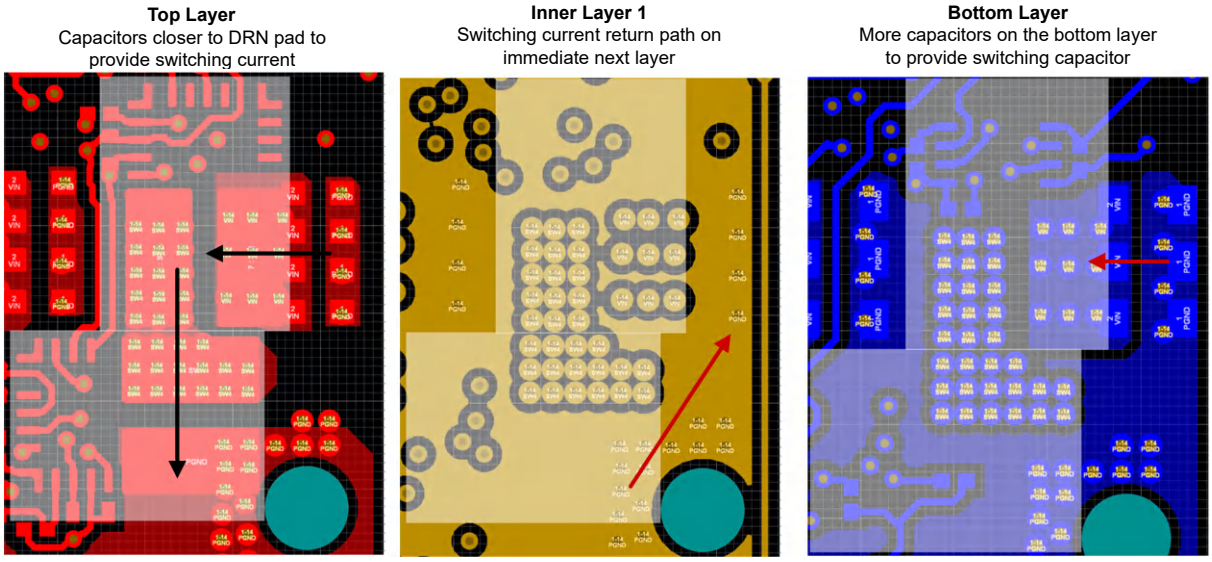

Figure 4-1. Power Loop Path

4.1.3.2 Return Current Through Output Power Ground

When doing the layout, prioritize the VOUT trace, as this trace carries the highest current in the design. Make sure that enough layers are also used for the PGND return. In the current design version, there are four dedicated layers for PGND return. If necessary, to reduce board thickness or minimize PCB losses, a copper bar can be added externally on the bottom side to route the return current from the PGND output pin to the low-side LMG3100R017 PGND.

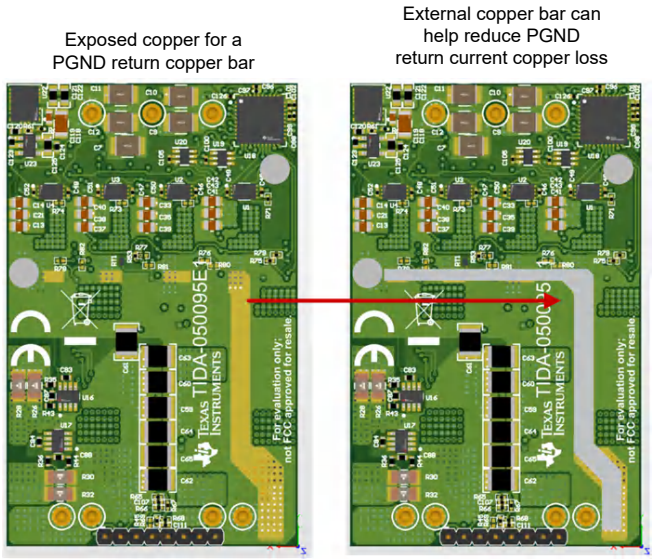

Figure 4-2. Copper Bar Placement

4.2 Tools and Software

Tools

CCSTUDIO Code Composer Studio™ is an integrated development environment (IDE) for TI's microcontrollers and processors. The IDE comprises a suite of tools used to develop and debug embedded applications.

Software

FUSION_DIGITAL_POWER_DESIGNER Fusion Digital Power™ semiconductor devices graphical user interface (GUI) software is used to configure and monitor select Texas Instruments digital power controllers and sequencer/health monitors. The application uses the PMBus protocol to communicate with the device over serial bus by way of a TI USB adapter.

4.3 Documentation Support

1. Texas Instruments, *LMG3100R017 100V, 97A GaN FET With Integrated Driver Datasheet*
2. Texas Instruments, *Benefits of a multiphase buck converter Analog Design Journal*
3. Texas Instruments, *Multiphase Buck Design From Start to Finish Application Report*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

4.5 Trademarks

5 About the Author

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