

TIDA-011001 Quad-Channel 6A, 0-5V Programmable Power Supply Reference Design



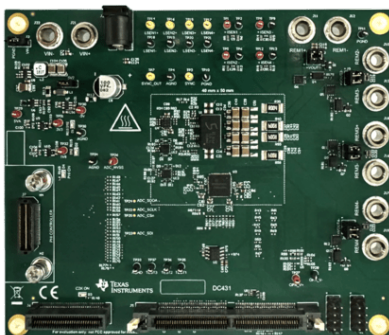
Description

This reference design presents a high-density, four-channel, digitally controlled programmable power supply targeting burn-in and reliability test applications. The design support 12V_{DC} input bus and delivers four independently regulated output channels, each adjustable from 0V to 5V with a maximum continuous output current of 6A per channel.

The control architecture centers on C2000™ real-time microcontroller (MCU), which executes a 2P2Z (two-pole, two-zero) digital compensator. A 16-bit quad-channel DAC dynamically modulates the buck power module output by feedback-pin current injection. While a 24-bit, 16-channel SAR ADC simultaneously captures current and voltage telemetry with integrated low drift PGA, the design can achieve a load regulation error of less than $\pm 0.005\%$ of full scale across the full load range.

Resources

TIDA-011001	Design Folder
TPSM8F7620	Product Folder
ADS9308V8I	Product Folder
DAC80508	Product Folder
TMS320F28P650	Product Folder
REF50 , OPA4990	Product Folder

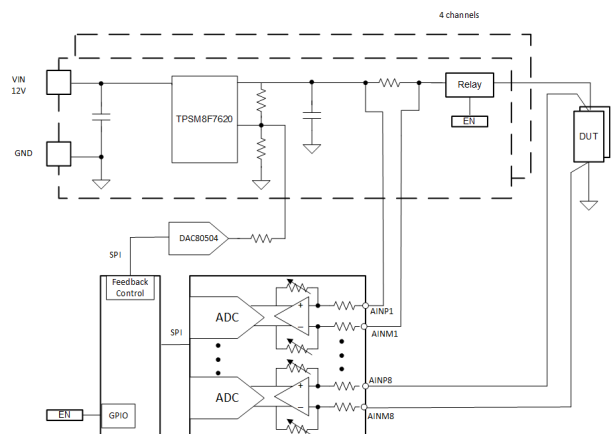


Features

- Four independent output channels programmable from 0V to 5V_{DC}
- Current clamping integrated in the digital control loop; no external analog limiting circuitry required
- High accuracy load regulation:
 - Voltage load regulation: $< \pm 0.25\text{mV}$ ($\pm 0.005\%$ of 5V Full Scale)
 - Current load regulation: $< \pm 0.3\text{mA}$ ($\pm 0.005\%$ of 6A Full Scale)
- 16-bit DAC resolution for sub-millivolt output voltage setpoints
- Simultaneous 24-bit Telemetry with multichannel precision SAR ADC for synchronous current and voltage monitoring at up to 125kSPS per channel.
- Output voltage settling time $< 200\mu\text{s}$ from no-load to full load condition

Applications

- [Programmable DC power supply](#)



1 System Description

Traditionally, burn in is viewed as a reliability screening process to eliminate infant mortality. By subjecting the device under test (DUT) to elevated temperatures and electrical stresses for an extended period, the process forces *infant mortality* failures—defects caused by manufacturing inconsistencies—to occur before the product reaches the customer.

For emerging application domains such as High Bandwidth Memory (HBM) used in AI accelerators and GPUs, and high-performance ASIC, burn-in is no longer just a sorting or screening operation—it is a non-negotiable, specification-mandated process. New packaging process require that devices endure a defined voltage and temperature stress profile for a prescribed minimum duration—often hundreds to thousands of hours—as a condition of product qualification or customer acceptance. The increasing complexity of these application-specific profiles—with multiple supply rails, tight current tolerances, dynamic power sequencing, and per-pin compliance monitoring—imposes requirements on the burn-in power supply that conventional analog designs cannot readily meet.

Modern burn-in systems must supply hundreds to thousands of DUT pins simultaneously with stable, repeatable voltage and current profiles. The power supply must maintain tight regulation despite the wide, dynamic load variation caused by DUT power-state transitions, while simultaneously providing accurate telemetry used to detect aberrant device behavior. As test floor density increases, packing more test points into a smaller footprint becomes equally important, placing a premium on channel density and efficient power conversion.

This reference design addresses these requirements with a multi-channel, digitally closed-loop architecture. The TPSM8F7620 quad-channel buck power module provides a high-density power stage, integrating MOSFETs, gate drivers, and inductors in a single 12.0mm × 7.0mm × 2.4mm BGA package. The TMS320F28P65x C2000 MCU closes the regulation loop in software, providing the flexibility to implement per-channel compensation tuning, programmable current clamping, and custom power sequencing—capabilities that would require complex discrete analog circuitry in a conventional design. The ADS9308V8I 24-bit ADC provides high-accuracy simultaneous telemetry across all channels, and the DAC80504 provides the high-resolution voltage actuation needed to achieve sub-millivolt setpoint accuracy.

1.1 Key System Specifications

Table 1-1. Specifications

Parameter	Specification
Input voltage	12V-15V
Output voltage	100mV-5V(FPWM)
DC current per channel	6A(max)
Current output accuracy	±0.005%
Voltage output accuracy	±0.005%
Voltage settling time	<150μs from no load to full load

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the block diagram of the TIDA-011001.

The 12V input bus feeds all four channels of the TPSM8F7620 buck power module. Each channel independently steps down the 12V rail to a regulated output voltage set by the position of its FB pin. The C2000 MCU issues a 16-bit digital code to the DAC80504 over a high-speed SPI bus; the DAC output drives a resistor network at the FB pin of each buck channel, injecting a bias current that shifts the regulated output voltage. On the feedback path, the ADS9308V8I samples each channel's load voltage and high-side shunt current simultaneously, returning the measurements to the C2000 MCU over a second SPI bus. The MCU closes the loop by computing a 2P2Z correction and writing an updated DAC code. The MCU closes the loop by computing a 2P2Z correction and writing an updated DAC code.

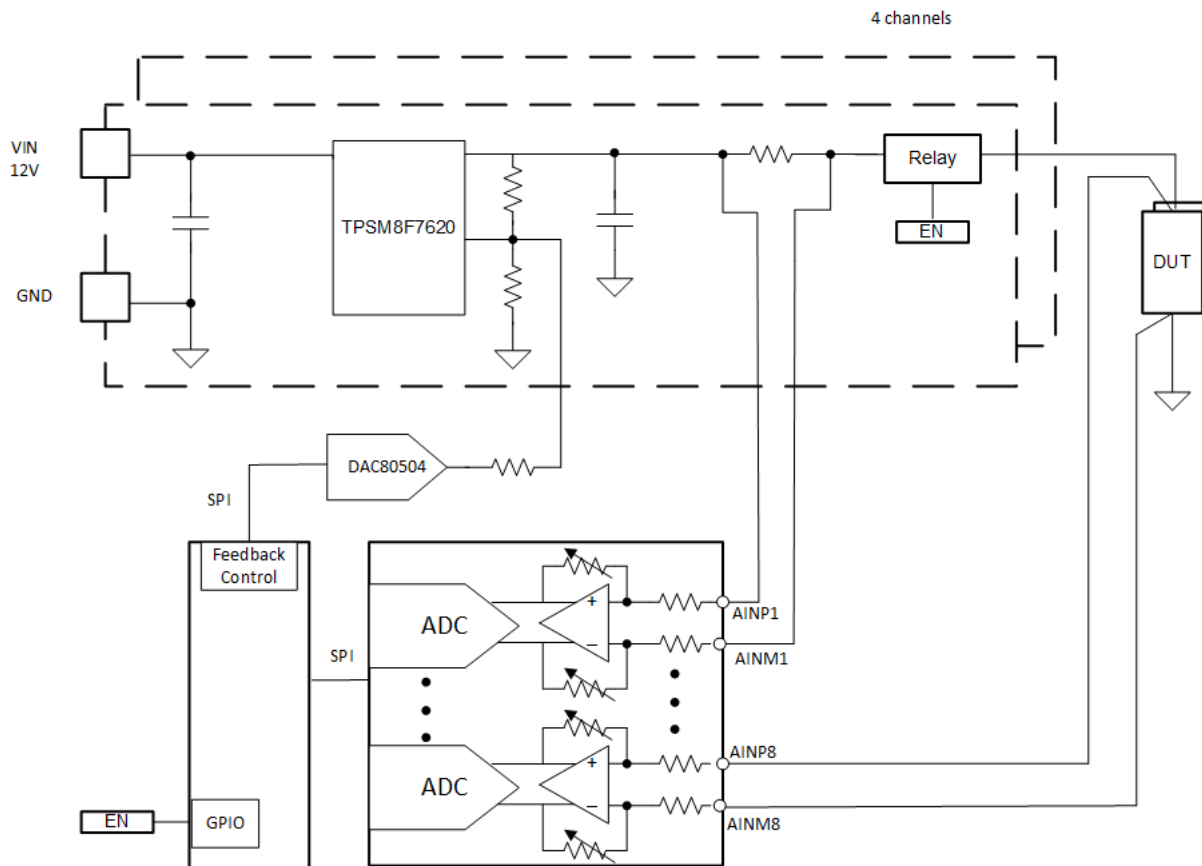


Figure 2-1. System Block Diagram

2.2 Design Considerations

2.2.1 Step-Down Converter Subsystem

The TPSM8F7620 is configured as four independent synchronous buck regulators sharing a common 12V input rail. Each channel operates in fixed-frequency peak current mode control, using an internal error amplifier to regulate the external FB node to a 0.6V reference. Because the MOSFET drivers, bootstrap circuitry, and a shielded inductor are integrated inside the module package, the external switching loop area is minimized, reducing EMI and simplifying PCB layout. Switching frequency is configurable from 400kHz to 2.2MHz; Various switching frequency can be adjusted to balance switching loss and output ripple for the 12V to 0.1V–5V conversion ratio.

2.2.2 Digital-to-Analog Control Set Path

To dynamically program individual channel limits, the C2000 DSP transmits digital codes across a high-speed SPI bus to the DAC80504. This design uses 2P2Z digital compensation filter inside C2000 digital control loop library. For more information please refer to [C2000WARE-DIGITALPOWER-SDK](#).

The DAC80504 is used to provide an exceptionally clean 0V to 5V continuous analog reference voltage. As V_{out} approaches 0V, V_{DAC} must approach the maximum of 5V. To maximize the control loop bandwidth, fast settling time is needed for both ADC and DAC. The DAC8050x settling time to 1 LSB (16-bit, 5V span $\approx 76\mu V$) is typically $< 10\mu s$.

2.2.3 High-Precision Measurement Front-End (Feedback Path)

Tracking load conditions to maintain a 0.005% regulation target requires telemetry that bypasses thermal drifting. The system routes point-of-load voltage sensing and high-side current shunt drops directly into the ADS9308V8I 24-Bit ADC.

- **Voltage Sensing:** Low-drift differential difference amplifiers attenuate and buffer the rail voltages directly from the DUT socket pins.
- **Current Sensing:** Integrated zero-drift programmable gain amplifiers (PGAs) amplify forward voltage drops across precision shunts without introducing offset errors.

Because the ADC samples all 16 channels simultaneously at 125kSPS, the C2000 MCU receives real-time phase-aligned measurements. The MCU processes these data vectors through a digital proportional-integral (PI) algorithm, calculating adjustment commands sent directly to the power conversion components to instantly neutralize any load or line fluctuations, maintaining rapid transition from constant voltage (CV) to constant current (CC) forward current limiting modes during a fault event.

2.3 Highlighted Products

2.3.1 TPSM8F7x20

The TPSM8F7x20 is a power-dense quad-channel buck power module designed to provide efficient and reliable power conversion for a wide output voltage range up to 11V. The module integrates MOSFETs, inductor, and select capacitors to reduce board space and layout complexity. The module can be configured into both multiphase and multi-output rails by supporting 2, 3, and 4-phase stackability with interleaved phases. It is in small form factor 12.0mm $\times$ 7.0mm $\times$ 2.4mm, overmolded BGA power module. This module employs current mode control with internal and external compensation.

Features include:

- Analog power supply of 5V and 1.8V and digital I/O supply of 1.8V-3.3V
- Continuously adjustable switching frequency from 400kHz to 2.2MHz
- Output discharge ability
- Synchronizable to an external clock

2.3.2 ADS9308V8I

The ADS9308V8I is a 16-channel, 24-bit SAR ADC with integrated analog front end for simultaneous current and voltage sensing. The device integrates eight zero-drift programmable gain amplifiers for current sensing, and eight low-drift programmable gain difference amplifiers for voltage sensing. This device operates in positive supply rails of 1.8V and 5V. ADS9308V8I can achieve up to 125kSPS sampling rate per channel and SNR of 95.5dB for $\pm 5V$ range.

Features include:

- Programmable current sense with input range of $\pm 25mV$, $\pm 50mV$, $\pm 100mV$, $\pm 150mV$, $\pm 200mV$
- Programmable voltage sense with input range from $\pm 50V$, $\pm 25V$, $\pm 12.5V$, $\pm 10V$, $\pm 6.25V$, $\pm 5V$, $\pm 2.5V$
- Analog power supply of 5V and 1.8V and digital I/O supply of 1.8V-3.3V
- 8.0mm $\times$ 8.0mm VQFN package

2.3.3 TMDSCNCD28P65X

TMDSCNCD28P65X is a low-cost evaluation and development board for TI C2000™ MCU series of F28P65x devices. TMDSCNCD28P65X comes with a HSEC180 (180-pin High speed edge connector) and, as a controlCARD, is ideal for initial evaluation and prototyping. For evaluation of TMDSCNCD28P65X, a 180-pin docking station TMDSHSECDOCK is required and can be purchased separately or as a bundled kit. In this design the control card is used for digital control loop settings.

The features of MCU include:

- Contains up to three CPUs: two 32-bit C28x DSP CPUs and one CLA CPU, all running at 200MHz
- 1.28MB of CPU-mappable flash (ECC-protected) with 5 flash banks
- 248KB of RAM (enhanced parity-protected)
- 36 pulse width modulator (PWM) channels, all with 150ps high-resolution capability (HRPWM)
- Various digital power supply library enable simpler software implementation

2.3.4 DAC80504

The DAC80504 is a 16bit, 4 channel, featuring high linearity of ± 1 LSB INL and ultra-low TUE of $\pm 0.1\%$ FSR.

The device integrates low drift, 2.5V internal reference, eliminating the need for an external precision reference in most applications. A user-selectable gain configuration provides full-scale output voltages of 1.25V (gain = $\frac{1}{2}$), 2.5V (gain = 1), or 5V (gain = 2). These devices operate from a single 2.7V to 5.5V supply, and is available in small 3mm $\times$ 3mm QFN package.

2.3.5 REF50

The REF50 provides low-noise, low-drift, and very high precision voltage references to both ADC and DAC to maintain the same drift. The device has a low noise of 3 μ VPP/V and long term drift of 50ppm after the first 1000 hours. REF50 family is available in enhanced grade (REF50xxEI), high grade (REF50xxI), and standard grade (REF50xxAI).

Features below:

- Temperature drift (maximum)
 - Enhanced-grade (new): 2.5ppm/°C
 - High-grade: 3ppm/°C
 - Standard-grade: 8ppm/°C
- High accuracy (maximum):
 - Enhanced-grade: 0.025%
 - High-grade: 0.05%
 - Standard-grade: 0.1%

2.3.6 OPAx990

The OPAx990 high voltage (40V) general purpose operational amplifiers, is used for general purpose clamp for buck converters. These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset ($\pm 300\mu$ V, typ), and low offset drift ($\pm 0.6\mu$ V/°C, typ)

The device features:

- Wide bandwidth: 1.1MHz GBW
- MUX-friendly/comparator inputs
- High common-mode rejection: 115dB
- Low bias current: ± 10 pA
- High slew rate: 4.5V/ μ s

3 System Design Theory

3.1 Converter Step Down Range

The TPSM8F7620 error amplifier holds the FB pin at exactly 0.6V by adjusting duty cycle. When the DAC drives V_{DAC} significantly above 0.6V, the device injects additional current into the FB node. To maintain the 0.6V equilibrium, the error amplifier reduces duty cycle until V_{OUT} drops. Mathematically, V_{OUT} can approach 0V by pushing V_{DAC} toward the full-scale value.

The TPSM8F7620 is configured in forced PWM (FPWM) mode, which is what enables low output voltages. In normal DCM the converter stops switching when load current is very light and V_{OUT} floats up. FPWM forces continuous switching and allows reverse inductor current (the low-side FET conducts after the inductor current crosses zero, actively pulling current from the output back toward ground). This is what allows stable regulation down toward mV.

$$\frac{V_{OUT} - 0.6}{R_{FBT}} + \frac{V_{DAC} - 0.6}{R_{DAC}} = \frac{0.6}{R_{FBB}} \quad (1)$$

3.2 Fault Clamping Protection

A low leakage operational amplifier configured as an active buffer, combined with a low-leakage Schottky diode, creates a precision 0.4V clamp on the FB node.

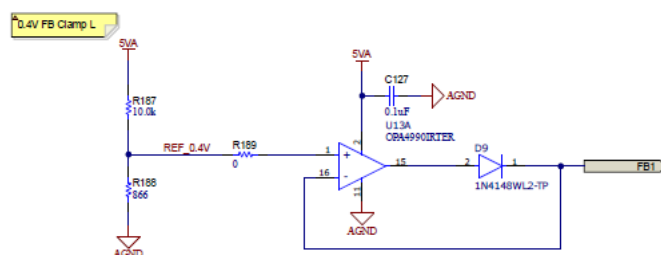


Figure 3-1. Fault Clamping Protection

Under normal operation the FB node rests at 0.6V and the clamp diode is reverse-biased and inactive. If a software fault or DAC code error drives the FB node below 0.4V—which causes the power module to demand maximum duty cycle and push V_{OUT} to an uncontrolled maximum—the clamp immediately locks the FB node at 0.4V, bounding the output overvoltage excursion regardless of software state.

3.3 Current Clamping Behavior

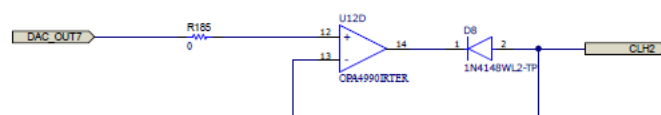


Figure 3-2. Buck Module Analog/Digital Loop Manipulation

This circuit bridged the control loop priority between buck module analog compensator and digital control loop signal, to achieve desired clamping behavior. The CLH node connects to hardware compensator of the TPSM8F7620.

The COMP pin of the TPSM8F7620 is the internal node of the peak-current-mode error amplifier, it can interact with special feature of the device like OVP limit, control loop priorities and so on. This design makes the COMP pin accessible externally (CLH node) and connects it through a unidirectional fast diode to the DAC's current-clamp output. Under normal CV (constant-voltage) operation, the COMP node voltage is lower than the DAC clamp level, the diode remains reverse-biased, and the digital compensation loop operates without interference.

During a short-circuit or sudden current surge, the COMP voltage rises rapidly as the power module attempts to increase duty cycle to sustain the output voltage. When COMP exceeds the DAC clamp threshold, the diode conducts, injecting current into the COMP node through a 1200pF capacitor and 10.5kΩ resistor network. This RC network limits the slew rate of the COMP ramp, immediately arresting the duty-cycle increase and capping the inductor peak current within a single switching cycle—well before the digital control loop can respond. Once the hardware suppresses the fault to within the controllable linear range, the digital PI loop takes over and transitions the channel smoothly from CV to CC (constant-current) mode, maintaining the programmed current clamp limit.

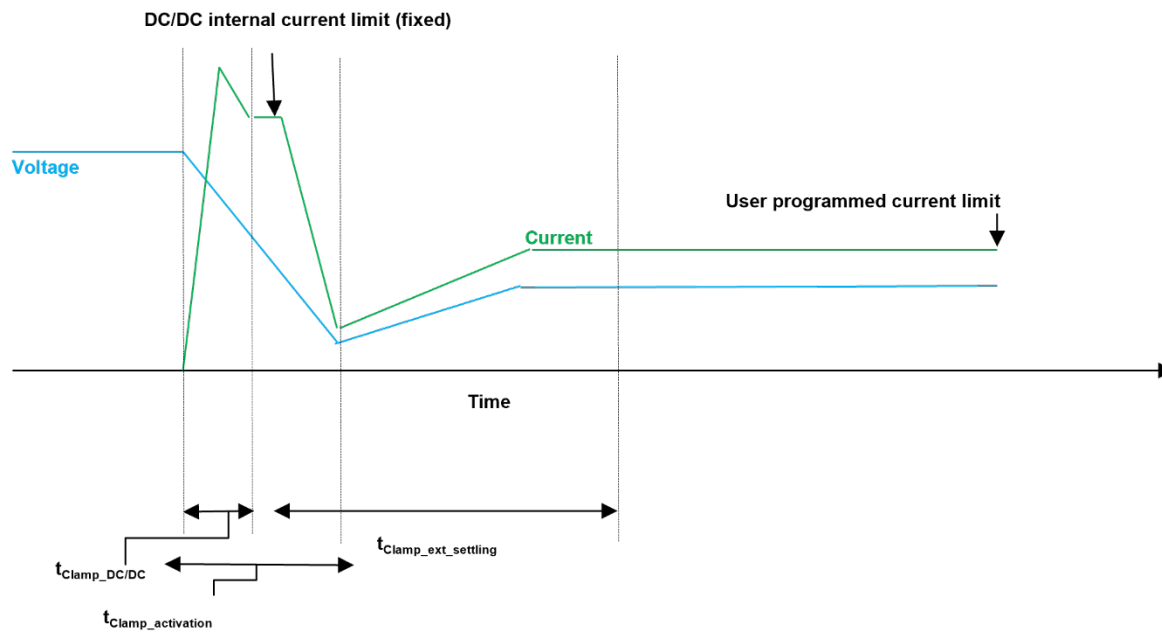


Figure 3-3. Current Clamping Behavior

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

This reference design can be setup using the following equipment:

- 12V power supply with capability of 120W output
- Oscilloscope with current probe and voltage probe
- 6.5 digital multimeter for voltage and current calibration
- Computer for real time system control and measurements

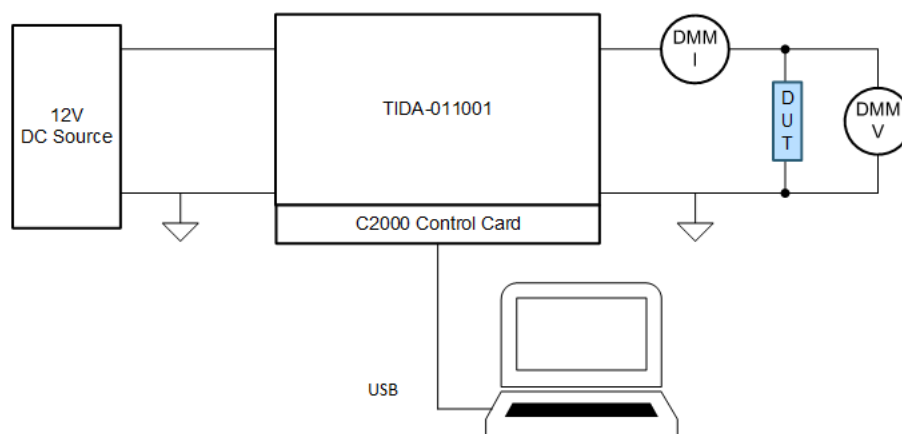


Figure 4-1. Hardware Requirements

4.2 Software

This design uses graphical user interface (GUI) to simplify the settings of current, voltage, compensation tuning and sensing.

1. To set up the test environment, download and install [UNIFLASH](#) software.
2. Connect the TMDSCNCD28P65X controlCARD to the host PC via USB. In UniFlash, select the F28P65x device and click *Connect*.
3. Select the .OUT file provided for the design, check the option *Run Target After Program Load Flash Operation*, and load the software image.
4. Once the image is loaded, P3S.exe can be executed to run the GUI.
5. Config serial port to UART communication by clicking File - Serial Port, select the COM Port with UART on the computer and click connect.

When the connection is successful, the lower right corner shows a green circle.

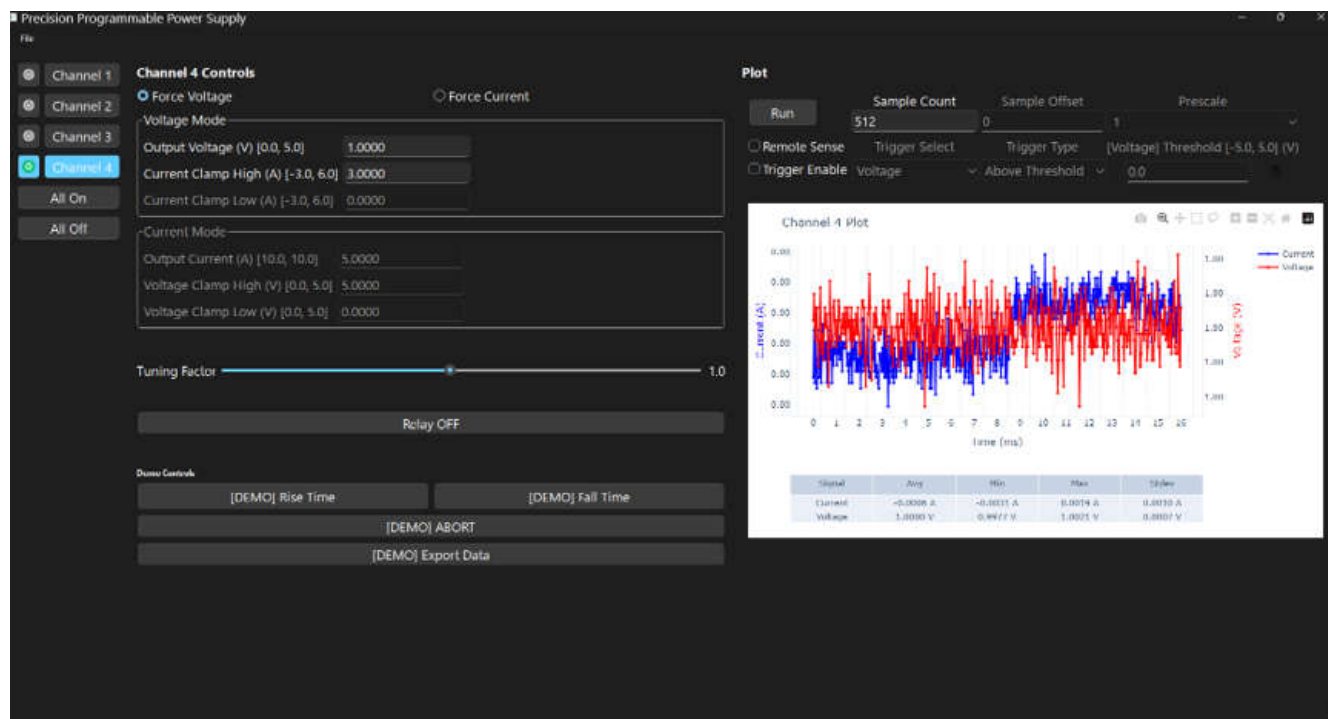


Figure 4-2. GUI for Evaluation

4.3 Test Setup

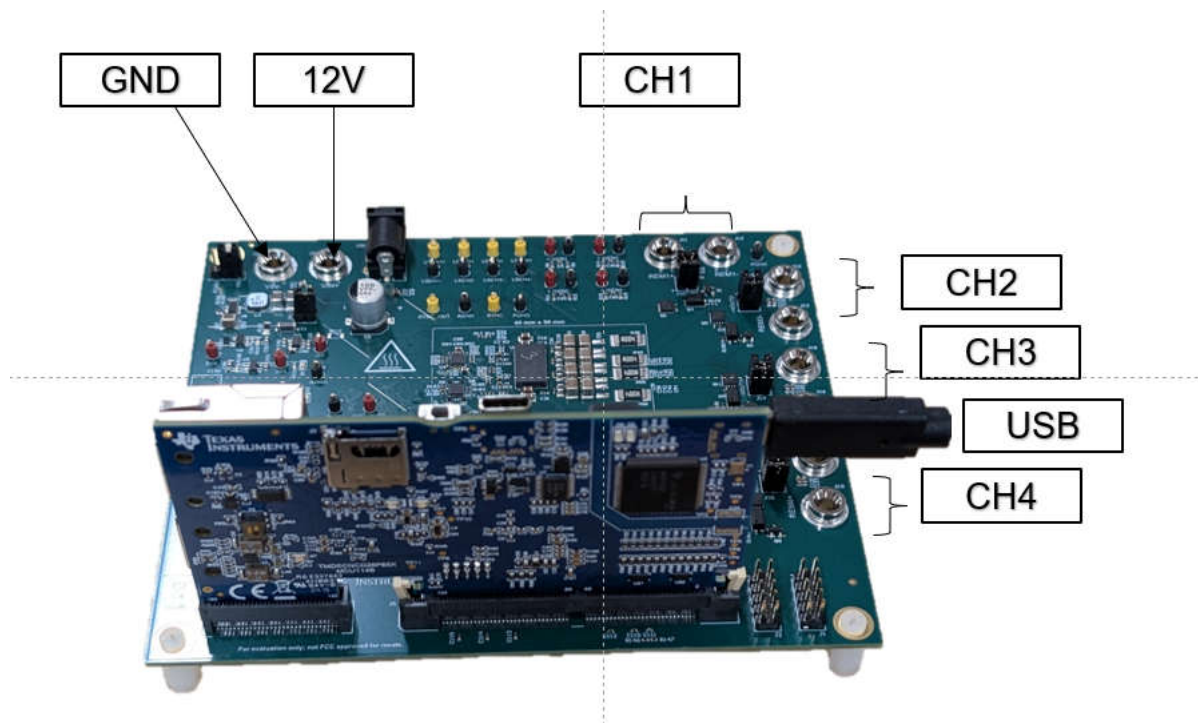


Figure 4-3. Board Setup for Testing

Figure 4-3 shows the reference design setup. This design uses the TMDSCNCD28P65X control card to configure the digital control loop. Connect positive terminal of 12V_{DC} power supply to J21 and negative terminal to J22 to enable the board. To test voltage accuracy, probe digital multimeter to J8, J9, J14, J15 for channel 1-4

output. To test current accuracy, probe digital multimeter across ISEN1-ISNS4 located on top of the board, and calculated the current value by using [Equation 2](#).

$$I = \frac{V}{R_{Shunt}} \quad (2)$$

4.4 Test Results

4.4.1 Voltage Linearity test

The voltage linearity test is performed under the open load condition.

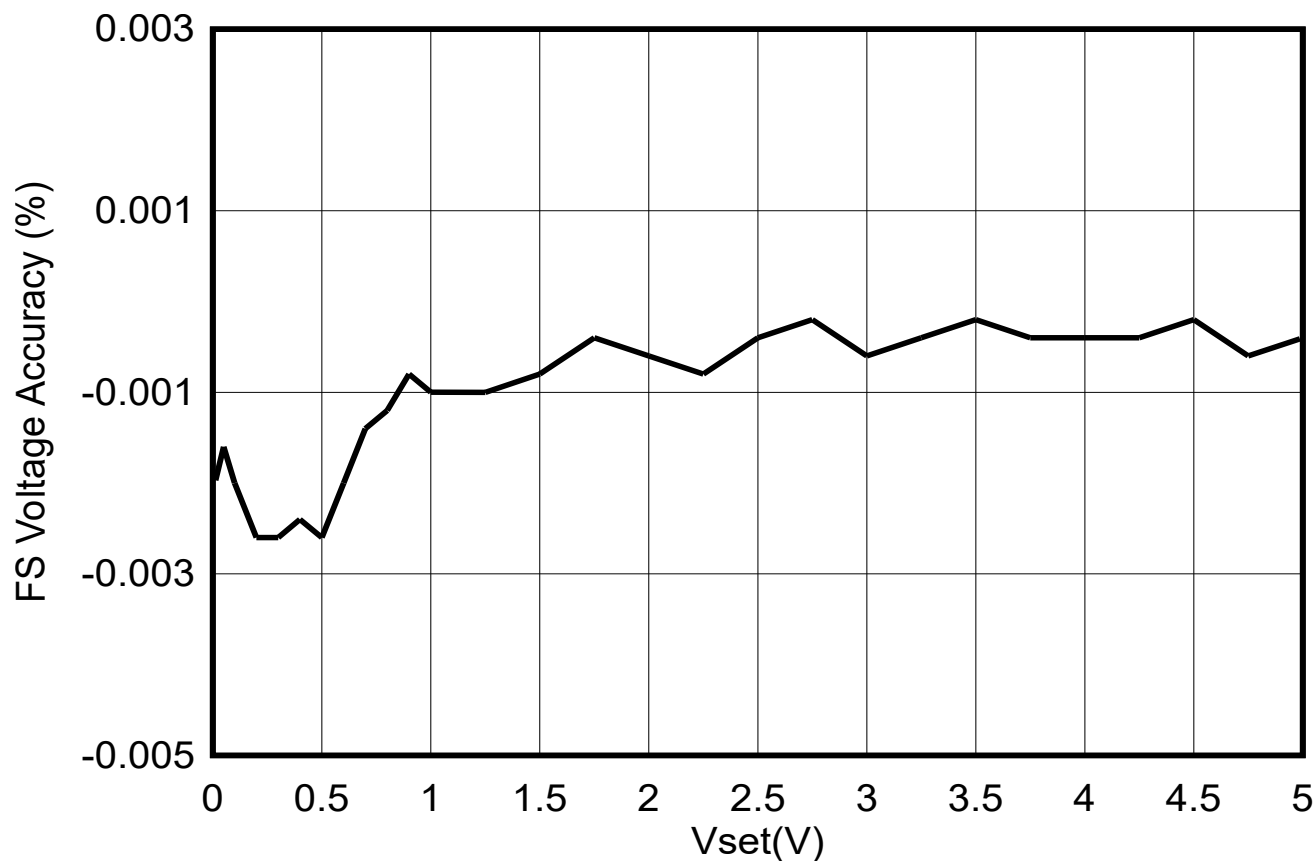


Figure 4-4. Voltage Linearity Test

4.4.2 Voltage Regulation Test

Output voltage tracks the DAC setpoint linearly from 0V to 5V with a worst-case deviation of < 0.2mV across the full range as seen in [Table 4-1](#).

Table 4-1. Voltage Load Regulation

Vset(V)	0.5	1	2	4
I_load (A)	V _{Actual} (V)			
0	0.500034	1.000000	1.9999	3.99982
1	0.500004	1.000022	1.99991	3.99988
2	0.500027	1.000048	1.99992	3.99982
3	0.500039	1.000019	1.99994	3.99988
4	0.500066	1.000009	1.99992	3.99987
5		1.000013	1.99993	3.99985
6		1.000036	1.99996	3.99983
Error(mV)	0.066	0.13	0.1	0.18

Table 4-1. Voltage Load Regulation (continued)

Vset(V)	0.5	1	2	4
I _{load} (A)	V _{Actual} (V)			
Error (%FS)	0.00132	0.0026	0.002	0.0036

4.4.3 Current Linearity Test

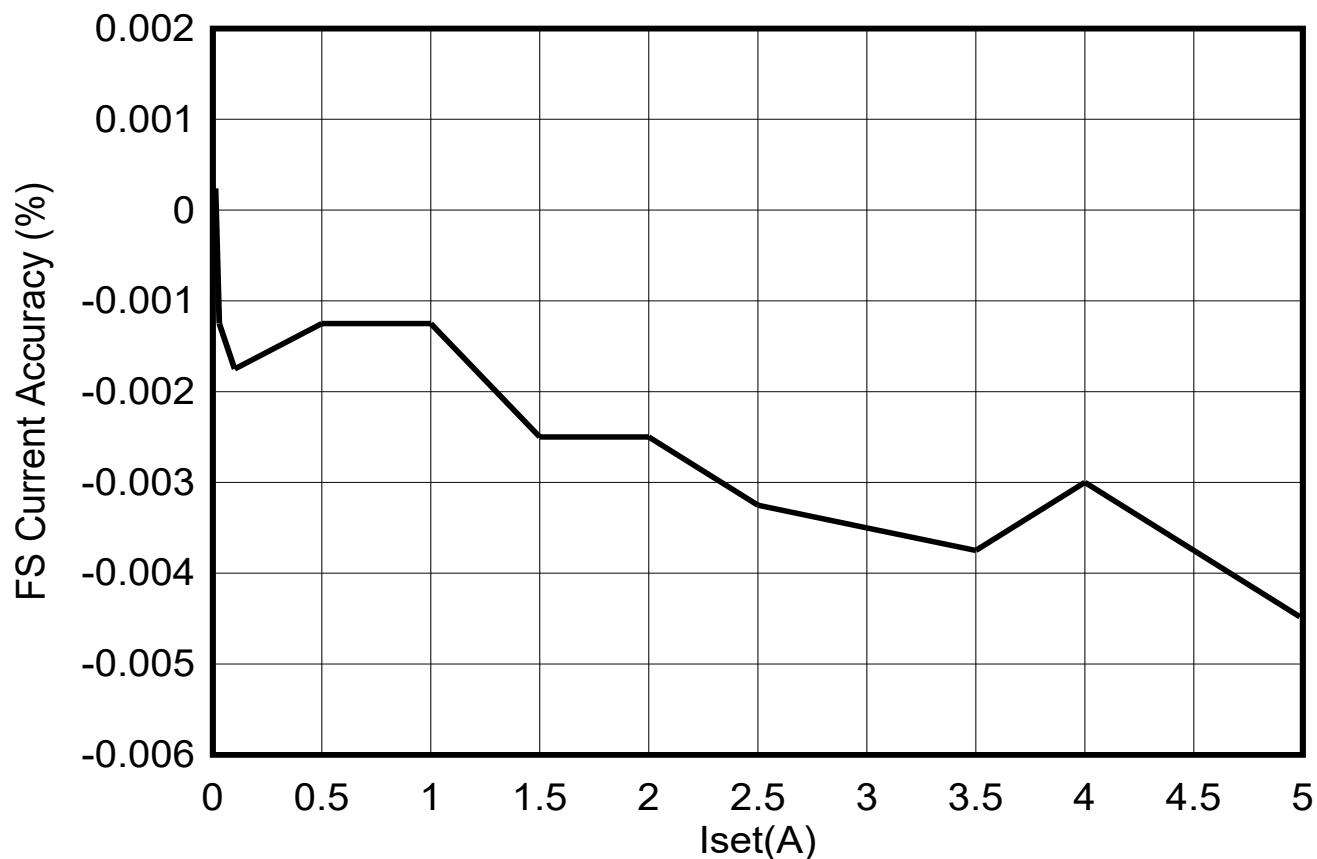


Figure 4-5. Current Linearity Test

4.4.4 Output Voltage Ripple

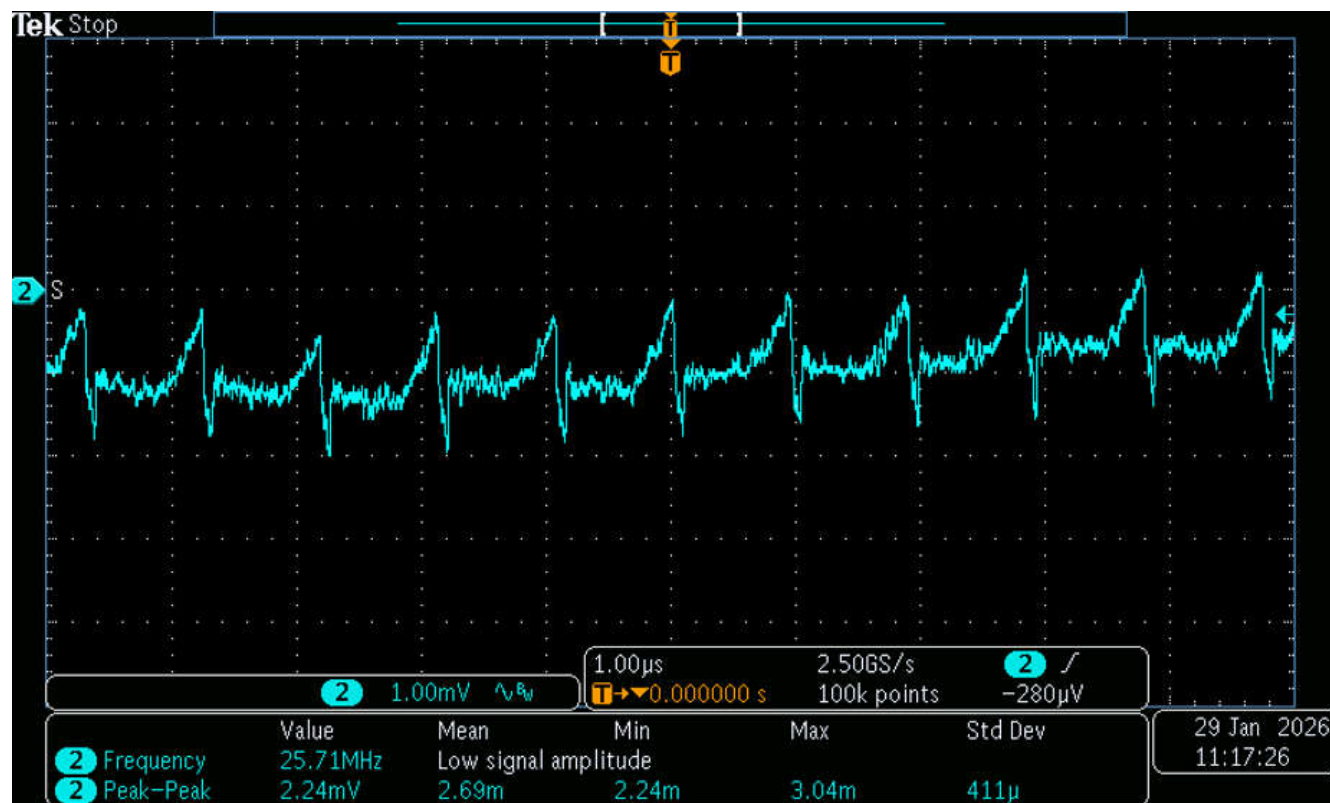


Figure 4-6. Output Voltage Ripple at 1V With No Load

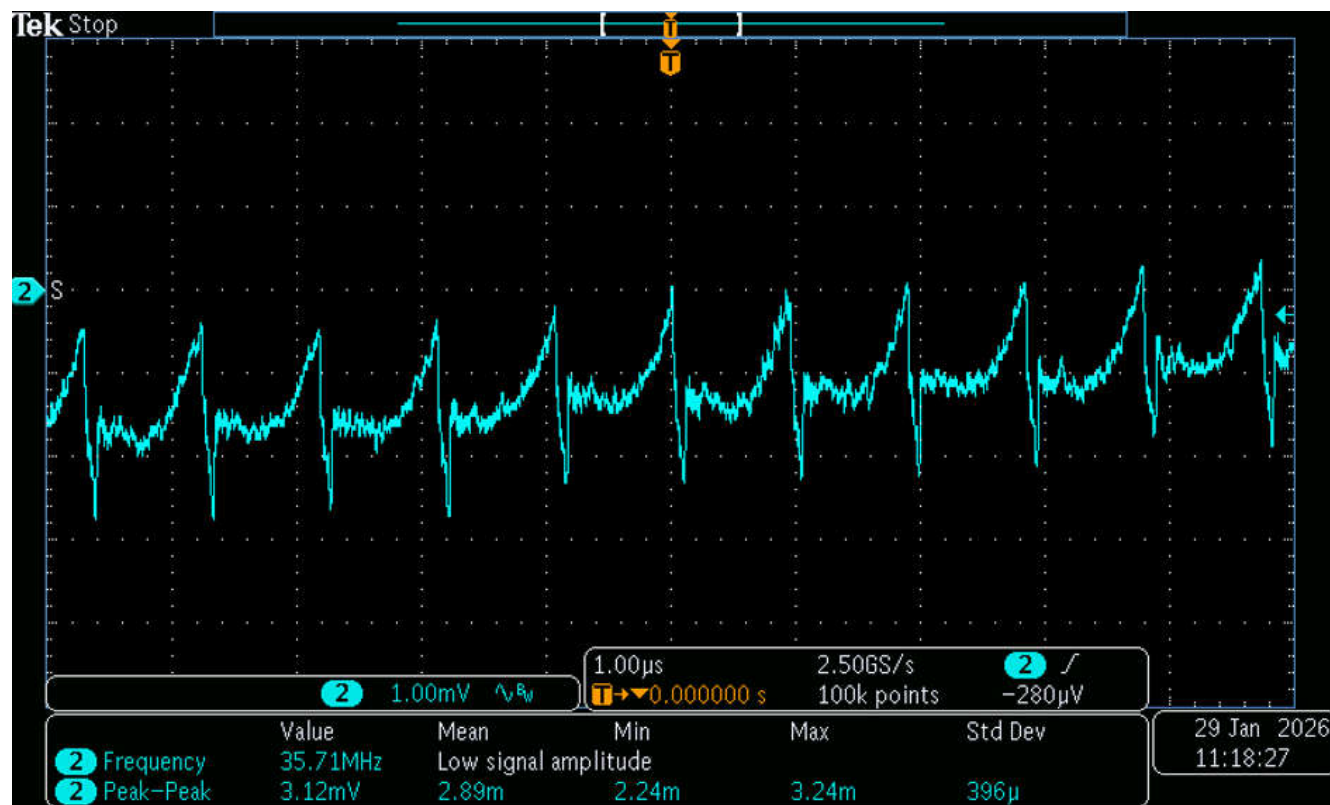


Figure 4-7. Output Voltage Ripple at 1V With Full Load

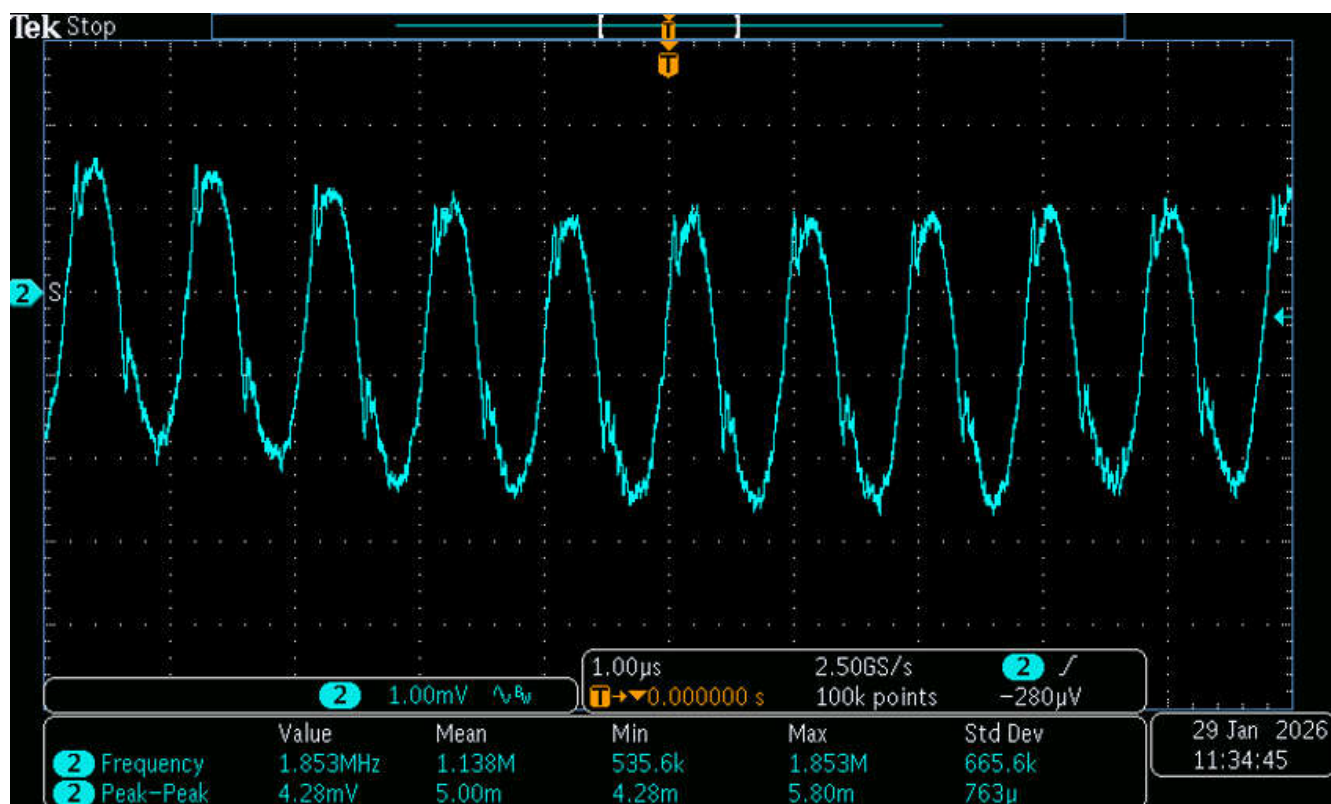


Figure 4-8. Output Voltage Ripple at 5V With No Load

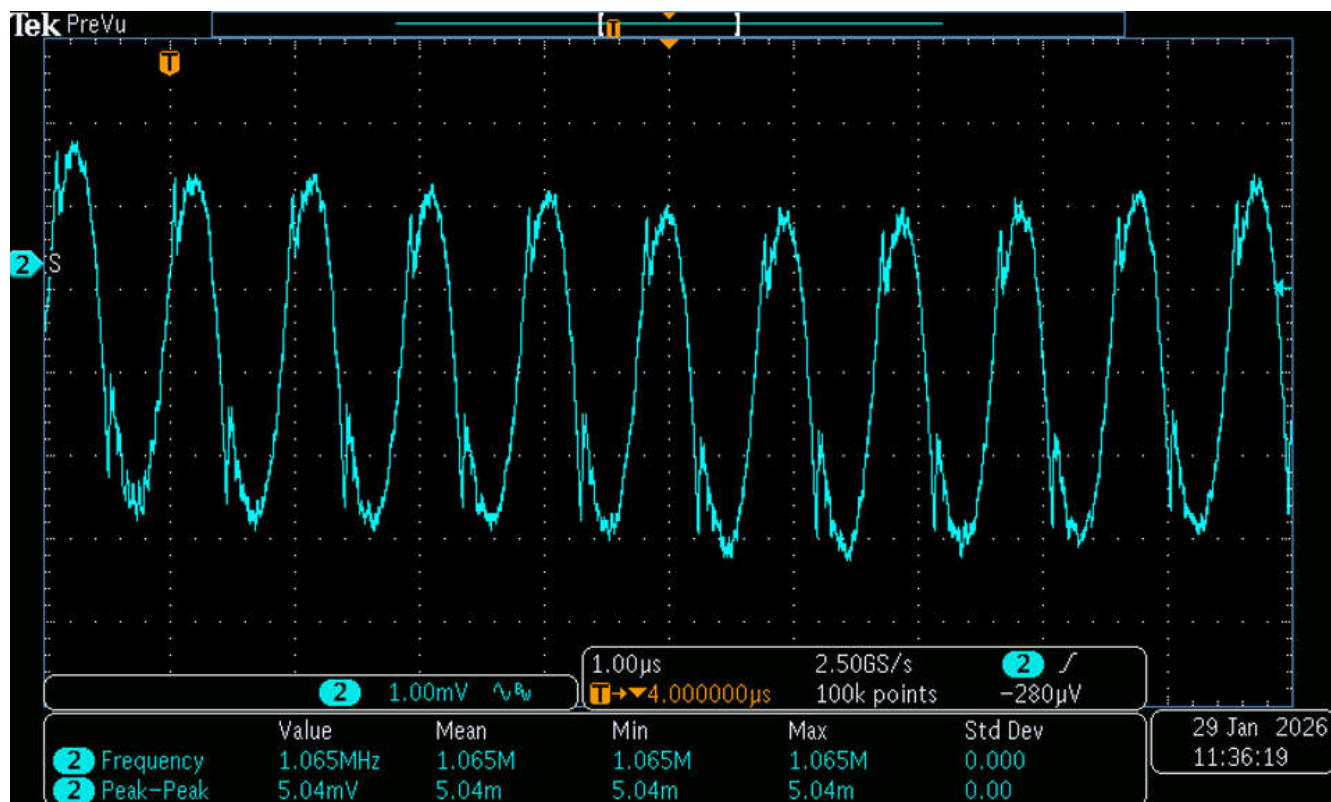


Figure 4-9. Output Voltage Ripple at 5V With Full Load

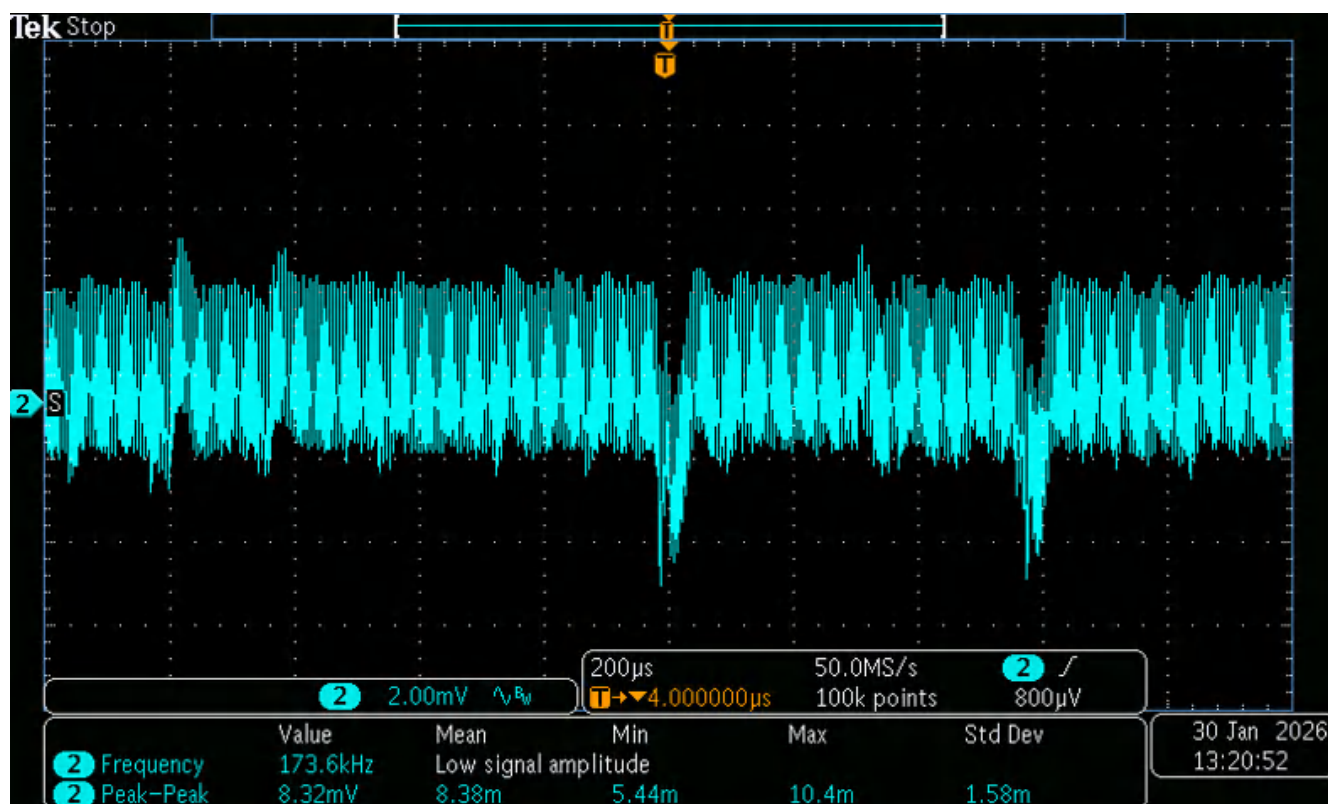


Figure 4-10. Output Voltage at 100mV

4.4.5 Full Load Transient Response

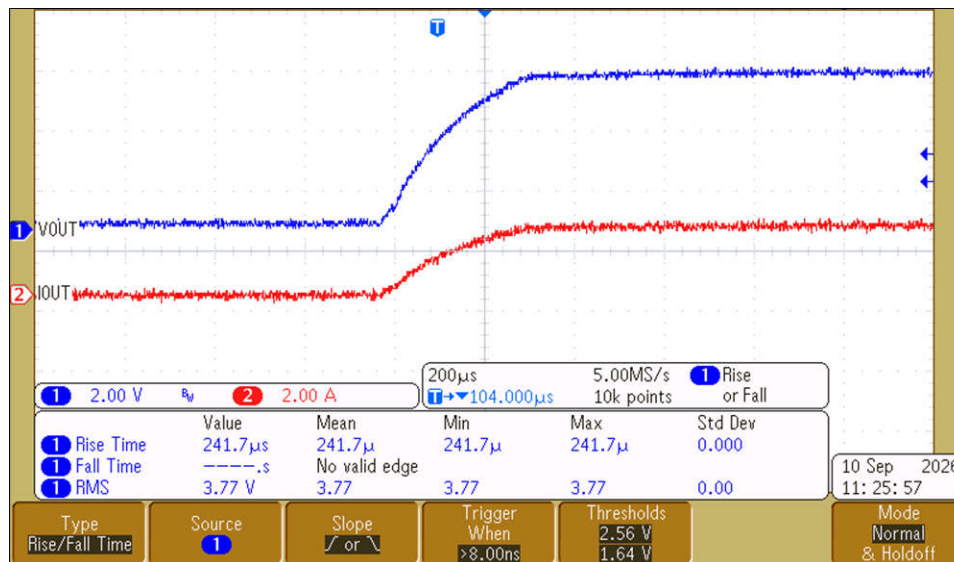


Figure 4-11. Transient Response From 0V to 5V Condition, at 2Ω Load

4.4.6 Sudden Load Switch In with Current Clamping Response

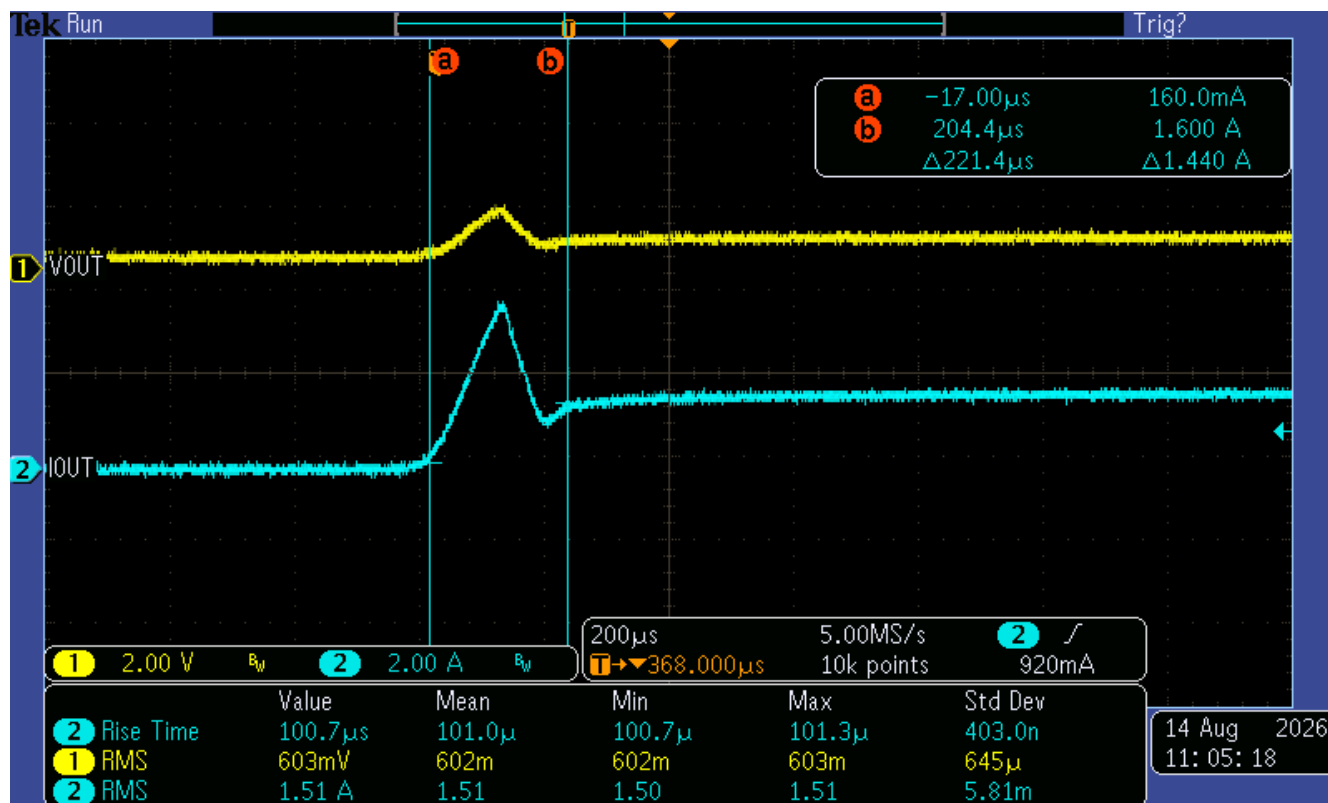


Figure 4-12. Short Circuit With CC Current Clamp at 2A With 200m Ω Load

4.4.7 Full Load Voltage Settling Time

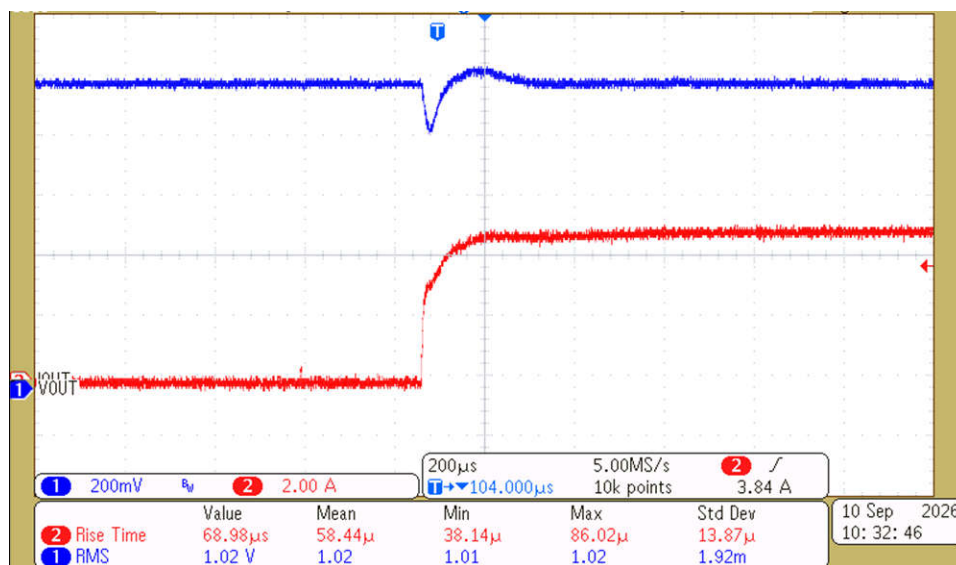


Figure 4-13. Load Switching From Open Load to Full load, With 100m Ω Load

5 Design and Documentation Support

5.1 Tools and Software

5.1.1 Tools

- [TMS320F28P65X controlCARD evaluation module](#)

5.1.2 Software

- [CCSTUDIO](#) integrated development environment (IDE)
- [UNIFLASH](#) programming tool

5.2 Documentation Support

1. Texas Instruments, [ADS9308V8I 24 -Bit, 16 -Channel, Simultaneous-Sampling, Precision ADC for Voltage and Current Sensing datasheet](#)
2. Texas Instruments, [TMS320F28P65x Real-Time Microcontrollers datasheet](#)
3. Texas Instruments, [TPSM8F7x20 4V to 17V, 4/6A, Quad Step-Down Power Module datasheet](#)

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need. Linked content is provided AS IS by the respective contributors.

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6 About the Author

ETHAN YU is a systems engineer at Texas Instruments, where he is responsible for developing reference designs for test and measurement applications. Ethan earned his bachelor degree in electrical engineering from Texas A&M University.

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