Design Guide: TIDA-011063

150A FPGA Core Rail Reference Design with Multi-Phase Power Module

Description

This 150A multi-phase power module reference design provides high-density power for field-programmable gate array (FPGA) core rails. This reference design addresses escalating power demands by delivering efficient, high-current regulation to support next-generation high-performance FPGA architectures.

Resources

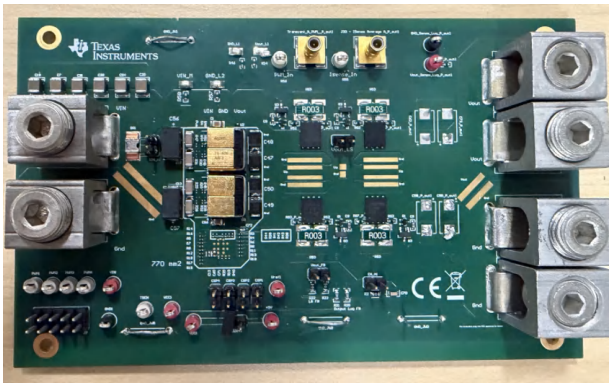
TIDA-011063	Design Folder
CSDM65295	Product Folder
TPS53689T	Product Folder

Features

- Utilizes a four-phase configuration to support 150A+ core rail current
- Achieved <10mV output voltage ripple and maintained voltage deviations within <3% during transient events
- Features an on-board transient generator capable of delivering 100A/µs slew rates
- Engineered for high efficiency and high-power density

Applications

- Communications payload
- Radar imaging payload
- Optical imaging payload



Top of Board

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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage	4.5V to 16V
Output voltage	0.5V to 5.5V
Maximum output current	360A peak, 150A continuous
Switching frequency	500khz to 1.2Mhz

1.2 Considerations

- Separate 12V, 5V and 3.3V bias are needed to power the module and controller for operation
- Transient circuit requires 5V bias and external PWM control signal
- Data was collected using 12V input, 0.8V output, and 800kHz frequency unless otherwise specified
- Voltage and current measurements were taken with a high-bandwidth differential probe

1.3 Dimensions

Board size: 3.5in × 5.5in, tallest component 5mm (power module).

1.4 Test Setup

The test setup is shown in Figure 1-1.

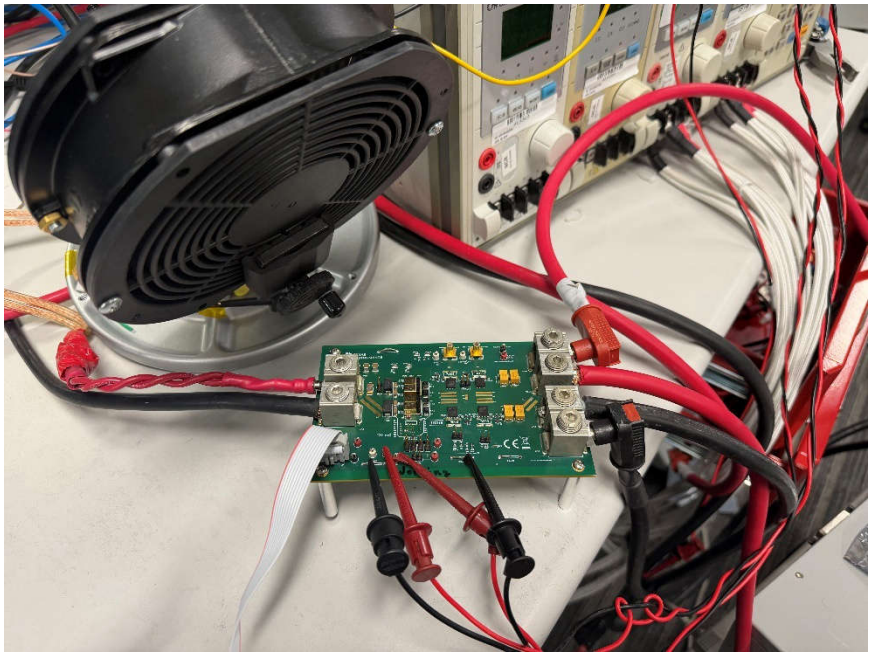


Figure 1-1. Test Setup

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2 Testing and Results

2.1 Efficiency Graphs

Efficiency and power loss are shown in Figure 2-1 and Figure 2-2.

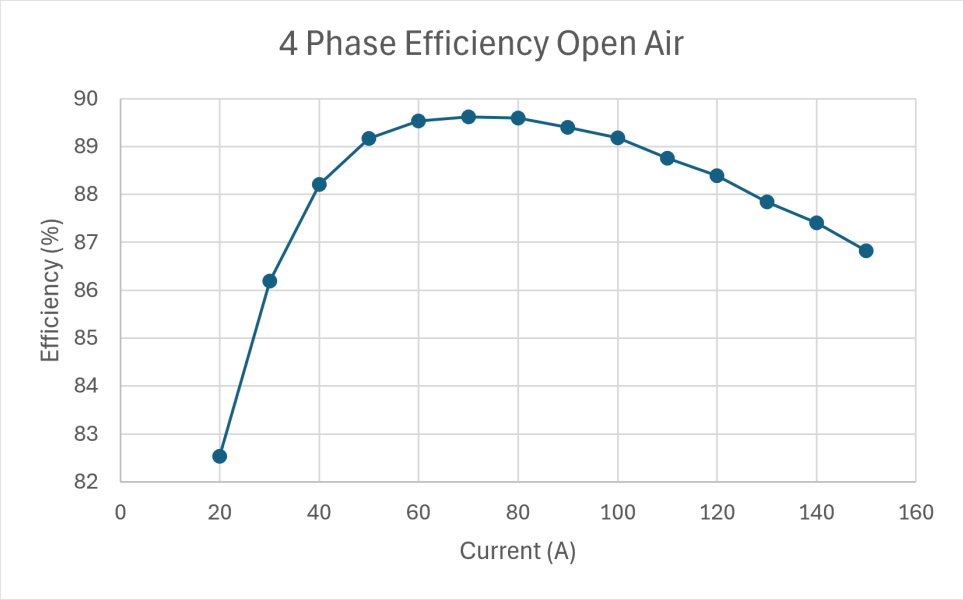


Figure 2-1. Efficiency Graph

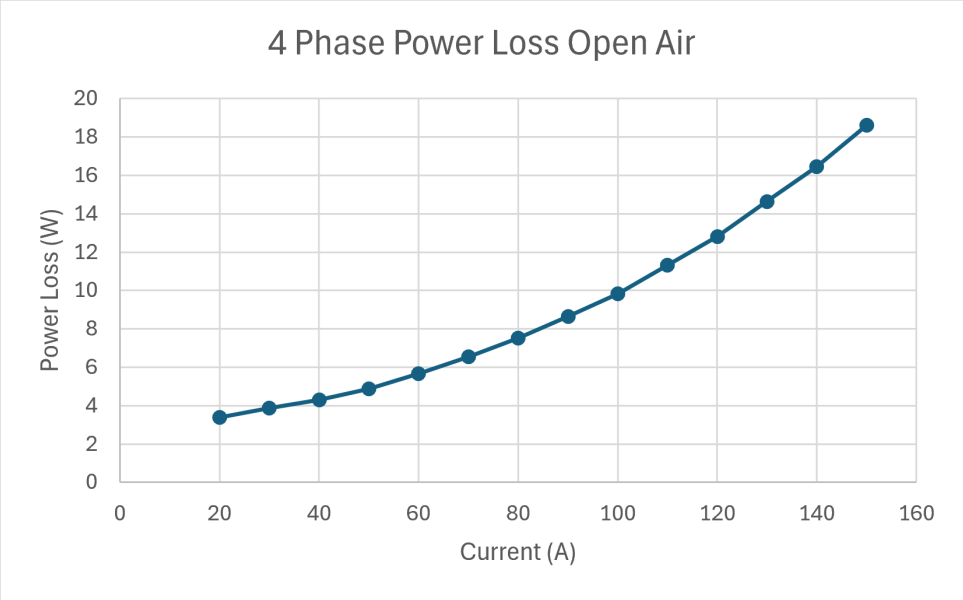


Figure 2-2. Power Loss Graph

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2.2 Efficiency Data

Efficiency data is shown in Table 2-1.

Table 2-1. Efficiency Data

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
12.08	1.61	0.80	20.00	19.42	16.02	3.39	82.53
12.07	2.31	0.80	30.00	27.93	24.08	3.86	86.19
12.06	3.02	0.80	40.00	36.45	32.15	4.30	88.21
12.05	3.75	0.80	50.00	45.12	40.24	4.88	89.18
12.04	4.49	0.81	60.00	54.01	48.35	5.65	89.53
12.03	5.25	0.81	70.00	63.04	56.49	6.55	89.62
12.02	6.02	0.81	80.00	72.17	64.66	7.51	89.59
12.01	6.80	0.81	90.00	81.49	72.86	8.64	89.40
12.00	7.59	0.81	100.00	90.89	81.06	9.83	89.18
12.00	8.41	0.81	110.00	100.63	89.31	11.32	88.75
11.99	9.23	0.81	120.00	110.37	97.56	12.81	88.39
11.97	10.09	0.81	130.00	120.52	105.87	14.65	87.85
11.96	10.94	0.82	140.00	130.62	114.17	16.45	87.40
11.95	11.83	0.82	150.00	141.11	122.51	18.60	86.82

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2.3 Thermal Image

The thermal image was captured after operating at 150A DC for 5 minutes with airflow.

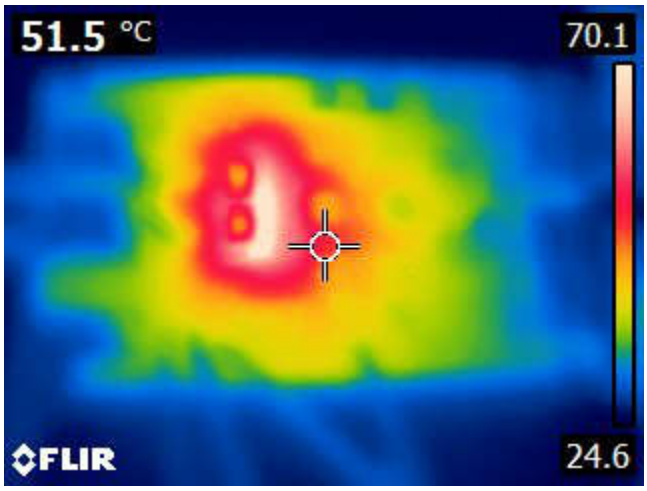


Figure 2-3. Thermal Image at 150A After 5 Minutes With airflow

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3 Waveforms

3.1 Startup

Startup behavior is shown in Figure 3-1.

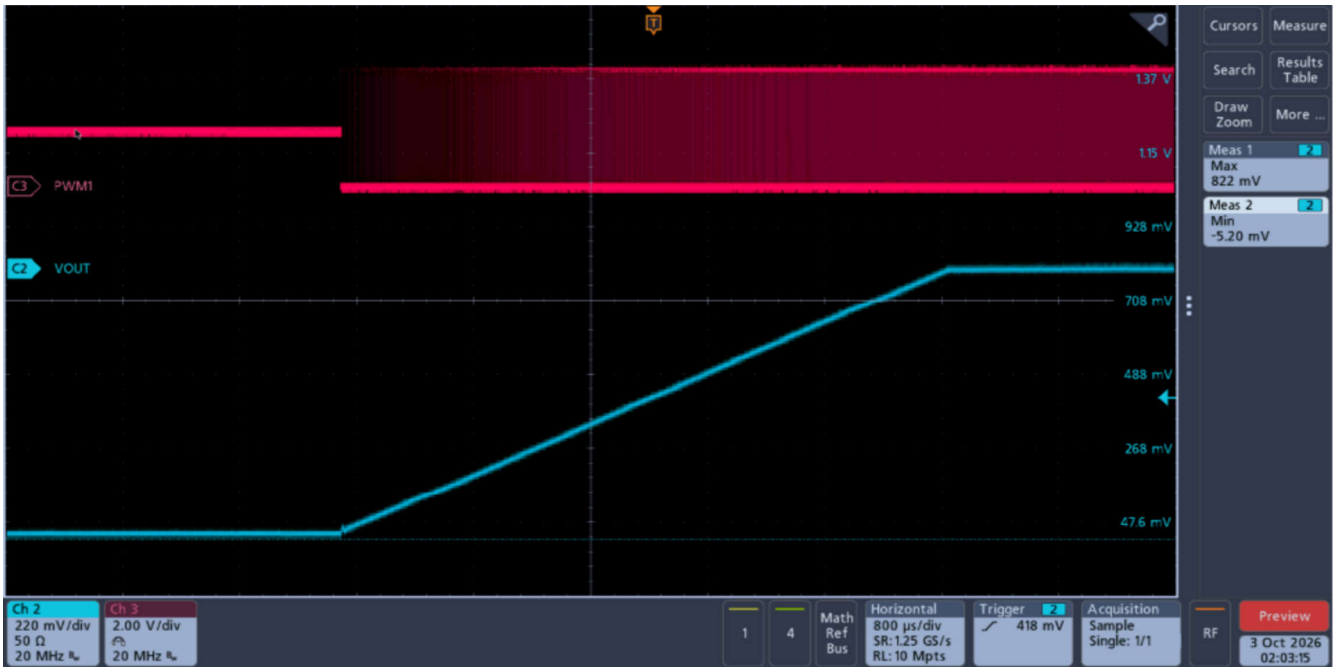


Figure 3-1. Startup

3.2 Output Voltage Ripple

Output voltage ripple is shown in Figure 3-2.

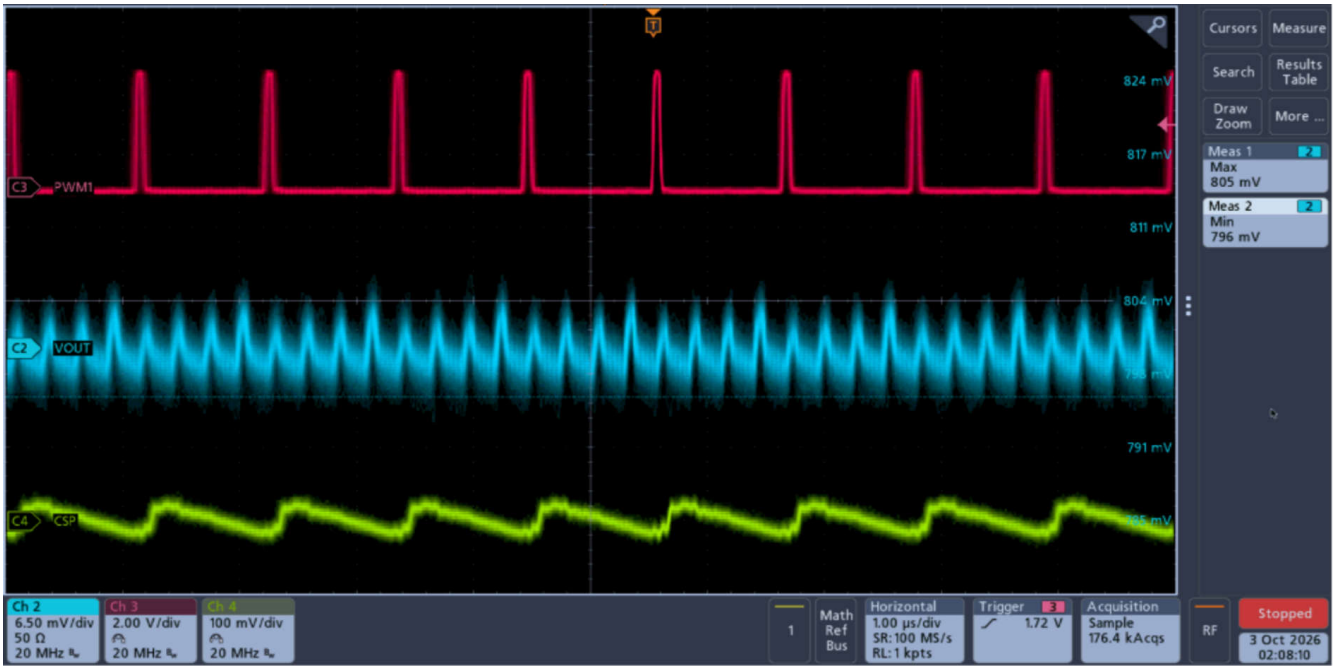


Figure 3-2. Output Voltage Ripple

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3.3 Load Transients

Load transient response was taken from 0A to 100A and 100A to 0A in 1µs.

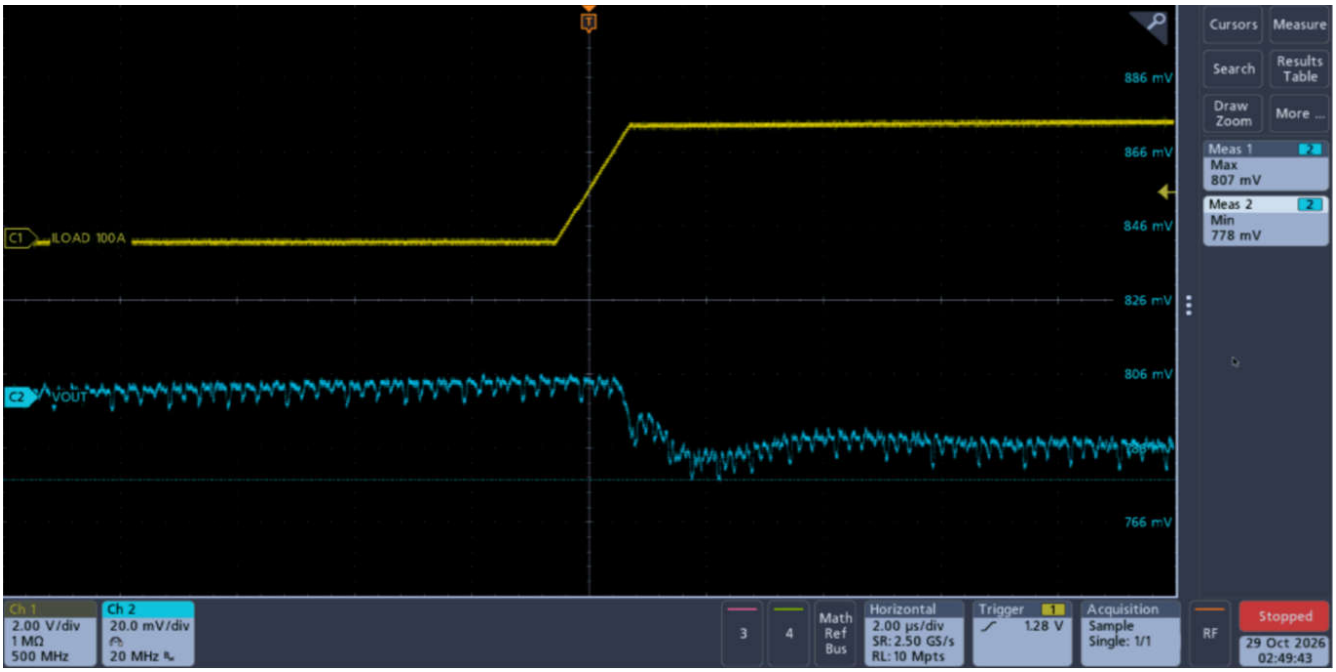


Figure 3-3. Load Transient Rising

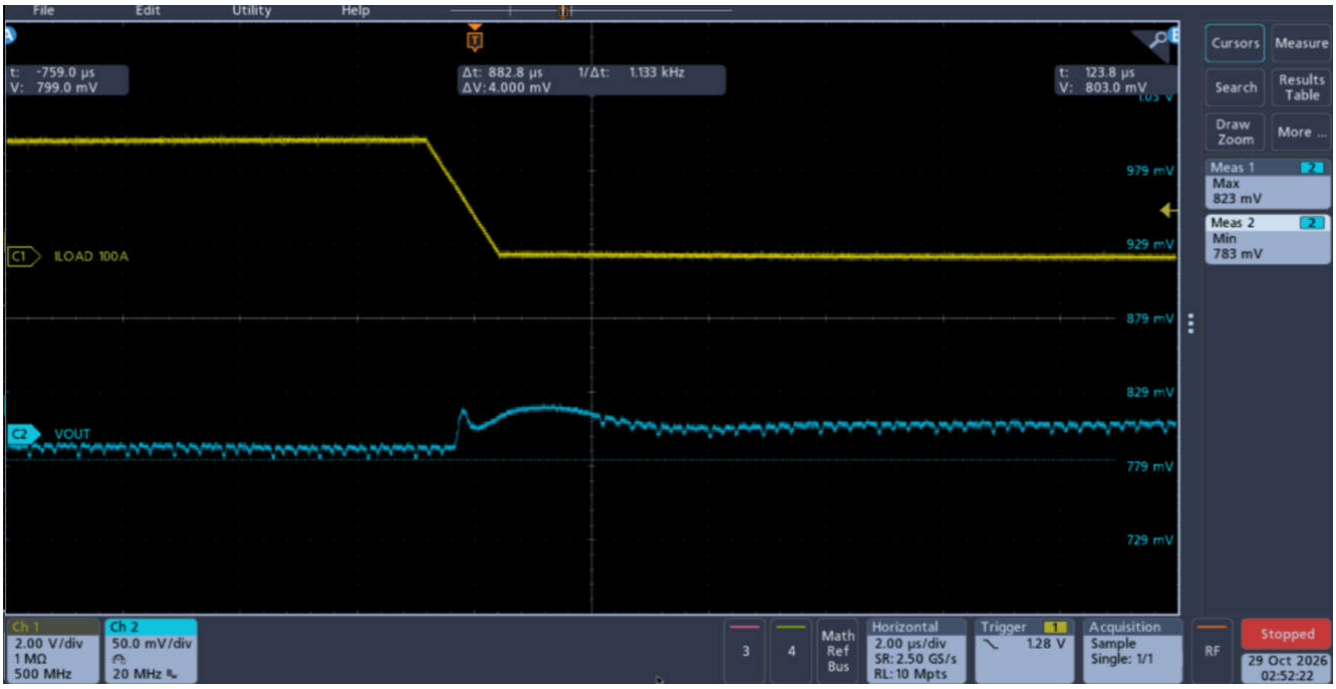


Figure 3-4. Load Transient Falling

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