Application Note

Determining Minimum Acquisition Times for SAR ADCs

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Abstract

The input structure circuit of a successive-approximation register analog-to-digital converter (SAR ADC) in combination with the driving circuit forms a transfer function that can be used to determine minimum acquisition times for different types of applied input signals. This application report, which builds on *Determining Minimum Acquisition Times for SAR ADCs When a Step Function is Applied to the Input* (see Reference 1), investigates the situation when a dc voltage is applied to the input. First, the input structure of the ADC is examined along with the driving circuit. Next, a simple method is derived for calculating the minimum acquisition time for SAR ADCs when the input is a dc voltage. This method will then be compared with the minimum acquisition time derived in the previous application report (see Reference 1). Last of all, three different test cases are evaluated using both exact and approximated equations in order to support the derivations in this report.

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1 Introduction

When it comes to designing the proper input driving circuit for analog-to-digital converters (ADCs), emphasis is typically placed on the calculation of the RC filter in front of the analog input and the selection of an operational amplifier (see Reference 2). The selection of the external RC components depends on the internal structure, sampling sequence, and charge injection of the SAR ADC (see Reference 3 through Reference 5). Knowledge of the internal input structure of the ADC, especially the value of the sampling capacitor, will assist users as they optimize the external RC components to obtain the maximum ac and dc performance from the device (see Reference 6).

The calculation of the external RC filter is simplified by assuming the analog input sampling switch resistance is negligible (see Reference 6). In the following analysis, the analog input sampling switch resistance will be included.

2 SAR ADC Analog Input Equivalent Circuit

A typical analog input driving circuit for the ADC includes an operational amplifier (op amp) as well as an input RC filter composed of R_{IN} and C_{IN} as shown in Figure 2-1. The signal from the driving circuit charges the sampling capacitor C_{SH} through the sampling switch SW with an equivalent on-resistance R_{SW}. The input switch is composed of a CMOS transmission gate or similar structure. The equivalent on-resistance of the sampling switch is not linear and depends on the input signal level (see Reference 7). For this analysis, the average on-resistance of the switch measured over the full-scale input range (FSR) of the ADC will be used.

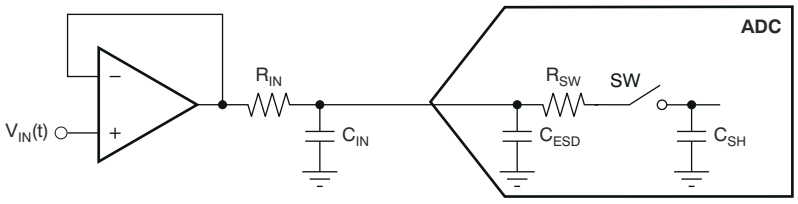

Figure 2-1. Typical SAR ADC Input Driving Circuit

Furthermore, the op amp is assumed to have ideal characteristics. Therefore, it can be modeled as an ideal voltage source. By modeling the op amp in this fashion, the circuit from Figure 2-1 can be simplified to the one shown in Figure 2-2.

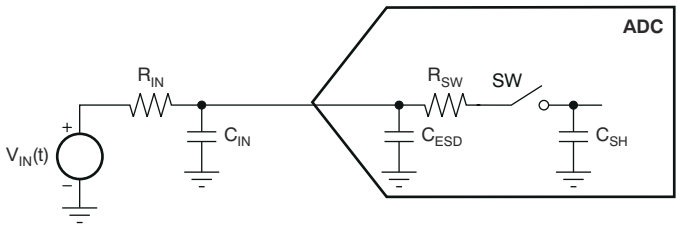

Figure 2-2. Simplified SAR ADC Input Driving Circuit

The ESD protection circuit at the input of the ADC has an equivalent capacitance C_{ESD}. This capacitance is the parallel combination of the protection circuit from the input pin to the power-supply rail and ground. The equivalent capacitance of C_{ESD} is typically between 4 pF and 10 pF. The input filter capacitance C_{IN}, on the other hand, usually ranges from 1 nF to 10 nF. If $C_{IN} >> C_{ESD}$, then C_{ESD} can be neglected. This analysis will represent the parallel combination of C_{IN} and C_{ESD} as capacitor C_1 (see Figure 2-3).

In addition to treating the op amp in Figure 2-1 as ideal, this analysis investigates the case of the input signal pre-charging capacitor C_1 to a constant dc voltage before the sampling switch SW closes. This situation can occur if the input signal $V_{IN}(t)$ changes state during the conversion period of a SAR ADC with a single input channel. It may also occur with a multi-channel SAR ADC, such as the ADS8331/32 (see Reference 8), when another channel is selected during the current conversion. Under these conditions, the input signal $V_{IN}(t)$ can be represented as a constant dc voltage source with magnitude V_{IN}.

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Moreover, the circuit in Figure 2-2 can be represented as a second-order, low-pass filter. The circuit for this case with updated variables is shown in Figure 2-3.

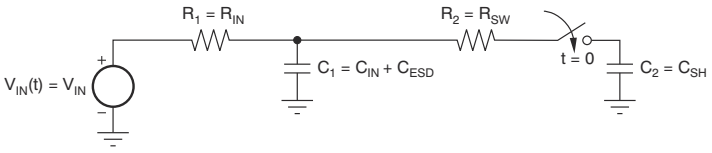

Figure 2-3. SAR ADC Input Driving Circuit Represented as a Second-Order, Low-Pass Filter

The worst-case transient response occurs when the difference in absolute magnitude between the initial voltage on capacitor C_1 [voltage of $V_{IN}(t)$] and the initial voltage on capacitor C_2 is equal to the full-scale input range (FSR) of the SAR ADC. The case where the initial voltage on capacitor C1 [voltage of $V_{IN(t)}$] is at V_{IN} or the positive full-scale voltage (PFS), while the initial voltage on capacitor C_2 is at zero or the negative full-scale voltage (NFS) will be analyzed here. The analysis of this case yields similar results for the case where the initial voltage on capacitor C_1 [voltage of $V_{IN(t)}$] is at zero or NFS while the initial voltage on capacitor C_2 is at V_{IN} or PFS. This second case is left to the reader as an exercise.

The FSR of a SAR ADC is the difference between the PFS and the NFS of the converter. In order to analyze the circuit in Figure 2-3 under worst-case conditions, the initial voltages on capacitors C_1 and C_2 are set to V_{IN} and zero, respectively. Figure 2-4 shows the Laplace transform of the circuit in Figure 2-3 with the initial conditions, reference currents, and voltages that are used in the analysis.

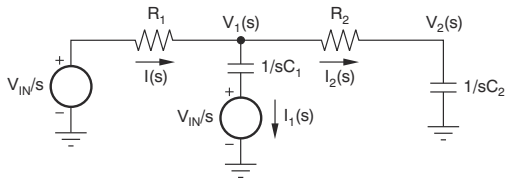

Figure 2-4. Second-Order Filter with Voltages and Currents Defined

The primary goal of this analysis is to determine the minimum acquisition time (t_{ACQ}) for the voltage on capacitor C_2 to settle within 1/2 LSB of the input signal for an *N*-bit SAR ADC as a function of R_1, C_1, R_2, and C_2. In order for this analysis to be performed, an expression for the voltage V_2 across capacitor C_2 as a function of time must be derived. The next section in this application report focuses on this calculation.

3 Mathematical Analysis of the Equivalent Circuit

The Laplace transform of voltage V_2 in Figure 2-4 is:

$$V_2(s) = A(s) \times V_{IN} \tag{1}$$

where:

$$A(s) = \omega_n^2 \times \frac{1}{s} \times \frac{sa + 1}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2}$$

The calculations for Equation 1 and Equation 2 are shown in Appendix A. The inverse Laplace transform of Equation 2 is:

$$A(t) = \frac{\sqrt{\zeta^2\omega_n^2 - \omega_n^2} - \sqrt{\zeta^2\omega_n^2 - \omega_n^2} \times \cosh(t\sqrt{\zeta^2\omega_n^2 - \omega_n^2}) \times e^{-\zeta\omega_n t}}{\sqrt{\omega_n^2(\zeta^2 - 1)}} \tag{3}$$

$$+\frac{a \times \omega_n^2 \times \sinh(t\sqrt{\zeta^2\omega_n^2 - \omega_n^2}) \times e^{-\zeta\omega_n t} - \zeta \times \omega_n \times \sinh(t\sqrt{\zeta^2\omega_n^2 - \omega_n^2}) \times e^{-\zeta\omega_n t}}{\sqrt{\omega_n^2(\zeta^2 - 1)}} \tag{4}$$

After simplifying, Equation 3 can be re-written as follows (see Appendix B for further details):

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$$A(t) = 1 - \frac{1}{2\sqrt{\zeta^2 - 1}} \times \left[\left(\zeta - a\omega_n + \sqrt{\zeta^2 - 1} \right) \times e^{-\omega_n(\zeta - \sqrt{\zeta^2 - 1})t} - \left(\zeta - a\omega_n - \sqrt{\zeta^2 - 1} \right) \times e^{-\omega_n(\zeta + \sqrt{\zeta^2 - 1})t} \right] \quad (5)$$

Equation 5, in turn, can be expressed as:

$$A(t) = 1 - \frac{1}{2\sqrt{\zeta^2 - 1}} \times \left[(\zeta - \mathbf{a}\omega_n + \sqrt{\zeta^2 - 1}) \times e^{-\frac{t}{\tau_1}} - (\zeta - \mathbf{a}\omega_n - \sqrt{\zeta^2 - 1}) \times e^{-\frac{t}{\tau_2}} \right] \quad (6)$$

where time constants τ_1 and τ_2 are defined as Equation 7 and Equation 8, respectively:

$$\tau_1 = \frac{1}{\omega_0(\zeta - \sqrt{\zeta^2 - 1})} \quad (7)$$

$$\tau_2 = \frac{1}{\omega_0(\zeta + \sqrt{\zeta^2 - 1})} \quad (8)$$

In order to observe the effects of these two time constants, Equation 6 can be rewritten as:

$$A(t) = 1 - [k1(t) - k2(t)] \quad (9)$$

where:

$$k1(t) = \frac{\zeta - a\omega_n + \sqrt{\zeta^2 - 1}}{2\sqrt{\zeta^2 - 1}} \times e^{-\frac{t}{\tau_1}} \quad (10)$$

and

$$k2(t) = \frac{\zeta - a\omega_n - \sqrt{\zeta^2 - 1}}{2\sqrt{\zeta^2 - 1}} \times e^{-\frac{t}{\tau_2}} \quad (11)$$

The plots of Equation 9, Equation 10, and Equation 11 as a function of time are shown in Figure 3-1.

The following values were used in Figure 3-1: R_1 = 100 Ω, R_2 = 800 Ω, C_1 = 1000 pF, and C_2 = 40 pF.

These component values set **a** = 100 ns, **b** = 4 ns, and **c** = 32 ns. These values set ω_n = 17.678 Mrad/s and ζ = 1.202. Furthermore, the time constants are calculated to be τ_1 = 105.721 ns and τ_2 = 30.267 ns.

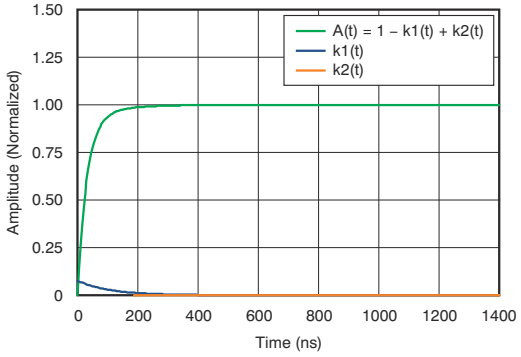

Figure 3-1. Plots of Equations (8), (9), and (10) versus Time

As shown in Figure 3-1, k2(t) decays faster than k1(t) when $\tau_2 << \tau_1$. Under these conditions, Equation 9 can be approximated as a function with only time constant τ_1, or:

$$A(t) \approx 1 - \frac{\zeta - a\omega_n + \sqrt{\zeta^2 - 1}}{2\sqrt{\zeta^2 - 1}} \times e^{-\frac{t}{\tau_1}} \quad (12)$$

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4 Minimum Acquisition Time

In order for the voltage on capacitor C_2 in Figure 2-3 to settle within 1/2 LSB of the input signal for an *N*-bit SAR ADC:

$$A(t) \geq 1 - \frac{1}{2^{N+1}} \tag{13}$$

If k1(t) >> k2(t) at the minimum acquisition time, then A(t) in Equation 13 may be approximated by Equation 12. When this approximation is done, the minimum acquisition time t_{ACQ} for an *N*-bit ADC is (see Appendix C for calculations):

$$t_{ACQ} \geq \frac{1}{\omega_n(\zeta - \sqrt{\zeta^2 - 1})} \times \left[N \times \ln(2) + \ln\left(\frac{\zeta - a\omega_n + \sqrt{\zeta^2 - 1}}{\sqrt{\zeta^2 - 1}} \right) \right] \tag{14}$$

The minimum acquisition time t_{ACQ} for an *N*-bit ADC from the application report *Determining Minimum Acquisition Times for SAR ADCs When a Step Function is Applied to the Input* (see Reference 1) is given in Equation 15.

$$t_{ACQ} \geq \frac{1}{\omega_n(\zeta - \sqrt{\zeta^2 - 1})} \times \left[N \times \ln(2) + \ln\left(\frac{\zeta + \sqrt{\zeta^2 - 1}}{\sqrt{\zeta^2 - 1}} \right) \right] \tag{15}$$

The difference between Equation 14 and Equation 15 is shown in Equation 16:

$$t_{ACQ_STEP} - t_{ACQ_DC} = \frac{1}{\omega_n(\zeta - \sqrt{\zeta^2 - 1})} \times \ln\left(\frac{\zeta + \sqrt{\zeta^2 - 1}}{\zeta - a\omega_n + \sqrt{\zeta^2 - 1}} \right) \tag{16}$$

Here, t_{ACQ_DC} and t_{ACQ_STEP} are the minimum acquisition times in Equation 14 and Equation 15, respectively. Because the ratio in the natural logarithm term in Equation 16 is greater than one, the difference between the acquisition times is a positive quantity. This effect means the acquisition time when the input signal is a step function is greater than the acquisition time when the input signal is a constant dc source, with all other components in the system remaining the same.

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5 Test Cases

In order to evaluate if the approximation derived in Equation 12 is valid, the following test cases were analyzed for a 16-bit ADC (*N* = 16):

- **(a)** $R_1C_1 = R_2C_2 \times 100$
- **(b)** $R_1C_1 = R_2C_2$
- **(c)** $R_1C_1 = R_2C_2 / 100$

The results of these cases are displayed in Table 5-1.

Table 5-1. Results of Three Test Cases

Parameter	Case			Units
	(a)	(b)	(c)	
R_1	100	100	10	Ω
C_1	1000	1000	100	pF
R_2	20	2000	2000	Ω
C_2	50	50	50	pF
$f_1 = \frac{1}{2\pi R_1 C_1}$	1.59	1.59	159	MHz
$f_2 = \frac{1}{2\pi R_2 C_2}$	159	1.59	1.59	MHz
f_2/f_1	100	1	0.01	
a(1)	100	100	1	ns
b(1)	5	5	0.5	ns
c(1)	1	100	100	ns
ω_n(1)	100	10	100	Mrad/s
ζ(1)	5.300	1.025	5.075	
τ_1	105.048	125.000	100.505	ns
τ_2	0.952	80.000	0.995	ns
t_{ACQ}	0.920	1.399	1.184	µs
k1(t_{ACQ})	0.000008	0.000008	0.000008	
k2(t_{ACQ})	0.000000	0.000000	0.000000	
$A(t_{ACQ})_{EQ08}$ (Equation 9)	0.999992	0.999992	0.999992	
$A(t_{ACQ})_{EQ11}$ (Equation 12)	0.999992	0.999992	0.999992	
Error(2)	0.000000	0.000001	0.000000	%

(1) Refer to Appendix A for equations.

(2) $\text{Error} = \left[\frac{A(t_{ACQ})_{(Eq11)} - A(t_{ACQ})_{(Eq08)}}{A(t_{ACQ})_{(Eq08)}}\right] \times 100$

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By using the acquisition times from Table 5-1, the final voltage on the sampling capacitor of the ADC from Figure 2-1 was calculated for each test case by using Equation 12 and Equation 9. The difference in the final voltage calculated with Equation 12 and Equation 9 for each test case is negligible (see Table 5-1 for details). This analysis clearly demonstrates that using the simplified Equation 12 to calculate the final voltage on the sampling capacitor does not introduce any significant error compared to using the exact formula (Equation 9). This assessment is further supported by the plots in Figure 5-1 through Figure 5-3. Another insight revealed by this analysis is that the acquisition times in Table 5-1 are less than the corresponding ones in the previous application report (see Reference 1).

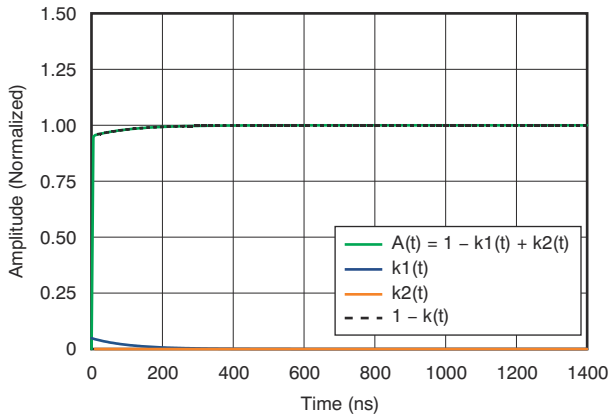

Figure 5-1. Case (a)

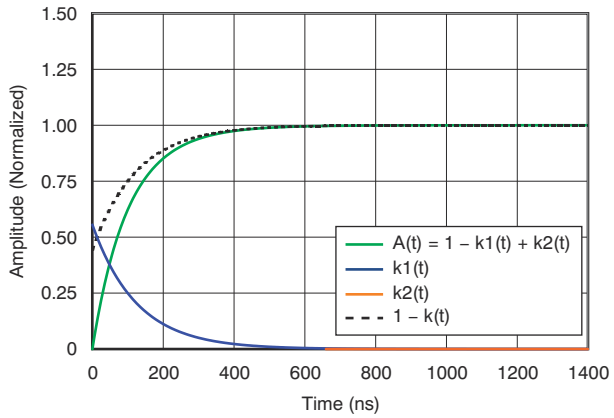

Figure 5-2. Case (b)

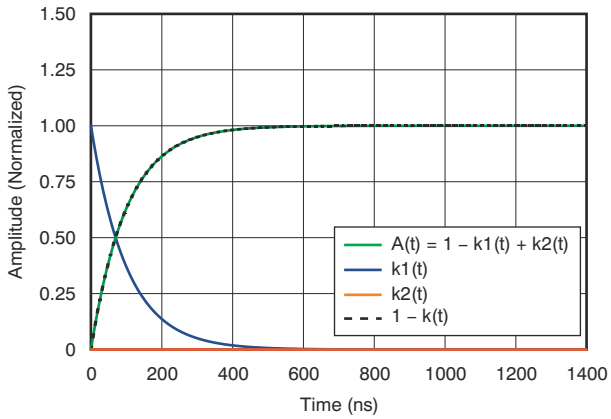

Figure 5-3. Case (c)

6 Conclusion

This report analyzes the input structure along with the driving circuit of a SAR ADC. It provides a simple analytical method for calculating minimum acquisition times for SAR ADCs when a constant dc voltage is applied to the input. Three different test cases were calculated using exact equations as well as simplified ones. The difference in the final acquired voltage calculated with these two equations was negligible. Last of all, it was shown through calculations and test cases that the minimum acquisition time of a system with constant dc source will be less than the identical system using an input step function (see Reference 1).

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7 References

The following documents are available for download through the indicated web sites.

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8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2011) to Revision A (November 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

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A Appendix A

The voltage and currents in the circuit of Figure 2-4 can be described with the following equations:

$$V_1(s) = \frac{I_1(s)}{sC_1} + \frac{V_{IN}}{s} \quad (17)$$

$$V_2(s) = \frac{I_2(s)}{sC_2} \quad (18)$$

$$V_1(s) - V_2(s) = R_2 I_2(s) \quad (19)$$

$$\frac{V_{IN}}{s} - V_1(s) = R_1 I(s) \quad (20)$$

$$I(S) = I_1(S) + I_2(S) \quad (21)$$

Equation 17, Equation 18, and Equation 20 can be rewritten as:

$$I_1(s) = sC_1 V_1(s) - C_1 V_{IN} \quad (22)$$

$$I_2(S) = sC_2 V_2(S) \quad (23)$$

$$I(s) = \frac{V_{IN}}{sR_1} - \frac{V_1(s)}{R_1} \quad (24)$$

Substituting Equation 22 through Equation 24 into Equation 21 yields:

$$V_{IN} = \frac{(s^2 R_1 C_1 + s)V_1(s) + s^2 R_1 C_2 V_2(s)}{sR_1 C_1 + 1} \quad (25)$$

Using Equation 23 in Equation 19 produces:

$$V_1(s) = (sR_2 C_2 + 1)V_2(s) \quad (26)$$

Substituting Equation 26 into Equation 25 produces:

$$V_{IN} = \frac{s[(sR_1 C_1 + 1)(sR_2 C_2 + 1) + sR_1 C_2]}{sR_1 C_1 + 1} \times V_2(s) \quad (27)$$

By using these constants:

a = R_1C_1

b = R_1C_2

c = R_2C_2

Equation 27 can be simplified to:

$$(sa + 1)V_{IN} = s[(sa + 1)(sc + 1) + sb] \times V_2(s) \quad (28)$$

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The voltage $V_2(s)$ can be described as a function of the constant dc source $V_{IN}(t)$ with magnitude V_{IN} by rearranging Equation 28 to yield:

$$V_2(s) = \frac{1}{ac} \times \frac{1}{s} \times \frac{sa + 1}{s^2 + s\frac{a + b + c}{ac} + \frac{1}{ac}} \times V_{\text{IN}} \tag{29}$$

The coefficients in Equation 29 can be represented as:

$$\frac{a + b + c}{ac} = 2\zeta\omega_n \tag{30}$$

and

$$\frac{1}{ac} = \omega_n^2 \tag{31}$$

Substituting Equation 30 and Equation 31 into Equation 29 produces:

$$V_2(s) = A(s) \times V_{\text{IN}} \tag{32}$$

where:

$$A(s) = \omega_n^2 \times \frac{1}{s} \times \frac{sa + 1}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{33}$$

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B Appendix B

The equation:

$$A(t) = \frac{\sqrt{\zeta^2\omega_n^2 - \omega_n^2} - \sqrt{\zeta^2\omega_n^2 - \omega_n^2} \times \cosh(t\sqrt{\zeta^2\omega_n^2 - \omega_n^2}) \times e^{-\zeta\omega_n t}}{\sqrt{\omega_n^2(\zeta^2 - 1)}} \tag{34}$$

$$+\frac{a \times \omega_n^2 \times \sinh(t\sqrt{\zeta^2\omega_n^2 - \omega_n^2}) \times e^{-\zeta\omega_n t} - \zeta \times \omega_n \times \sinh(t\sqrt{\zeta^2\omega_n^2 - \omega_n^2}) \times e^{-\zeta\omega_n t}}{\sqrt{\omega_n^2(\zeta^2 - 1)}} \tag{35}$$

Can be reduced to:

$$A(t) = 1 - e^{-\zeta\omega_n t} \times \left[\cosh\left(\omega_n\sqrt{\zeta^2 - 1}t\right) - \frac{a\omega_n - \zeta}{\sqrt{\zeta^2 - 1}} \times \sinh(\omega_n\sqrt{\zeta^2 - 1}t)\right] \tag{36}$$

The definitions of the hyperbolic sine and hyperbolic cosine terms are:

$$\sinh(x) = \frac{e^x - e^{-x}}{2} \tag{37}$$

$$\cosh(x) = \frac{e^x + e^{-x}}{2} \tag{38}$$

The arguments of the hyperbolic sine and hyperbolic cosine terms in Equation 36 can be defined as:

$$X = \omega_n\sqrt{\zeta^2 - 1}t \tag{39}$$

Substituting Equation 39 into Equation 37 and Equation 38 yields:

$$\sinh(\omega_n\sqrt{\zeta^2 - 1}t) = \frac{e^{\omega_n\sqrt{\zeta^2 - 1}t} - e^{-\omega_n\sqrt{\zeta^2 - 1}t}}{2} \tag{40}$$

and

$$\cosh(\omega_n\sqrt{\zeta^2 - 1}t) = \frac{e^{\omega_n\sqrt{\zeta^2 - 1}t} + e^{-\omega_n\sqrt{\zeta^2 - 1}t}}{2} \tag{41}$$

Using Equation 40 and Equation 41 in Equation 36 produces:

$$A(t) = 1 - e^{-\zeta\omega_n t} \times \left[\frac{e^{\omega_n\sqrt{\zeta^2 - 1}t} + e^{-\omega_n\sqrt{\zeta^2 - 1}t}}{2} - \frac{a\omega_n - \zeta}{\sqrt{\zeta^2 - 1}} \times \frac{e^{\omega_n\sqrt{\zeta^2 - 1}t} - e^{-\omega_n\sqrt{\zeta^2 - 1}t}}{2}\right] \tag{42}$$

By re-arranging the terms, Equation 42 can be simplified to:

$$A(t) = 1 - \frac{1}{2\sqrt{\zeta^2 - 1}} \times \left[\left(\zeta - a\omega_n + \sqrt{\zeta^2 - 1}\right) \times e^{-\omega_n(\zeta - \sqrt{\zeta^2 - 1})t} - \left(\zeta - a\omega_n - \sqrt{\zeta^2 - 1}\right) \times e^{-\omega_n(\zeta + \sqrt{\zeta^2 - 1})t}\right] \tag{43}$$

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C Appendix C

For k1(t) >> k2(t), Equation 6 reduces to:

$$A(t) \approx 1 - \frac{\zeta - a\omega_n + \sqrt{\zeta^2 - 1}}{2\sqrt{\zeta^2 - 1}} \times e^{-\frac{t}{\tau_1}} \tag{44}$$

In order for Equation 44 to satisfy the criteria in Equation 13 for minimum acquisition time t_{ACQ}:

$$\frac{1}{2^{N+1}} \geq \frac{\zeta - a\omega_n + \sqrt{\zeta^2 - 1}}{2\sqrt{\zeta^2 - 1}} \times e^{-\frac{t_{ACQ}}{\tau_1}} \tag{45}$$

Re-arranging the terms in Equation 45 and solving for t_{ACQ} yields:

$$t_{ACQ} \geq \tau_1 \times \left[N \times \ln(2) + \ln\left(\frac{\zeta - a\omega_n + \sqrt{\zeta^2 - 1}}{\sqrt{\zeta^2 - 1}} \right) \right] \tag{46}$$

Using Equation 7 to replace τ_1 in Equation 46 produces the inequality:

$$t_{ACQ} \geq \frac{1}{\omega_n(\zeta - \sqrt{\zeta^2 - 1})} \times \left[N \times \ln(2) + \ln\left(\frac{\zeta - a\omega_n + \sqrt{\zeta^2 - 1}}{\sqrt{\zeta^2 - 1}} \right) \right] \tag{47}$$

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Last updated 10/2025