Using the CDC857 and CDCV850 to Transform a Single-Ended Clock Signal Into Differential Outputs

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ABSTRACT

The CDC857 and the CDCV850 devices are PLL-based differential clock drivers with a maximum operational frequency of 167 MHz. These devices have been designed to support a double-data-rate (DDR) specification and, therefore, they have higher immunity against incoupling common mode noise. However, they require a differential clock input signal.

This report shows (a) how to convert a single ended clock signal into a differential clock signal, (b) how to find a useful circuit and (c) pitfalls for the designer. Measurement results given at the end of the report verify the suggestions made.

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1 Introduction

The major system difference between a double-data-rate (DDR) type clock driver and a standard clock driver is that the DDR driver clocks data on both the rising and falling edges of the clock signal, and thus interprets every clock edge as a strobe signal. Differential signals are preferred because of their greater immunity to incoupling common mode noise.

The CDC857 and CDCV850 differential clock drivers have a differential clock input. Unfortunately, today's available clock synthesizers usually do not have a differential clock output with which to feed the double data rate (DDR) input. Exceptions are the CDC930-, CDC936- and CDC950-clock synthesizers that offer differential outputs at 100 MHz, 133 MHz and 200 MHz. However, if these frequencies do not fit the application's needs, or if there is some other reason to convert a single-ended clock signal into a differential signal, then the following critical design issues must be given attention:

- A setup is needed that minimizes jitter introduced by the CDC857 clock driver.
- To achieve similar noise performance, the edge of the single-ended signal will need to rise twice as fast compared to a one-line input from a differential source.
- Two setups of the CDCs are possible: a buffered mode and a PLL-enabled mode. If the PLL mode is required in order to lock to the clock input signal with zero phase error, the feedback from FBOUT to FBIN must be routed in a similar way to that of the CLK input. If this is not done, the circuitry variations around the CDC will add an offset to the static phase error, and a maximum phase variation of ±150ps can no longer be ensured.

The CDC857 and CDCV850 differential clock drivers have certain specific parameters that are important to their use in the proposed application.

1.1 CDC857 Parameters

Within the CDC857 family, two devices from Texas Instruments are available. The CDC857-3 has V_{CC} = 2.5 V but with the PLL running at AV_{CC} = 3.3 V. The CDC857-2 works with all rails at 2.5 V (V_{CC} = AV_{CC} = 2.5 V).

INPUT:

Input slew rate: ≥ 1 V/ns

- The 10%-90% rise time, therefore, needs to be at or below 2 ns.

Clock frequency: (66 - 167) MHz

Clock input:

Voltage swing (ac): recommended: 0.7 V ≤ swing ≤ V_{CC} + 0.6 V
tolerated: rail-to-rail

- The minimum swing under normal operating conditions is 0.7 V.
- From a dc perspective, a voltage swing above 0.35 V will already ensures switching.

DC input voltage: –0.3 V ≤ dc voltage ≤ V_{CC} + 0.3 V

- Any input signal has to fall within this range. Ideally the differential input will swing around V_{CC}/2 but the signal is allowed to shift anywhere within ±300mV of the rail voltage.

Differential crossing point: V_{CC}/2 ± 200 mV

OUTPUT:

Differential crossing point: $V_{CC}/2 \pm 100$ mV

1.2 CDCV850 Parameters

The CDCV850 is the latest DDR clock driver from TI and offers ac inputs. This component is pin compatible with the CDC857 with the exception that an I2C I/O replaces the enable pin of the CDC857.

A decoupling circuit in series with the clock input obviates the need for external components. The CDCV850 operates from a dual 2.5 V / 3.3 V supply.

INPUT:

Input slew rate: $\geq$ 1 V/ns

- The 10%-90% rise time, therefore, needs to be at or below 2 ns.

Clock frequency: (66 - 170) MHz

Clock input:

Voltage swing (ac): rail-to-rail

- The minimum swing under normal operating conditions is 0.7 V.

OUTPUT:

Differential crossing point: $V_{CC}/2 \pm 100$ mV

2 Proposed Solutions

Both the CDC857 and the CDCV850 devices can be used to convert single-ended clock signals into differential clock signals. The preferred choice of device depends on the type of application. As previously mentioned, the CDCV850 already has a decoupled CLK input. Therefore, just by tying the single ended clock signal to the CLK input, this device allows a setup with the lowest number of components. On the other hand, if a certain phase shift of the input signal is required or if the input frequency falls below 20MHz, the CDC857 might be the better choice, since the CLK input allows dc-coupling. There are also considerations regarding the PLL.

The designer has to choose if the PLL will be used at all. Some of the factors that affect that decision are:

- ***Best Jitter Performance:*** The best jitter performance can be achieved with an accurate clock source and the PLL disabled.
- ***Jitter Filtering****:* A clock source with high jitter can be corrected by the CDC with the PLL enabled. Here it is important that the jitter frequency band is above the bandwidth of the CDC's internal PLL. The cutoff frequency is design- and device-dependent, with a typical value of a few MHz.
- ***Zero Delay Buffer:*** In case a zero delay buffer is required, the PLL must be enabled.
- ***Duty Cycle Correction:*** If the duty cycle of the clock input signal is unbalanced, the PLL of the CDC can correct the duty cycle to 50%. The clock driver's PLL phase aligner adjusts to only one of the two incoming edges, thus correcting the input duty cycle error.

2.1 Possible CDC857 Circuits

2.1.1 A Workable Circuit

The most promising way to a reasonable setup seems to be to shift both the CLK and $\overline{CLK}$ signals to $V_{CC}/2$ and couple the input signal into the CLK input.

Possible problem: An incoupling network uses a capacitor that, together with the resistor network connected to the power terminals, forms a high-pass filter. Consequently, a frequency-dependent phase shift will be introduced into the CLK input circuitry. If signal delay through the CDC is critical to the application, this additional phase shift will add further delay.

Correction when PLL is enabled: If the PLL is being used on the clock driver, a feedback line must be wired from the CDC output FBOUT/$\overline{FBOUT}$ to the input terminal FBIN/$\overline{FBIN}$. If one can ensure the same delay in the feedback loop, then the phase error will be corrected. This can be accomplished by using exactly the same RC network in the feedback loop, as the one that is coupling the input signal into the CLK pins.

Tradeoff when CDC857 runs in buffered mode (PLL disabled): The input duty cycle will worsen if the trigger voltage is offset from the mean of the input signals. It will worsen also in proportion to the rise time, causing an asymmetrical swing in the CDC857 outputs.

2.1.2 Simplified Circuitry for the CDC857

Another, even simpler setup is to bring just $\overline{CLK}$ to $V_{CC}/2$ and connect the CLK signal directly to the input. The weakness in this solution is that it requires symmetry of the driving-clock input signal about $V_{CC}/2$.

2.1.3 Fail Safe

Ensuring system reliability even when the input clock signal becomes lost (e.g. backplane cards), is detailed later in this report. If, when the PLL is enabled, there occurs a very low input frequency (far below minimum input frequency specified in the data sheet), the detection logic within the clock driver puts the device outputs into a high impedance state. This feature also makes up for a loss of signal on the CLK/$\overline{CLK}$ input.

2.2 Possible CDCV850

2.2.1 A Workable Circuit

On the CDCV850, the CLK and $\overline{CLK}$ inputs already have an RC high-pass filter built into them. Thus, no external component is required to interface those inputs with the clock signal. The simplest circuit is to tie the CLK input to the single-ended clock signal and tie the $\overline{CLK}$ input to GND or V_{CC}.

Possible problem: The input high-pass filter will introduce a certain frequency-dependent phase shift. If the signal delay through the CDC is critical to the application, this phase shift will introduce an additional delay. The design was optimized to keep this phase shift negligible over the specified operating bandwidth, but care must be taken at low frequencies.

Correction when PLL is enabled: As already mentioned when discussing possible CDC857 circuits, the PLL, together with a feedback loop, can be used to build a zero-delay buffer. The physical length of the feedback loop adjusts the lengths of the clock input and output lines. As long as the feedback line matches the electrical length of the clock line, the CDCV850 should have a zero device delay. The inputs FBIN/$\overline{\text{FBIN}}$ and CLK/$\overline{\text{CLK}}$ of the CDCV850 are identical except that FBIN draws more current than CLK to make up for voltage swing differences between the clock and the feedback signals. In theory, the static phase error can be corrected easily by applying similar conditions to both complementary inputs. In practice, a straight connection between FBOUT/$\overline{\text{FBOUT}}$ and FBIN/$\overline{\text{FBIN}}$ is perfectly adequate.

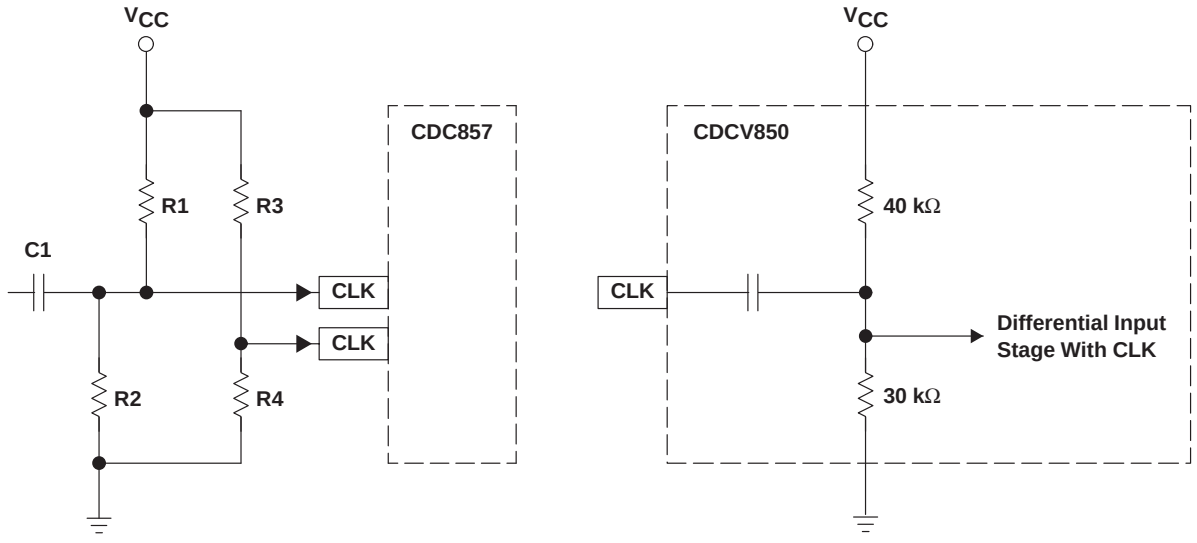
Fail safe : The CDCV850 detects if the input signal is lost, or if it falls below the 20 MHz minimum input frequency. The 20MHz limit is an historical value and specifies only that the CDC needs to be working with an input signal above that frequency. On the other hand, a dc signal must always be detected. There is no specification on the frequency at which the device should switch off. TI has chosen to set this value at a few MHz (typically 3 MHz). In that case, all outputs go into a high-impedance state. A combination of pullup and pulldown resistors on the input stage of the driven device could be used to ensure a stable logic level when outputs are in a high-impedance state. Some differential input stages already have a built in fail-safe circuit, e.g., all of TI's LVDS devices.

3 Design and Implementation

In this section, an approach to designing an easy setup that addresses and overcomes the foregoing issues is described. Then, a proposal is made of a useful design and the steps taken to adjust all the parameters are outlined. Finally, an error analysis is presented

3.1 Initial Design Proposal

To shift the dc input voltage of the clock inputs to $V_{CC}/2$ and to couple the input signal into one of the two CLK input pins, the simple RC network shown in Figure 1(a) can be used. This circuit is already built into the CDCV850, as seen in Figure 1(b).



a) Input Circuitry for Single-ended Drive Signal Into the CLK Differential Input of the CDC857

b) Simplified Input Circuit of the CDCV850 CLK Input

Figure 1. Input Circuitry of CDC857 and CDCV850

If the clock signal driving the CDC85x has a voltage swing of 2.5V, the input network of R1, R2 and C1 is not needed. In that case, a simple line termination is sufficient.

3.2 Calculation of the Input Resistors R_1, R_2

The values for resistors R1 and R2 depend on the drive capability of the driving-clock signal and the impedance of the signal trace on the PCB. To save power, the resistor values are typically 10 kΩ. To minimize effects of incoupling noise for this test application, a 50-Ω transmission line and a 50-Ω line driver were used. Thus,

$$R_1 \| R_2 = R_3 \| R_4 = \frac{R_1 \times R_2}{R_1 + R_2} = \frac{R_3 \times R_4}{R_3 + R_4} = 50\ \Omega \quad (1)$$

If the voltage on the CLK and $\overline{CLK}$ inputs is set to $V_{CC}/2$, then

$$R_1 = R_2 = R_3 = R_4 = 100\ \Omega \quad (2)$$

Ideally, the CLK terminal should have the same voltage ($V_{CC}/2$) as $\overline{CLK}$.

Consider now the situation when the clock input signal is lost, e.g., in a card-plug environment. Suddenly, no driving signal is applied to the capacitor, C_1. When using the clock driver with the PLL enabled, the built-in low-frequency detection circuit will detect the signal loss and disable all outputs. Using the CDC in buffered mode, the signal loss might allow incoupling noise to start the CDC857 oscillating. To prevent this from happening, the voltage at the R_1–R_2 node must either be increased to a logical high or decreased to a logical low. According to the data sheet, a differential voltage V_{ID}, greater than 350 mV between $\overline{CLK}$ and CLK must be applied to the inputs . This could be achieved by using an asymmetrical resistor network on the CLK input, e.g. 82 Ω and 130 Ω. On the other hand, this would also be the source of duty cycle error. Therefore, the two termination circuits shown in Figure 2 are recommended for the buffered mode.

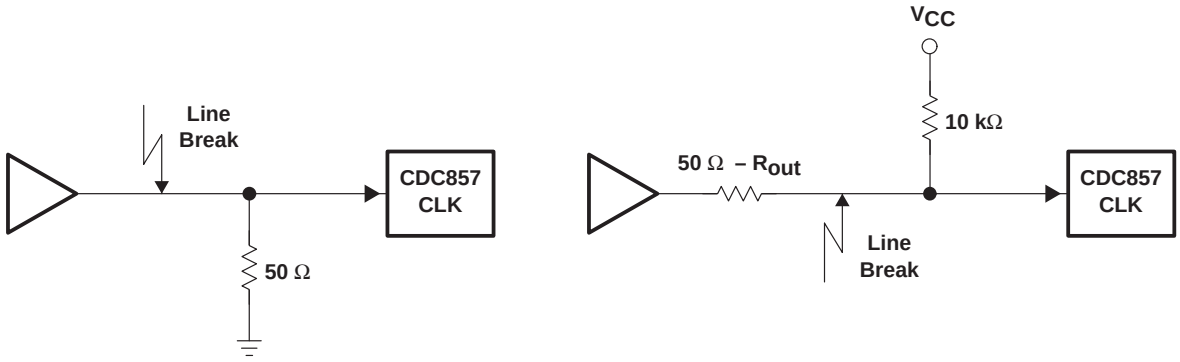


Figure 2. Loss of Signal Protection—Left: Termination at the Line End; Right: Serial Termination and a 10-kΩ Pullup Resistor for Fail Safe

3.3 Determination of the Value of the Coupling Capacitor, C1

As shown in Figure 1(a), the coupling capacitor, C_1, and the resistor network, $R_1||R_2$, form a high-pass filter. The clock frequency of the CDC857 is important to the determination a good value for C_1. The cutoff frequency of the high-pass filter should be lower than the lowest expected operating frequency of the device. The larger the value of C_1, the lower will be the cutoff frequency. On the other hand, to ensure a good rectangular (trapezoidal) shape for the input signal, it is also important that many harmonics of the fundamental wave can pass the filter. Because larger capacitors have higher lead inductance, they attenuate high frequencies; thus, it could be recommended that the fastest capacitor available be selected.

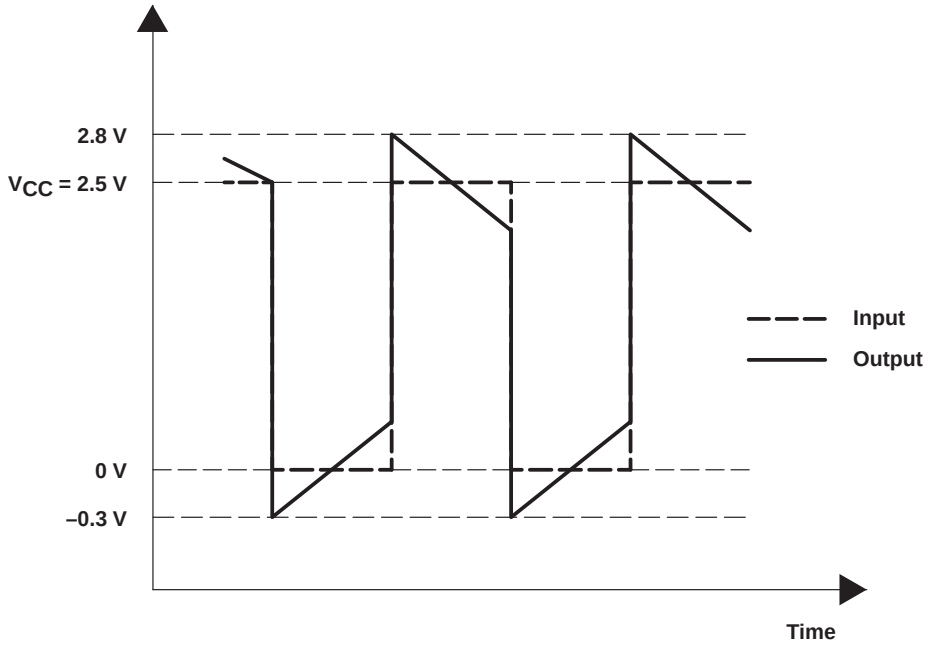


Figure 3. Rectangular and Saw Tooth Signals

As shown in Figure 3, the clock input signal into the capacitor has a rectangular or trapezoidal shape; therefore, in addition to its fundamental frequency, it also contains several harmonics that are attenuated with 20 dB/dec and 40 dB/dec. When such a signal enters a high-pass filter, the output easily follows the rising edges. Then, during the high- and low-times when the voltage remains constant, the voltage across the capacitor discharges. The problem that arises now is that, depending on the amount of discharge, the peak voltage of the next rising edge will exceed the rail voltage V_{CC} or undershoot the GND potential on the falling edge. In contrast, the data sheet allows the signal to depart from the rail voltage by, at most, ±300 mV. Therefore, the capacitor must be chosen large enough to guarantee that these under- and over-shoots do not exceed 300 mV above or below the rail voltage.

To determine the capacitor C_1, one needs either to have knowledge of the input signal shape or to use the worst-case input signal—a rectangular pulse. It is well known that the simple, high-pass, RC filter shown in Figure 4 has the time constant RC_1 and its cutoff frequency is

$$f_{CO} = 1/(2\pi\tau) = 1/\left(2\pi RC_1\right) \quad (3)$$

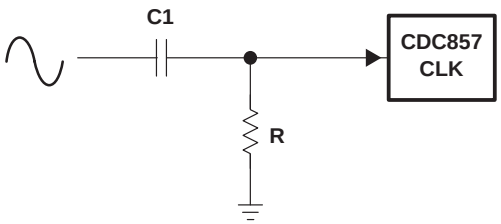


Figure 4. Simple RC Circuit

Thus, if this circuit contains a 100-Ω resistor, and ideal sine waves having frequencies greater than 66MHz are to be applied to the CLK input, a capacitance of 47 pF is required for an output signal amplitude of -3 dB. The phase shift is

$$\varphi = \arctan(\omega \tau) = \arctan\left(2\pi RC_1\right) \quad (4)$$

To deal with a rectangular input, the circuit of Figure 5 can be used. Here, the designer must ensure that the input signal to CLK neither exceeds (V_{CC} + 300 mV) nor falls below (GND – 300 mV). This circuit can be simplified to the one shown in Figure 6.

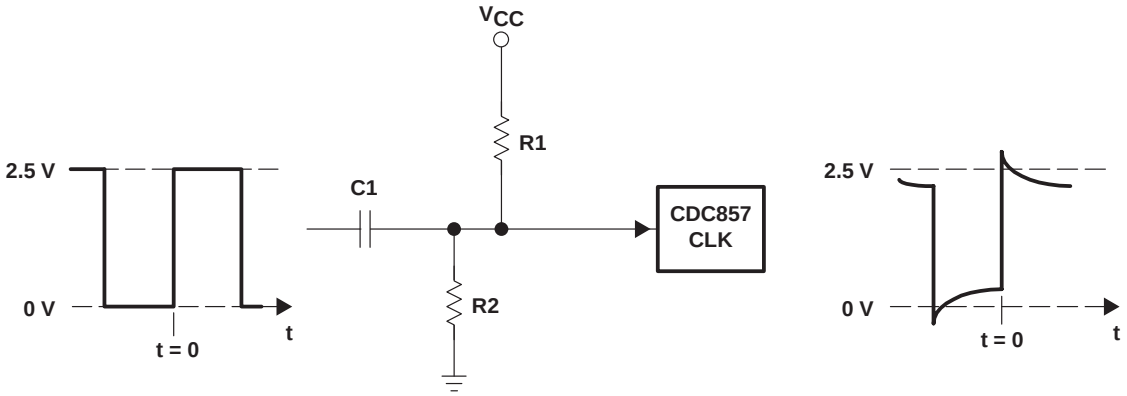


Figure 5. Rectangular Input Into R1/R2 Divider

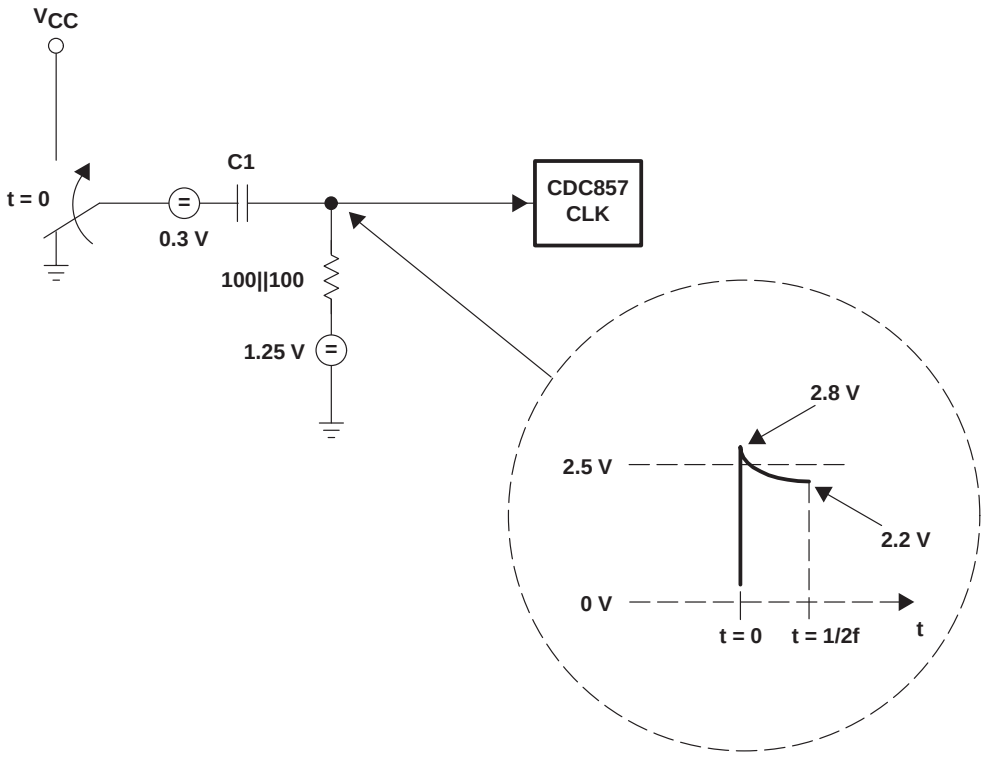


Figure 6. Simplification of the Circuit in Figure 5 for Approximation of Required Capacitance, C_1

The instantaneous voltage at CLK is

$$V(t) = \left(V_{pulse} + 0.3\ V – 1.25\ V\right) \exp(–t/\tau) + 1.25\ V = 1.55\ V \exp(–t/\tau) + 1.25\ V \quad (5)$$

$$\tau = R \times C_1 \quad (6)$$

$$C_1 = \frac{–t}{2 \times R \times f_{min} \times \ln\left(\frac{V(t)–1.25}{1.55\ V}\right)} \quad (7)$$

Using t = 1/2f, a minimum frequency of 66 MHz, and $V(t) = V_{CC} – 0.3\ V = 2.2\ V$ gives $C_1 \geq 310$ pF.

Based on this worst case, C_1 should be larger than 310 pF—a 680-pF capacitor would be preferred. The test results presented later in this report were obtained using a 1.5-nF capacitor.

It should be noted that the real signal will have a finite rise time; therefore, the high-pass (C_1+$R_1||R_2$) filter will shift the phase of the clock input signal. The shorter the rise time, the larger will be the phase shift. The size of the capacitor is proportional to the phase shift. Thus, if one uses the PLL mode to align the input and output phases, the capacitor must be large enough to follow the slowest-rising signal.

3.4 Error Analysis

The components that make up the external circuitry are all manufactured to limited tolerances and, therefore, all will contain errors or exhibit deviations from prescribed values. Such errors inevitably affect the accuracy of a clock signal. The effect of random deviations in the values of resistors and capacitors is discussed in the following.

3.4.1 Effect of Resistor Tolerances

A variation in the values of the four resistors R_1...R_4 will shift the dc level on the CLK terminals away from ideal $V_{CC}/2$. The tolerance of the resistors (given in percent) depends on temperature; therefore, having the resistors in close physical proximity to one another will improve the tolerance a little. However, consider the worse case with the four-resistor network of Figure 1(a). Tolerances ΔR_1 and ΔR_2 lead to the following, worst-case values of the CLK voltage:

$$V_{CLK} \pm \Delta V_{CLK} = V_{CC} \times \frac{R_2 \pm \Delta R_2}{R_1 \mp \Delta R_1 + R_2 \pm \Delta R_2} = \frac{V_{CC}}{2} \pm \Delta\left(\frac{R_2}{R_1 + R_2}\right) \quad (8)$$

When the tolerances are equal but opposite, the denominator of equation (8) is least and the error in V_{CLK} is greatest. The result is:

$$V_{CLK} \pm \Delta V_{CLK} = \frac{V_{CC}}{2}\left(1 \pm \frac{\Delta R}{R}\right) \quad (9)$$

and the relative error in the CLK voltage is directly proportional to the tolerance of the resistors. Thus, if the resistor tolerance is ±10%, the output V_{CLK} can see a dc voltage between 450 mV and 550 mV. Since the same analysis is valid for the $\overline{CLK}$ pin , the result is that the voltage difference ($V_{CLK} - V_{\overline{CLK}}$) can be as high as ±100 mV. This difference will result in duty cycle error of the CDC857 outputs that is directly proportional to the rise time of the input signal and is reciprocal to the operating frequency.

As long as the tolerances of R3 and R4 remain identical, the absolute resistor value can be chosen within a wide range to adjust the dc level on the $\overline{CLK}$ terminal. Our low-impedance choice of 100-Ω resistors in parallel, as used in the tests described in this report, is not necessary, and even 2 kΩ should work satisfactorily.

The only additional sources of error are (i) the $\overline{CLK}$-pin current, which is drawn only through one of the resistors, and (ii) the fact that a high-impedance resistor network is more sensitive to incoupling noise. A good solution might be to buffer this input with an additional capacitor, C_{buffer}, against ground to shortcut noise (see Figure 7). An additional diode to V_{CC} will be a good choice if a fast discharge of C_{buffer} is required to prevent a latch-up of the single-ended clock-driver output.

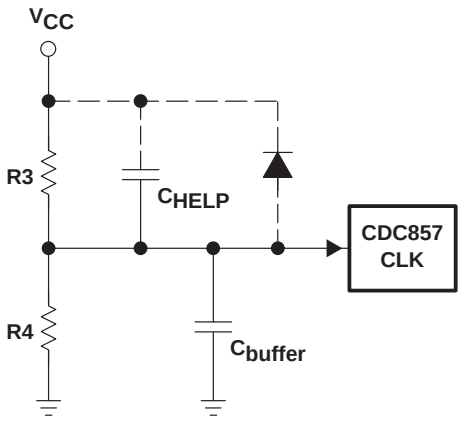


Figure 7. Input Buffering

Tradeoff using C_{buffer}: When powering up, the capacitor needs to be charged; therefore, there will be a time delay before $\overline{CLK}$ sees $V_{CC}/2$. If this time delay is unacceptable, another capacitor, C_{HELP}, tied to V_{CC}, would solve the problem. However, in that case the designer should ensure that this path is not the lowest impedance trace for shorting high-speed noise on the PCB; otherwise, the $\overline{CLK}$ input will collect all the spurious signals.

3.4.2 Effect of C_1 Tolerance

The tolerance of C_1 will not influence the dc performance of the input stage but it does affect the cutoff frequency of the high-pass filter comprised of C_1 and $R_1||R_2$. However, this behavior is not critical to the application if C_1 has been chosen a little larger than is ideally required—see discussion accompanying equation (3).

4 Experimental Verification

The test setup shown in Figure 7 was used for validation of the foregoing proposals.

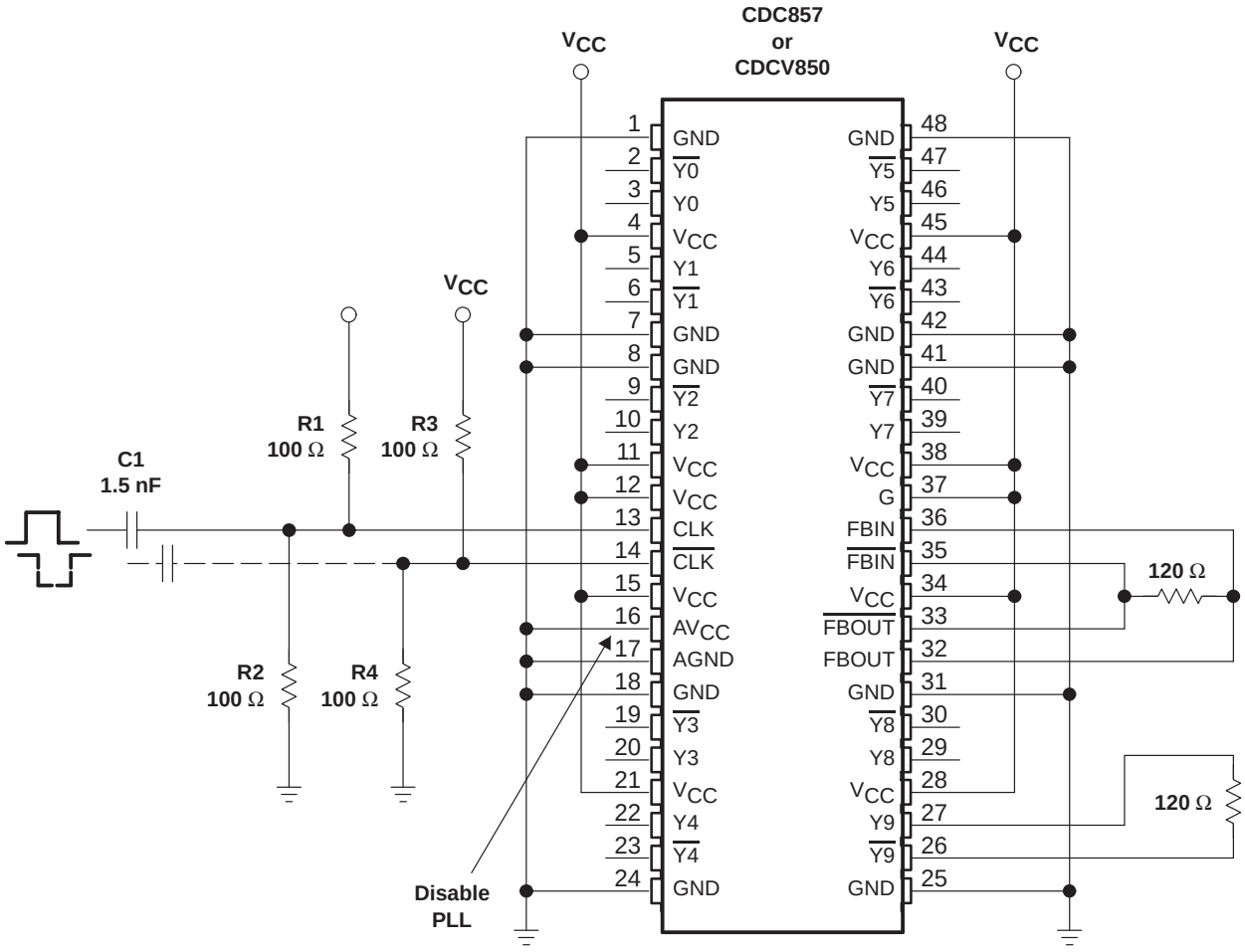


Figure 8. Test Setup for CDC857 and CDCV850

4.1 Peak-to-Peak Jitter—Evaluation Circuit 1

To extract the impact of the input circuitry from the overall performance of the DDR clock driver, the following test setup was used:

- Signal source: HP 8133A pulse generator (clock accuracy around 5 ps of jitter)
- Sampling scope CSA803A (20 GHz inputs at 50 Ω)
- The CDC857 and the CDCV850 were both mounted on the same experimental board (a 2-layer board made with a milling cutter. The expected RF performance is rather poor because of low assembling accuracy)

The tests were made on a PCB with a GND plane on the bottom layer and the device and all other components mounted on the top layer. The top area was optimized to house a V_{CC} plane to provide a fast capacitance with low lead inductance for the power rails. However, this PCB was manufactured on a milling machine having very limited capabilities; consequently, expected CDC performance is far below optimum. Therefore, the results to follow will permit comparisons between different design approaches but they will not yield absolute numbers. For the absolute ratings generated during the high-accuracy qualification process, refer to the data sheet.

4.1.1 Influence of AV_{CC} and V_{CC} Supply Stability

As shown in Figures 9 and 10, AVcc and Vcc both have strong influence on the overall clock jitter.

The stability of both the analog power rail and the power supply are crucial for good jitter performance. Adding two capacitors to the decoupling network of the test board improved the peak-to-peak jitter performance by about 10 ps.

Local noise on the power rail directly adds into the resultant signal. With the measurement setup used, a further performance improvement of around 10 ps was achieved by choosing the decoupling capacitors very carefully.

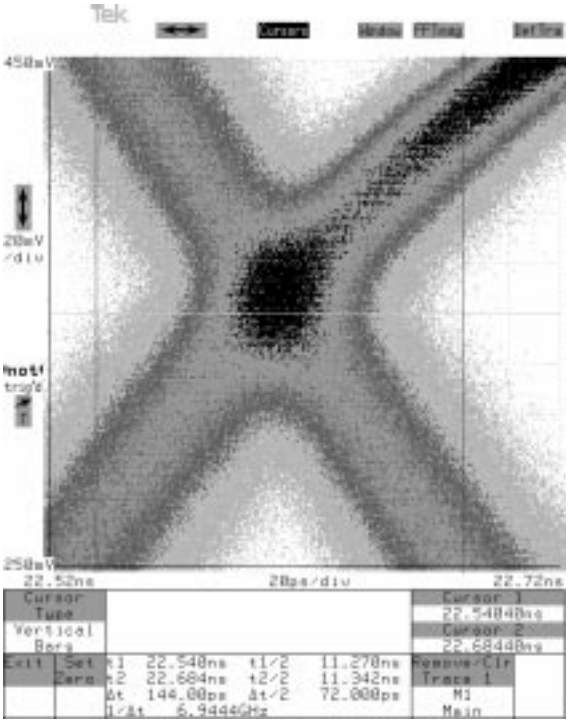


Figure 9. Input Clock at 100 MHz

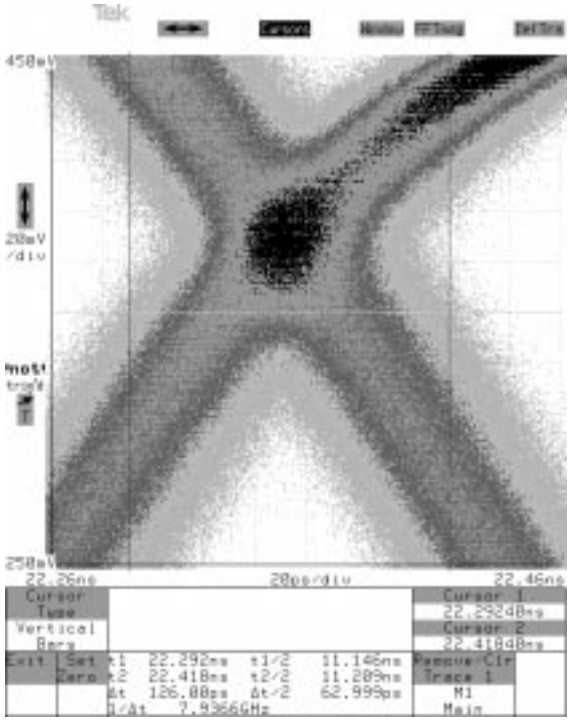


Figure 10. Input Clock at 100 MHz With Improved V_{CC} Supply and Optimized AV_{CC} Supply

4.1.2 Jitter vs Operation Frequency With Disabled PLL

Figures 11 and 12 show the results of jitter measurements with the PLL of the CDC857 and CDCV850 disabled. The jitter performance over the full frequency range for the two devices is summarized in Table 1.

Table 1. Jitter Performance Summary With Disabled PLL

	JITTER (ps) 100 MHz INPUT CLOCK	JITTER (ps) 166 MHz INPUT CLOCK
CDC857	24	16
CDCV850	18	16

Generally, it can be said that when a very accurate clock signal is used to feed the CDC857 or CCV850 input, the additional jitter added by the clock driver is very small and can be neglected. The amount of jitter is also independent of the clock frequency.

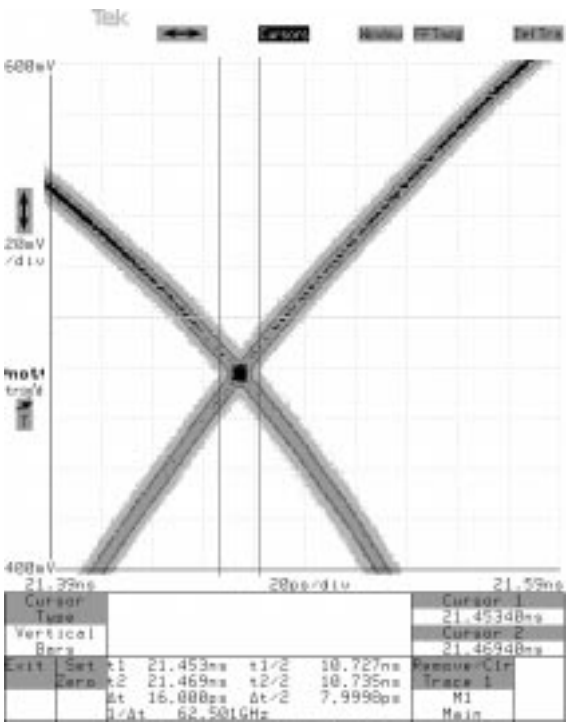


Figure 11. CDC857 With Input Clock at 166 MHz and PLL Disabled

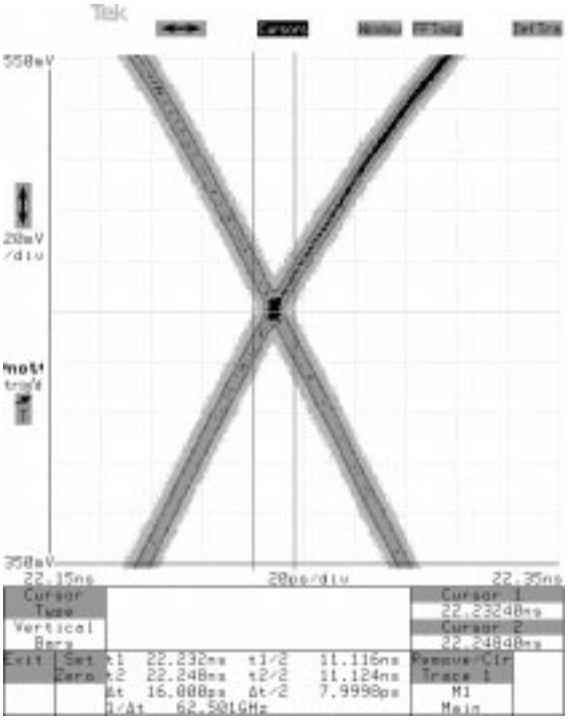


Figure 12. CDCV850 With Input Clock at 166 MHz and PLL Disabled

4.1.3 Jitter vs Operation Frequency (PLL Enabled)

The data collected in Figures 13–16 were taken to examine the effect of clock speed on jitter for the CDC857 and CDCV850 devices with single-ended input. As expected, and as summarized in Table 2, jitter decreases with increasing input clock frequency. This results from the higher update rate of the phase detector. Note that the experimental setup used for the figures and the table differed. The data in the figures were taken from a rather poor setup with a noisier clock; whereas, the tabulated values were made in a laboratory approved for jitter measurements.

Table 2. Jitter Performance Summary With Enabled PLL

	C-C/P-P JITTER (ps) 100 MHz INPUT CLOCK	C-C/P-P JITTER (ps) 166 MHz INPUT CLOCK
CDC857	126	66
CDCV850	108	40

CDC857 Because of board-layout issues, the peak-to-peak jitter of 126 ps observed at 100 MHz is higher than expected. In contrast, the peak-to-peak jitter of 66 ps observed at 166 MHz is below the 70 ps data sheet specification for this device. The test setup always showed a peak-to-peak jitter difference of approximately 60 ps between the operation frequencies of 100 MHz and 166 MHz.

CDCV850 The peak-to-peak jitter at 100 MHz was measured at around 108 ps, which is a little higher than expected because of the non-ideal board layout. At 166 MHz, the 40 ps peak-to-peak jitter achieved was excellent. For this device, the test setup always showed a peak-to-peak-jitter difference of approximately 70 ps between the operation frequencies of 100 MHz and 166 MHz.

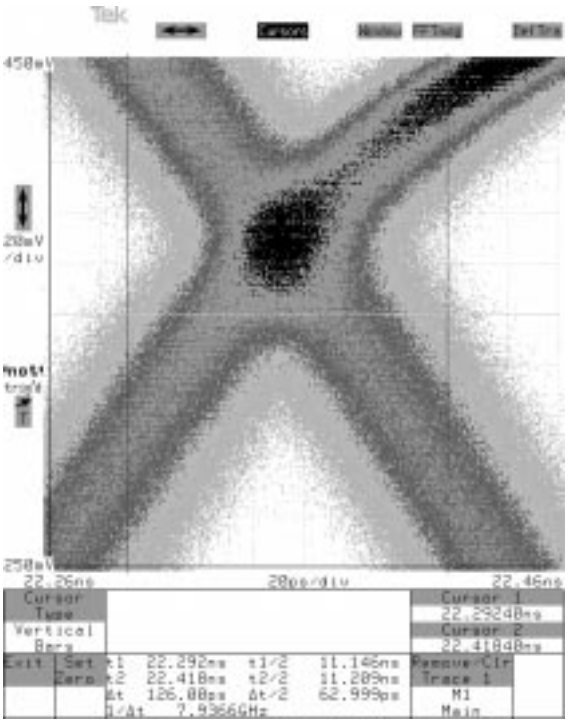


Figure 13. CDC857 With Input Clock at 100 MHz (Single-Ended Input)

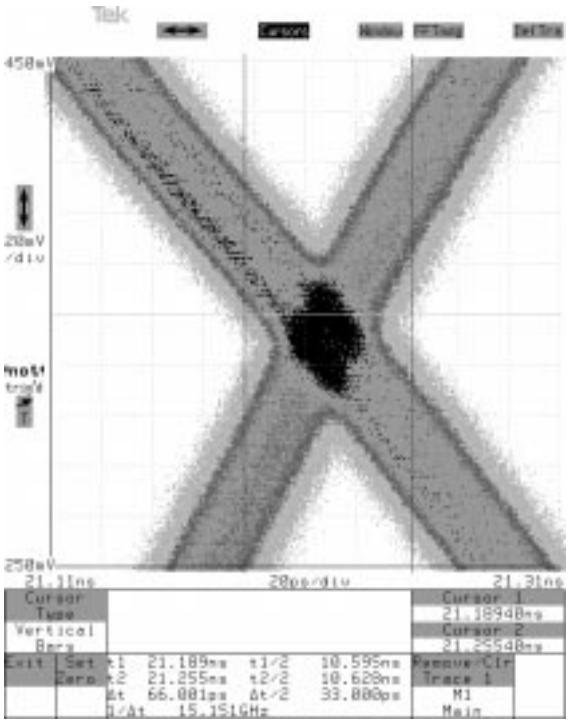


Figure 14. CDC857 With Input Clock at 166 MHz (Single-Ended Input)

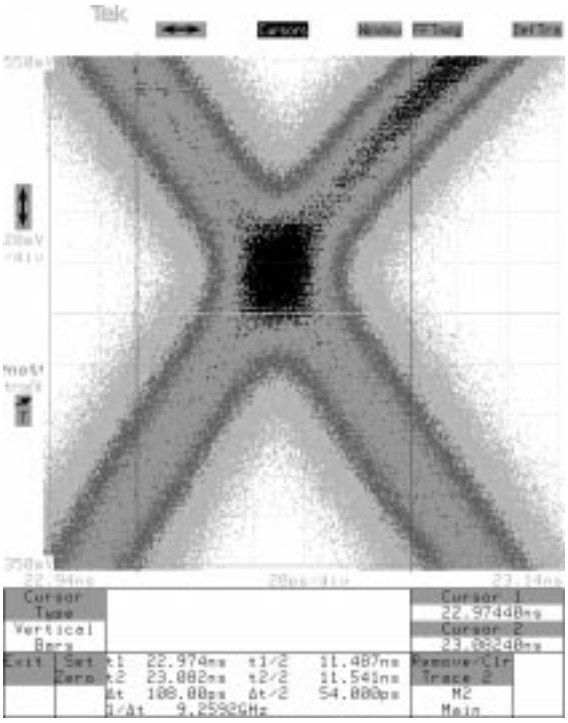


Figure 15. CDCV850 With Input Clock at 100 MHz (Single-Ended Input)

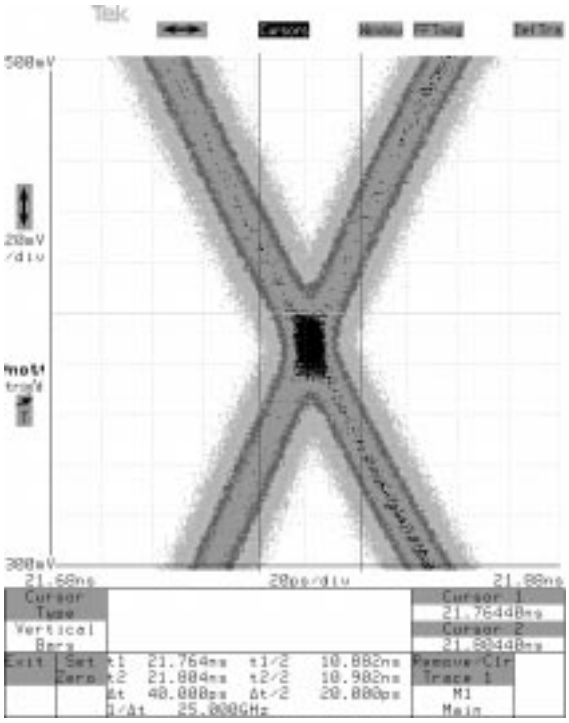


Figure 16. CDCV850 With Input Clock at 166 MHz (Single-Ended Input)

4.1.4 The Effect of Differential vs Single-Ended Input on Jitter

As discussed earlier, several errors can compound to reduce the performance of the CDC devices when a single-ended-input signal is applied. However, as can be seen in the Table 3, the results made with our test setup did not show any performance variation between the single-ended and the differential-input setups.

Table 3. Jitter Performance Summary: Single-Ended vs Differential Inputs (PLL Enabled)

	C-C/P-P JITTER (ps) For DIFFERENTIAL-INPUT CLOCK		C-C/P-P JITTER (ps) For SINGLE-ENDED-INPUT CLOCK	
	100 MHz	**166 MHz**	**100 MHz**	**166 MHz**
CDC857	126	60	126	66
CDCV850	114	47	108	40

CDC857 No performance difference in terms of peak-to-peak jitter was found between the single-ended-input and the differential-input setups.

CDCV850 Generally, the jitter in the single-ended setup using the CDCV850 was found to be better than with the CDC857 and as good as with a differential clock source. The explanation is the coupling capacitors that are already built into the CLK input circuit of the CDCV850. Thus, *the CDCV850 is an ideal candidate to convert single-ended into differential signals*

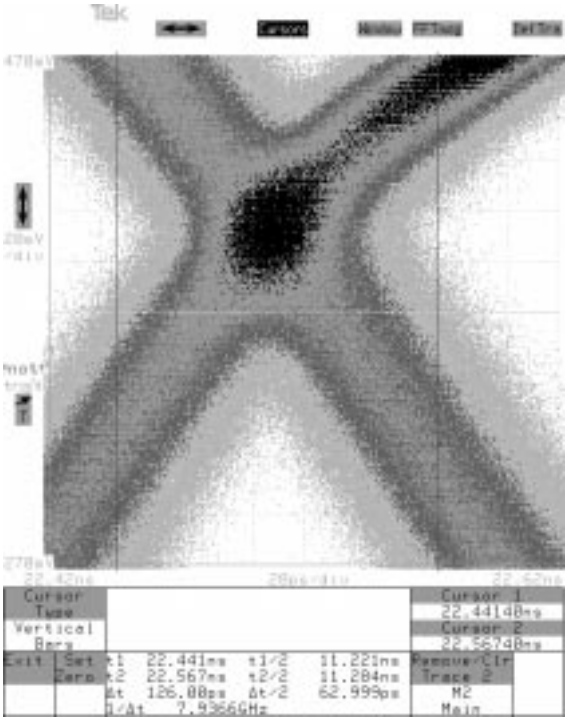


Figure 17. CDC857 With Differential Input Clock at 100 MHz (PLL Enabled)

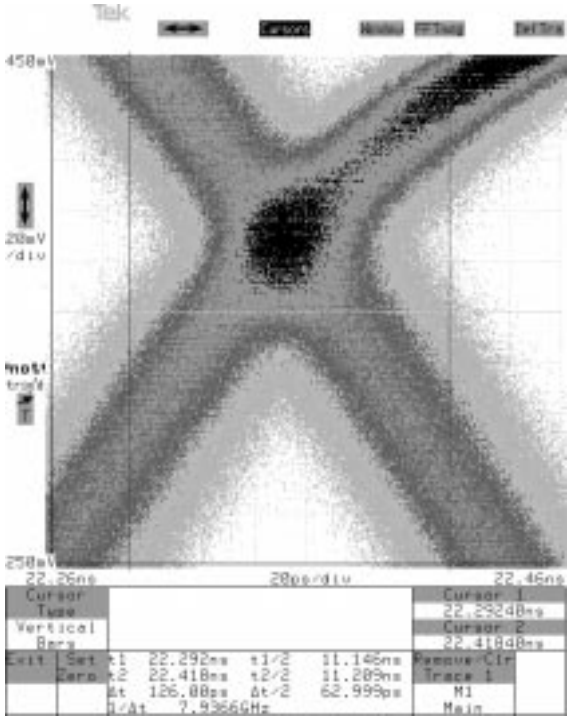


Figure 18. CDC857 With Single-Ended Input Clock at 100 MHz (PLL Enabled)

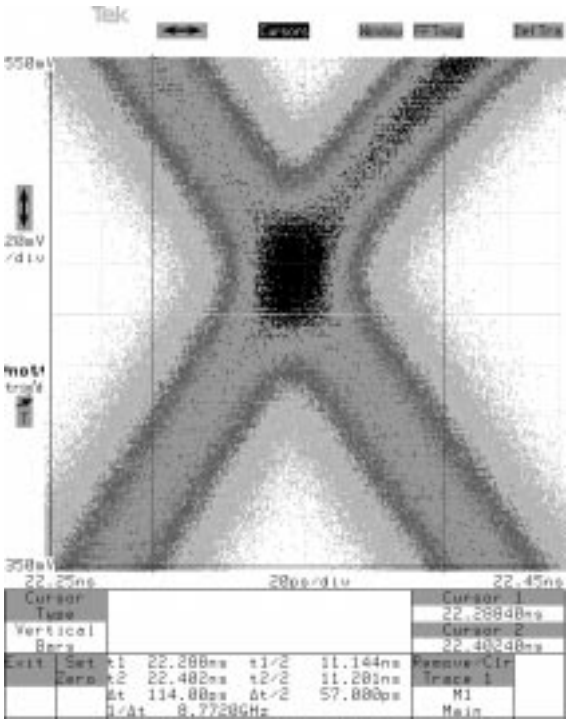


Figure 19. CDCV850 With Differential Input Clock at 100 MHz (PLL Enabled)

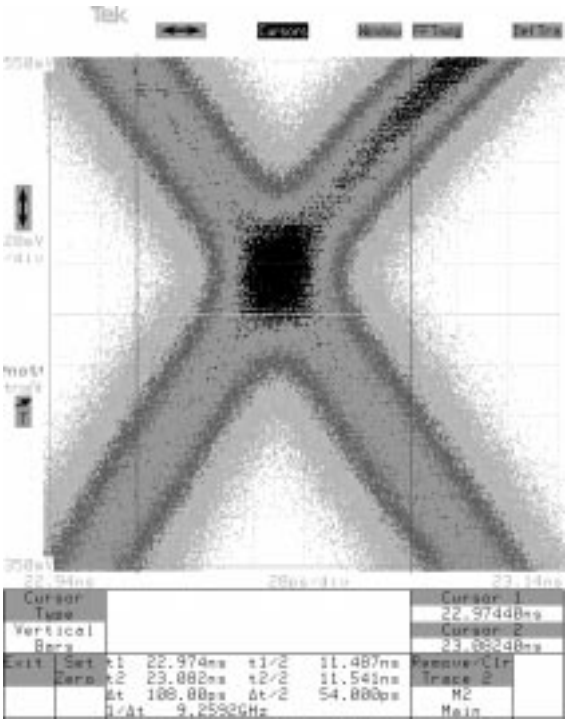


Figure 20. CDCV850 With Single-Ended Input Clock at 100 MHz (PLL Enabled)

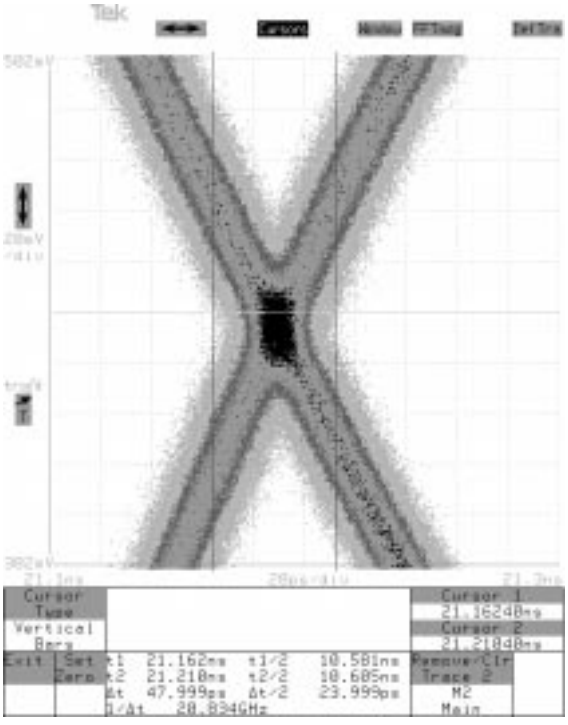


Figure 21. CDCV850 With Differential Input Clock at 166 MHz (PLL Enabled)

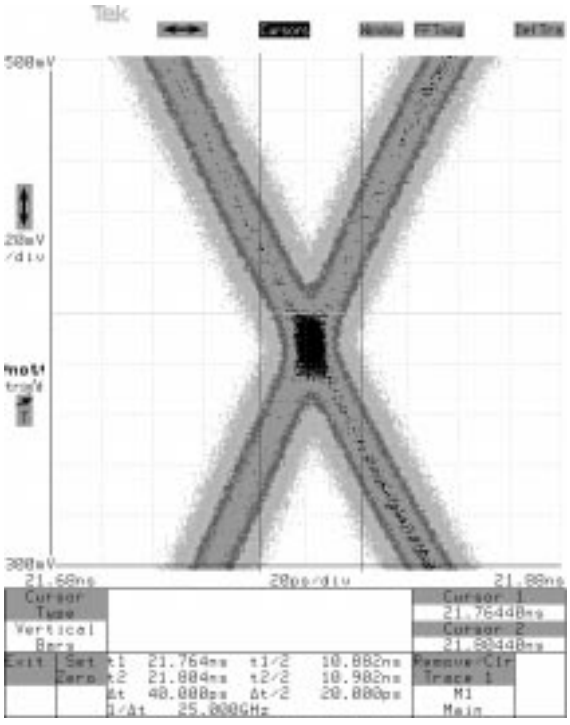


Figure 22. CDCV850 With Single-Ended Input Clock at 166 MHz (PLL Enabled)

4.2 Additional CDC857 Test Results—Evaluation Circuit 2

The measurements described here were made using a different evaluation module and different measurement equipment. The power supply voltage, V_{CC}, chosen for the CDC857 was 2.3 V which is the minimum voltage specified in the data sheet for this device, and the worse-case value within specifications. The following equipment and board were used:

- Signal source: HP 8110A pulse generator (rise-time adjustable)
- Digital oscilloscope: TDS794D (4G samples)
- 1 GHz differential probe
- The CDC857 was mounted on a simple, multifunctional one-layer board without a ground layer. Therefore, low device performance is to be expected. Nevertheless, in the soldering phase of building the board, care was taken to position adequate and fast buffer capacitors as closed to all power terminals as possible. Furthermore, special care was taken to keep line lengths as short as possible for the CLK/$\overline{\text{CLK}}$ and Y9/$\overline{\text{Y9}}$ terminals.

The test data reported in the following were taken to verify calculated and expected tendencies but they do not give absolute values. The numbers specified in the data sheet are much more precise and no doubt is cast upon them by any of the results seen during the current tests.

4.2.1 Buffered Mode—Using an Asymmetrical Clock Source (Duty Cycle ≠ 50%)

The data shown in Figure 23 were taken to show the effect of a not-fully-symmetrical high and low ratio of the input. As can be seen, the CDC857 operates just as a buffer when the PLL is disabled and it follows the high-low ratio of the input signal.

When using the CDC857 in buffered mode, an input signal with symmetric duty cycle could still cause the same problem. If the resistor network ahead of the CLK and $\overline{\text{CLK}}$ inputs is asymmetric, a dc offset will force the outputs to switch with an asymmetrical duty cycle.

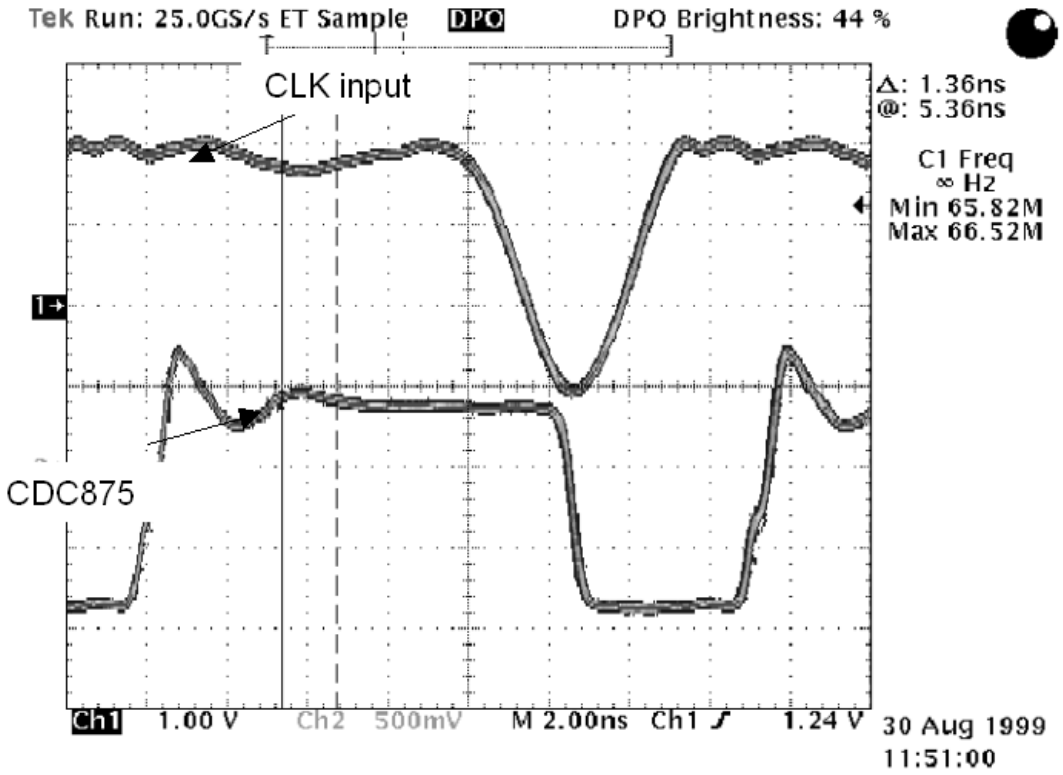


Figure 23. Input-Signal Duty Cycle Far Away From 50%

4.2.2 Effect When the Input Signal Has a Smaller Amplitude (Peak-to-Peak Voltage)

The data sheet for this device specifies that the minimum required voltage swing of the clock input signal is 0.7 V. Measurements taken during the current study confirmed that a much smaller swing will drive the CDC857 without problem. The only danger in using a single-ended clock signal is an unmatched dc level between the CLK/$\overline{\text{CLK}}$ terminals. Any dc offset across the CLK/$\overline{\text{CLK}}$ pins demands a larger swing of the input clock signal and adds to, or subtracts from, any duty cycle error. The data of Figure 24 were gathered with an input signal swing of less than 500 mV. The duty cycle error is easily seen in this figure. Another undesirable effect, namely higher jitter, was observed compared with the results from using a voltage swing of V_{CC} on the clock inputs. This error relates to the greater impact of incoupling noise.

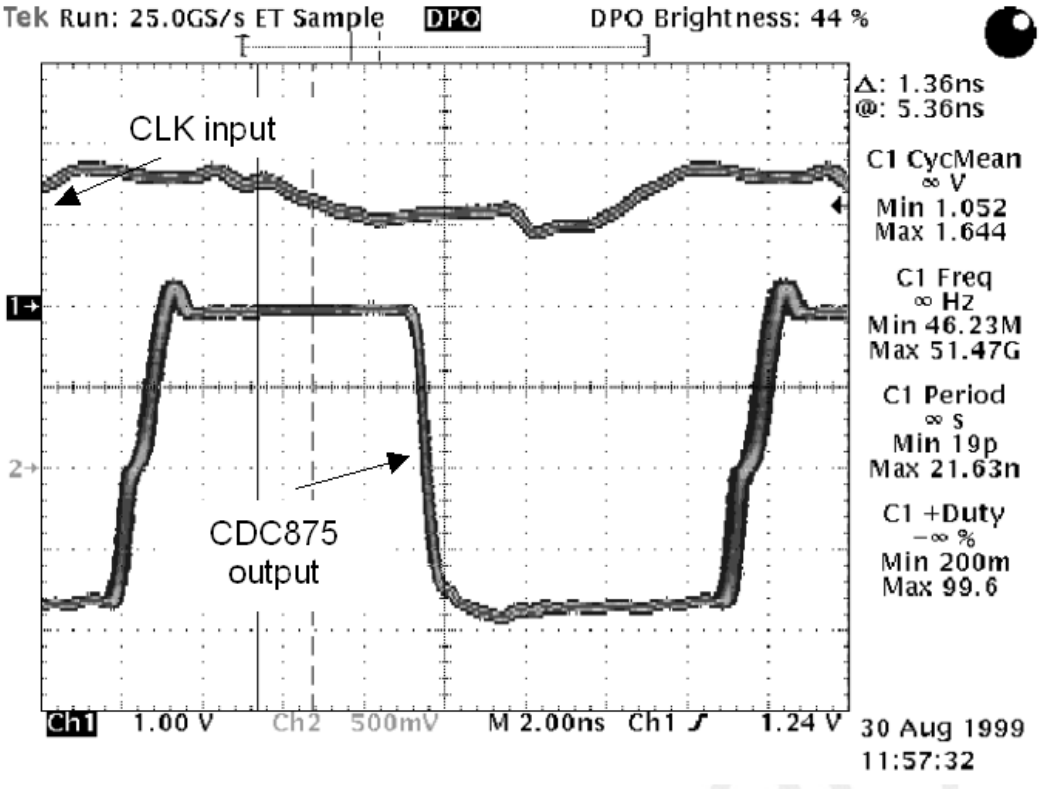


Figure 24. A Single-Ended Input Signal With Only 500 mV Driving the CLK Input of the CDC857

4.2.3 Jitter Performance Related to Rise Time of the Input Signal

Generally, the rise time of the reference clock signal will impact the overall jitter performance. The slower the input rise time is, the more influence have noise, drift and cross-point mismatches.

CDCV850 As can be seen in Table 4, the rise time did not have any effect on the CDCV850.

CDC857 The faster the clock transitions, the better will be the CDC857 output jitter. Figure 25 compares an input signal with a 2-ns (1.2 V/ns) rise time to an almost triangular input rise time 3.87 ns (0.6 V/ns).

Table 4. Jitter Performance With Variable Rise Time on CDCV850

	C-C/P-P JITTER (ps) 100 MHz INPUT CLOCK	C-C/P-P JITTER (ps) 166 MHz INPUT CLOCK
60 ps rise time	22/37	17/20
1 ns rise time	21/40	18/20

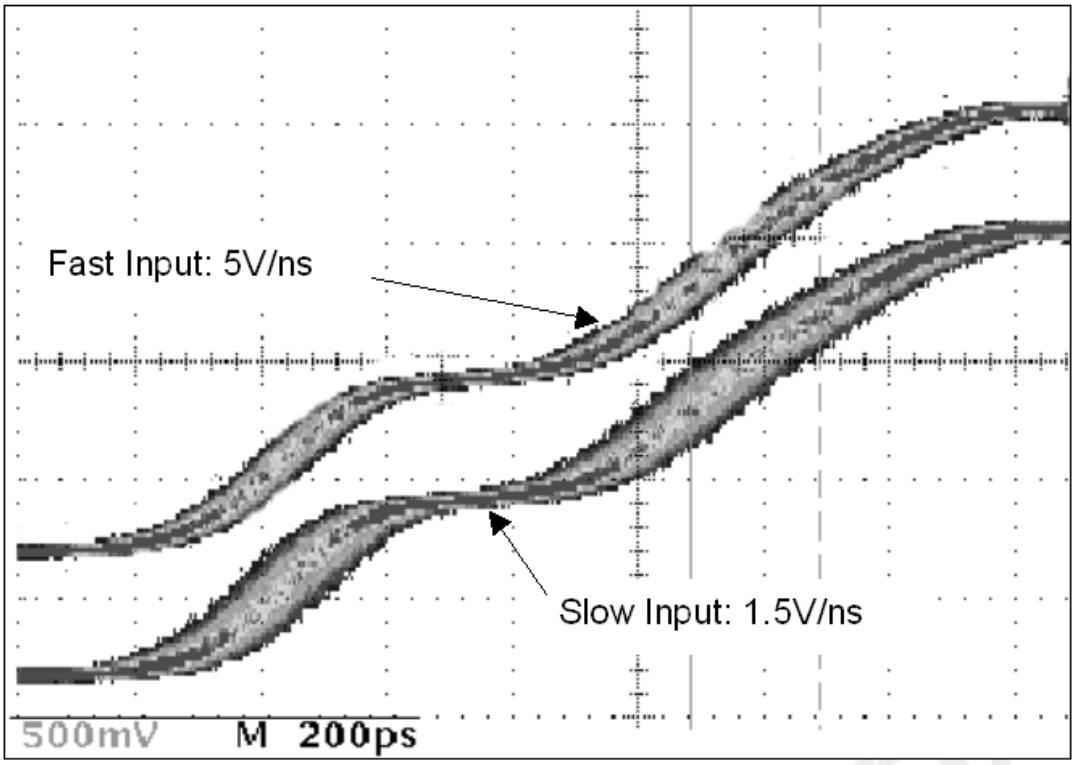


Figure 25. Jitter Performance Depends on the Input Edge-Rise Time. Both Signals Were Measured With an Infinite Persistence Over Several Seconds (>1G Consecutive Cycles)

4.2.4 Behavior of Nonterminated Outputs

The output behavior when not terminated into a 120-Ω resistor, but left open, is shown in Figure 26. The output jitter increases substantially.

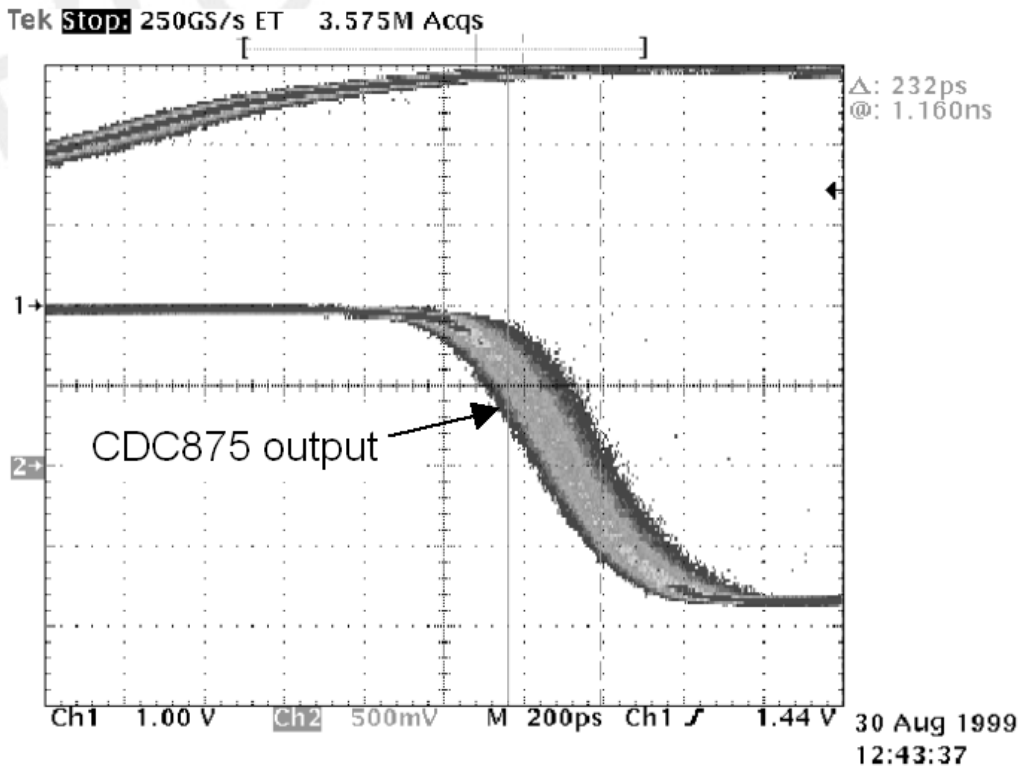


Figure 26. Observed, Nonterminated Output Signal With Input Clock at 100 MHz

4.2.5 Buffered Mode—Using the CDC for Frequencies Below Data Sheet Specifications

If the PLL circuit on the CDC857 is disabled (AV_{CC} tied to GND), the device will not have a minimum frequency. The only frequency limitation then comes from the clock-input circuitry. As discussed previously, the best way to drive the CDC857 with a single-ended signal is to couple this signal into one of the differential input clock pins, CLK/$\overline{\text{CLK}}$, using a coupling capacitor. This capacitor, together with the termination resistors $R_1||R_2$, forms a high-pass filter. The -3 dB cutoff frequency of the high-pass filter limits the lowest input frequency supported. A 1 MHz signal feeding the test circuit still forced the CDC857 to toggle its outputs (Figure 27). However, proper functionality could not be guaranteed with this setup because the input did not meet the 0.35-V critical minimum voltage swing for a defined high or low input level.

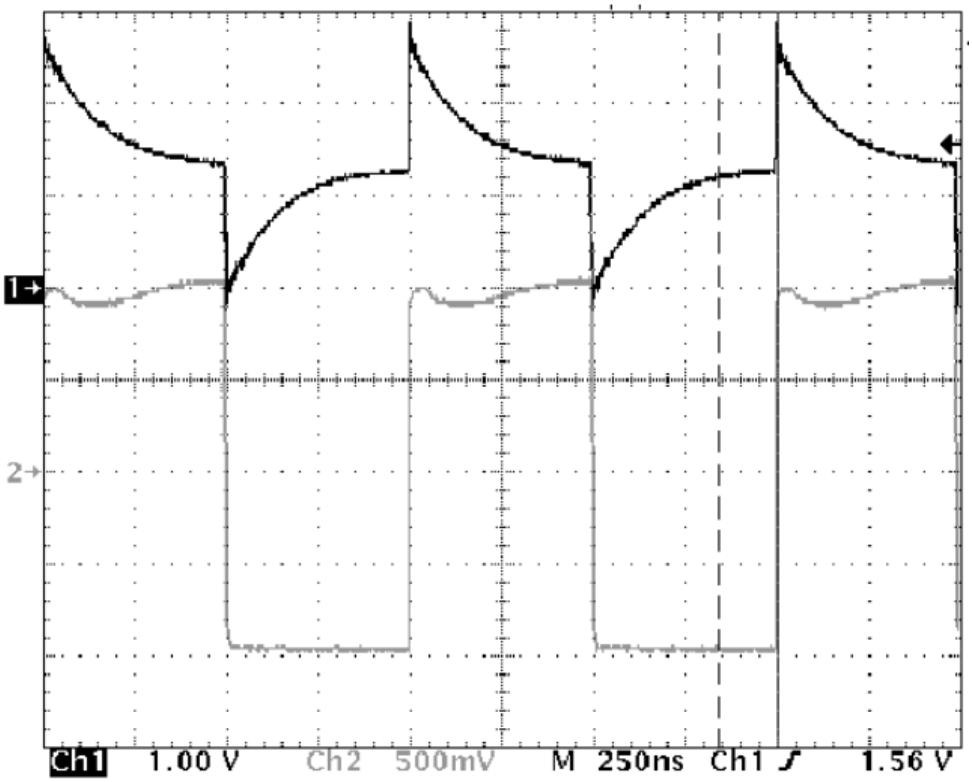


Figure 27. A Very Slow Input Signal Driving the CDC857

5 Summary

The CDC857 and CDCV850 clock drivers are good choices for converting a single-ended line signal into a differential-clock signal. If the CDC delay is unimportant, the buffered mode with the PLL disabled is preferred. The CDCV850 already has a high-pass input filter built, in series, into the CLK-input rail. Using the CDC857, a very simple resistor network can be used to offset the clock input signal, and allow a single-ended input to drive the differential-input stage. The lower the impedance of this resistor network, the higher the noise immunity. However, within the guidelines discussed in this report, even a higher-impedance network will work properly and reduce current drain to the application.

In terms of jitter, the signal quality of the CDC output is very high, and is only related to that of the single-ended input signal. The signal swing of the outputs is not a function of the input signal and, therefore, the results of the measurements are very promising.

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