Application Note

Analysis and solution of restart problem after SN74ACT244 inverter relay drive power-off

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ABSTRACT

This document was translated from a simplified Chinese source. (ZHCAG55)

SN74ACT244 is an 8-channel 3-state buffer/driver. Thanks to wide voltage (4.5V-5.5V), high speed transmission (propagation delay 5-10ns), strong drive capability of ±24mA, and industrial temperature width of -45℃ to 125℃, it has become a common supporting material for inverter. Its applications in inverters focus on three core scenarios: first, serving as a signal buffer between the MCU/FPGA and power device drive circuits to enhance control signal drive capability and prevent signal attenuation and distortion during long-distance transmission. Second, enabling TTL-to-CMOS level conversion to resolve interface compatibility issues between devices operating in different voltage domains within the inverter, ensuring reliable transmission of control commands. The chip's compact size (available in multiple packages, with the smallest VQFN package measuring just 11.25mm²) simplifies inverter PCB design while reducing circuit complexity and cost.

This paper mainly studies the SN74ACT244 in the inverter drive relay scenario, the power-off relay restart analysis idea, and two solutions in practical application.

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1 Introduction of the application scenario

In inverter applications, relays typically serve 3 core functions centered around safe startup, fault protection, and mode switching.

1. Pre-charging and soft start: When powering up the motor drive inverter, the relay works with the current-limiting resistor to slowly charge the DC bus capacitor. This prevents massive surge currents from instantaneous capacitor short circuits, which could damage the IGBT and power supply. Once the capacitor voltage stabilizes, the relay closes to short the capacitor, allowing the drive circuit to enter normal operation.
2. Main circuit switching control: Acting as the “master switch” for the motor drive's main circuit, it connects DC bus to the inverter power units during system startup. When the motor stops or enters standby mode, it disconnects the main circuit, physically isolating the power units from the high-voltage power supply. This reduces static power consumption and enhances circuit safety.
3. Fault emergency cut-off: When the drive system detects fatal faults such as overcurrent, overvoltage, motor stall, IGBT overtemperature, relays immediately disconnect the main circuit or cut off the drive signal path, quickly isolating the source of the fault, to prevent the failure from extending damage to the core components such as the motor, inverter power module, and so on.

In real-world applications, the voltage supplied by the relay is usually much higher than the voltage of the MCU control signal, and the ground of the transformer is not common with the control ground of MCU, so it is common to use optocouplers to achieve functional insulation. Additionally, since the MCU is typically located on the control board while the optocoupler and relay reside on the power board at a considerable distance, the drive signal is susceptible to interference. Therefore, as shown in Figure 1-1, SN74ACT244 is employed to buffer the 3.3V output signal from P55 to 5V. This enhances drive capability while elevating the drive level, thereby improving immunity to interference. This represents a typical application of the SN74ACT244 with relays in the inverter as described in this document.

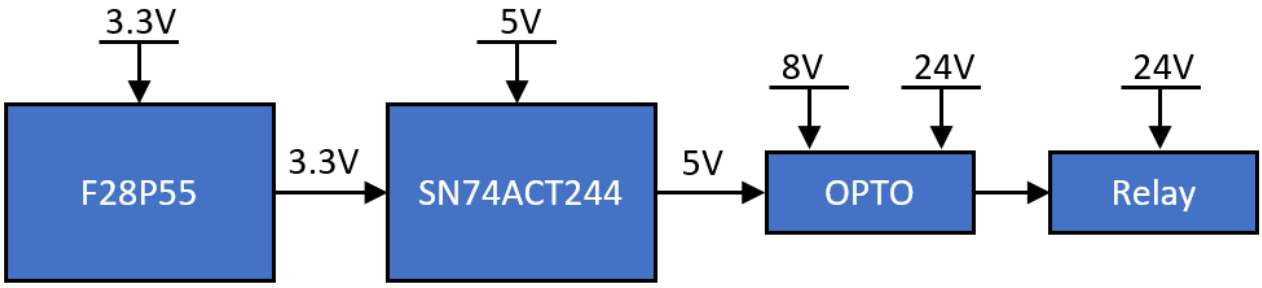

Figure 1-1. Typical block diagram of the inverter SN74ACT244 relay drive

2 Test and cause analysis of abnormal power-off phenomenon

In the process of production line discharge, the inverter needs to be tested at the factory by power-up and power-off. At the time of power-off, the worker may hear some inverters emit a relay engagement shutdown sound, which should not occur. After positioning the relay through sound, during the power-off process, the abnormal relay drive waveform is captured, as shown in Figure 2-1, while the abnormal relay drive waveform is captured, as shown in Figure 2-2.

By comparing Figure 2-1 with Figure 2-2, it shows that when the normal SN74ACT244 loses power, the input 3.3V and 5V levels will gradually decay to 0V; however, when the abnormal relay loses power and the INPUT drops to about 0.4V, SN74ACT244 outputs a 0V low level for 100ms.

Figure 2-1. SN74ACT244 abnormal relay drive waveform

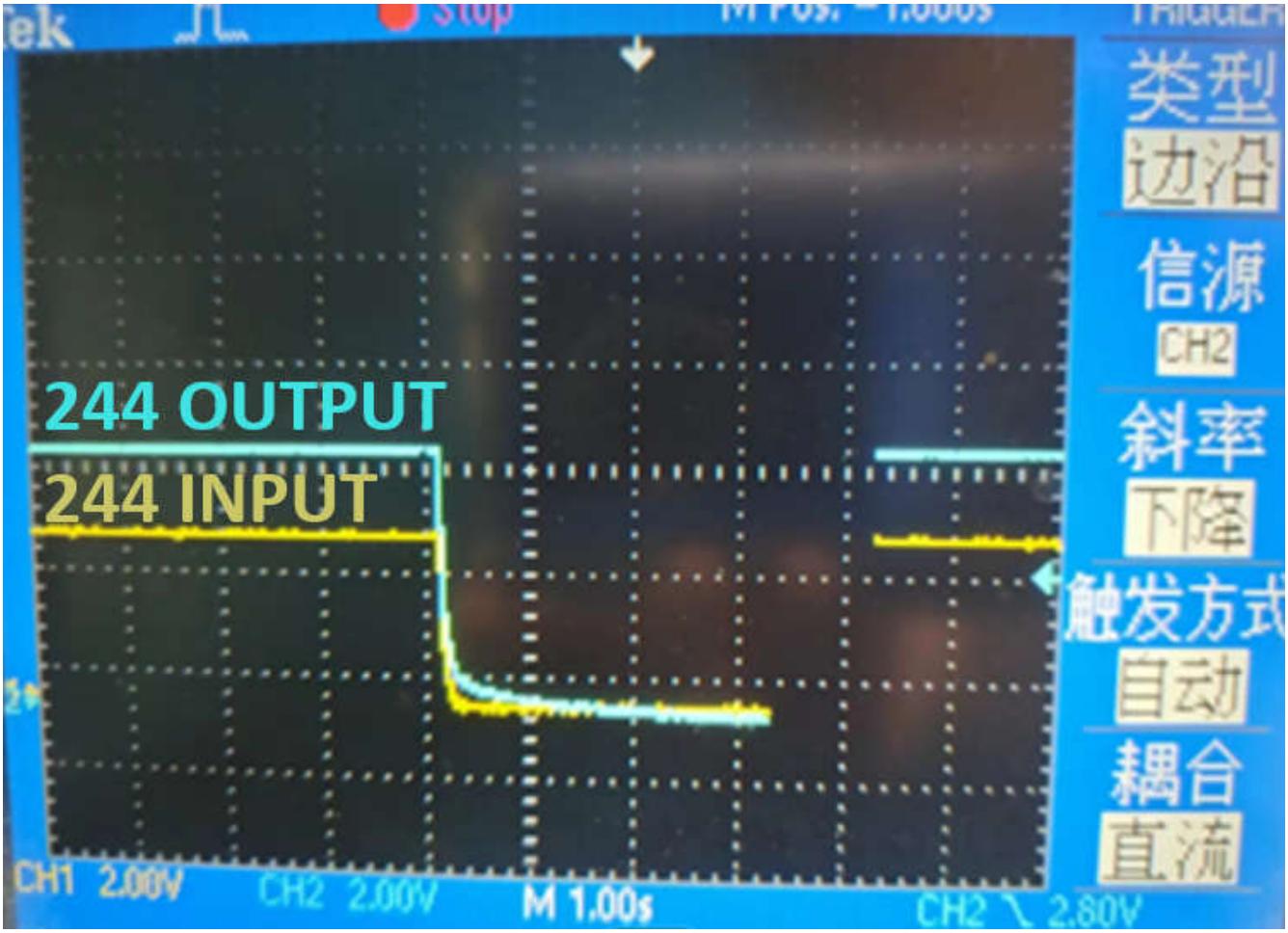

Figure 2-2. SN74ACT244 normal relay drive waveform

Combined with Figure 2-3 the power supply block diagram and Figure 2-1 abnormal power-off waveform, it shows that during abnormal power-off, 100ms low level output from SN74ACT244 causes the optocoupler output to trigger, activating the downstream relay. This behavior is unacceptable in customer applications and may lead end-users to question the reliability of the inverter's operation.

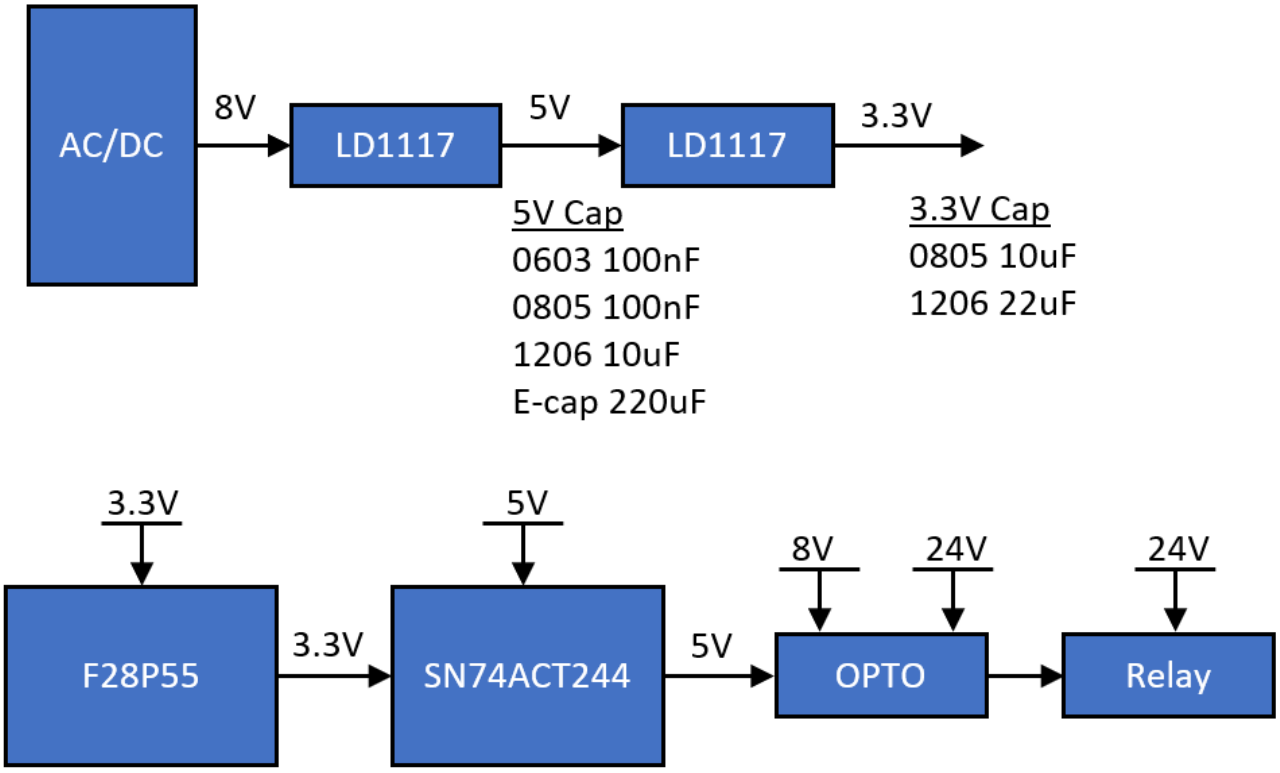

Figure 2-3. Typical block diagram for inverter relay drive

Based on the specifications for V_{IL} and V_{IH} and the reference values shown in Figure 2-5 [1], when V_I is less than 0.8V, the chip outputs a low level; when V_I is more than 2V, the chip outputs a high level. Typical values of V_{IL} at different supply voltages are not specified, in this case:

- For a normal chip, when the supply voltage drops from 5V to about 2V, the chip V_{IL} is shown as Figure 2-4 normal power-off logic. When V_{IL} is lower than INPUT voltage, it does not trigger the low output of OUTPUT.
- For an abnormal chip, when the supply voltage drops from 5V to about 2V, the chip V_{IL} is shown as Figure 2-4 abnormal power-off logic, and V_{IL} is higher than INPUT voltage. When the INPUT drops to V_{IL}, it will trigger the OUTPUT low output in the figure below, resulting in abnormal relay action.

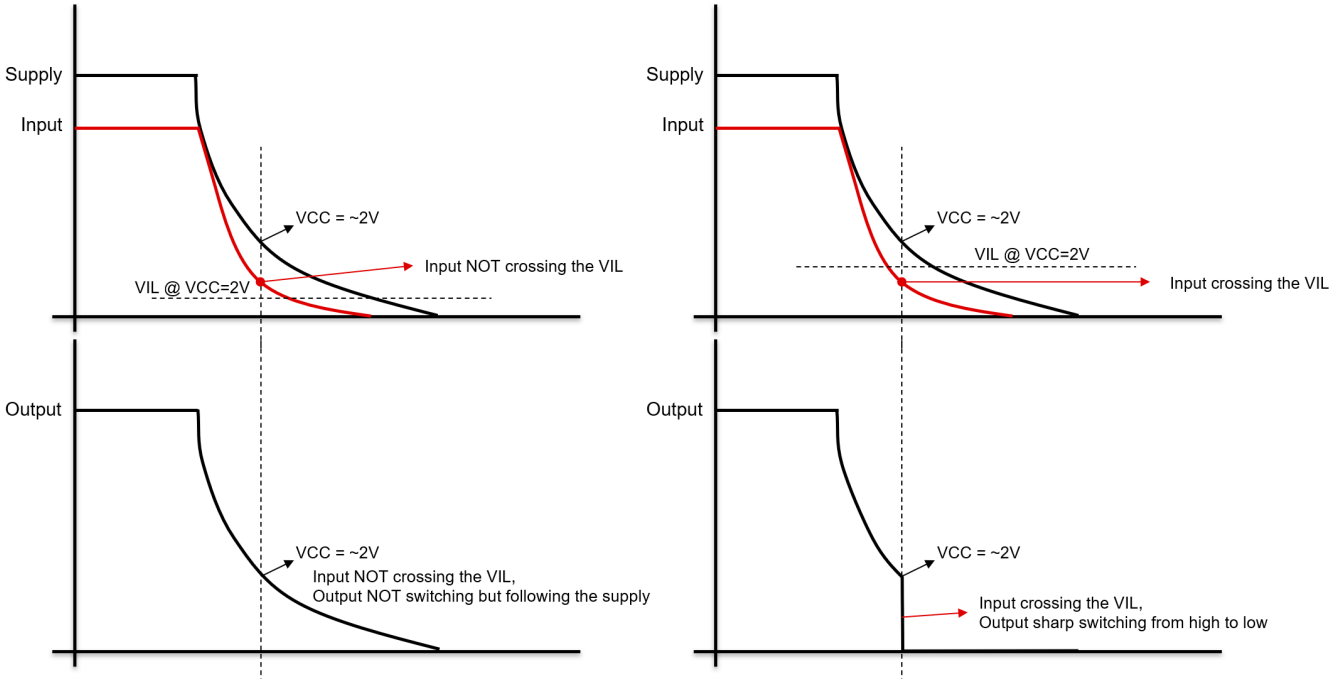

Figure 2-4. Normal vs abnormal power-off logic

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V

Figure 2-5. SN74ACT244 specifications

Once confirming with the product line, the chip factory and process upgrades can cause variations in V_{IL}, but all variations meet V_{ILmax}=0.8V parameter mentioned in specifications. In order to avoid this problem, we can only allow INPUT voltage to be greater than V_{IL} at any point in power-off.

3 Peripheral circuit modification methods and experiments

As analyzed above, in order to ensure that the INPUT voltage is greater than V_{IL} when power is lost and V_{IL} will decrease as V_{cc}decreases, we need to make 3.3V voltage of INPUT drop down as slow as possible, and 5V voltage of V_{cc} drop down as fast as possible. The simplest way is to increase 3.3V load capacitance and reduce 5V load capacitance, as shown in Figure 2-3. 5V capacitance is 220uF+10uF+0.1uF+0.1uF and 3.3V capacitance is 10uF+22uF. Actual test steps and waveforms in the final method 1 are described as follows:

Method 1: Adjust the power-off speed by increasing or decreasing capacitance

1. Remove 220uV E-cap on 5V

   5V power-off is faster. SN74ACT244 OUTPUT low level time is reduced from 100ms to 40ms, which it is effective but still outputs low level, causing abnormal relay action.

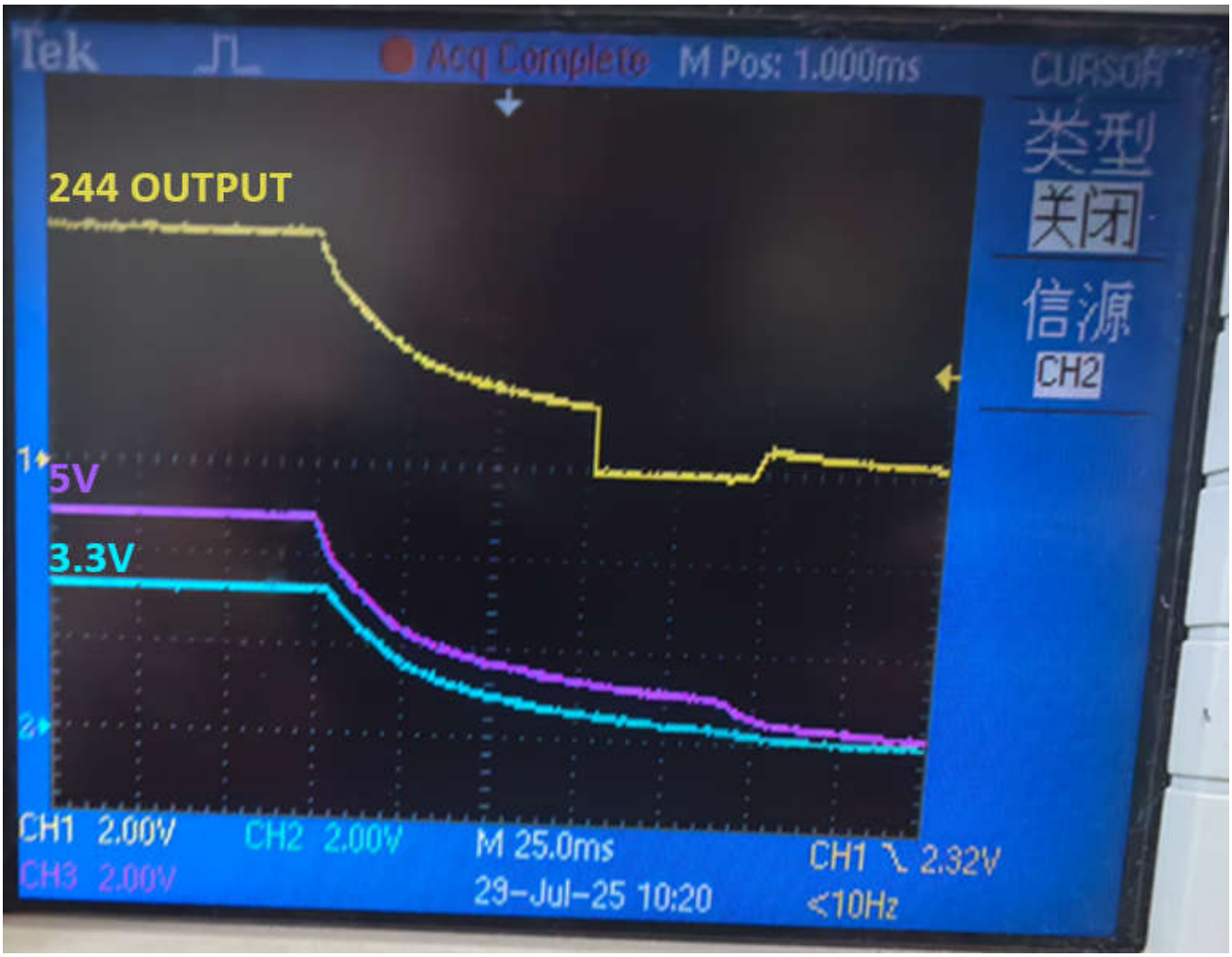

Figure 3-1. Remove 220uV E-cap power-off waveform

2. Add 10uF to 22uF on 3.3V

   Without modifying PCB, constrained by the capacity of 1206 capacitors, 3.3V capacitor could only be increased from 10uF to 22uF. SN74ACT244 output low level time further shortens from 40ms to 25ms. This also had an effect but did not resolve the issue.

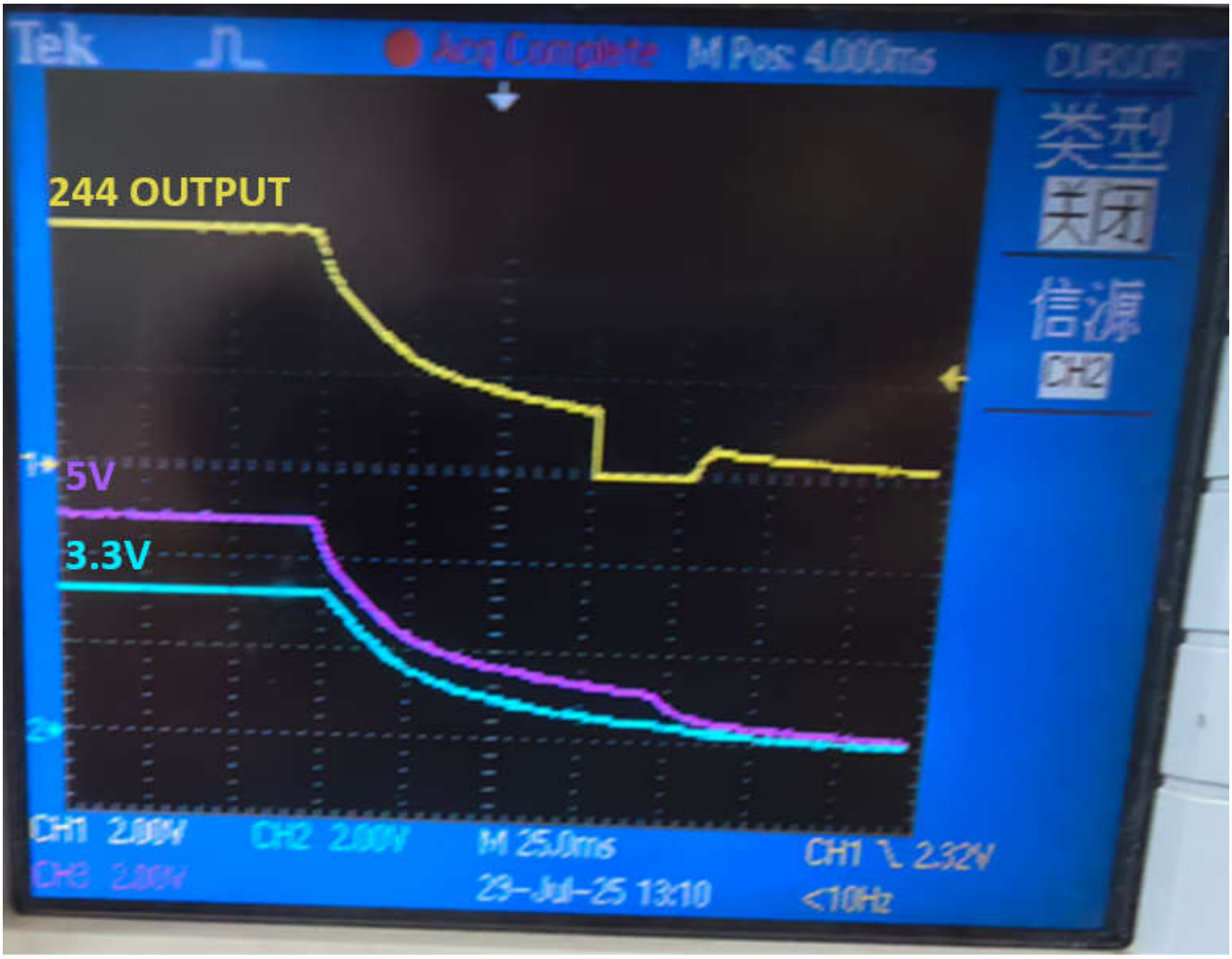

Figure 3-2. Add 22uF 1206 capacitor power-off waveform

3. Add 220uF E-cap on 3.3V

To validate the preceding analysis and proposed method, we soldered a 220uF E-cap via wire-bond to the 3.3V line. This resolved the issue, but due to PCB space constraints, this approach is impractical in this specific case.

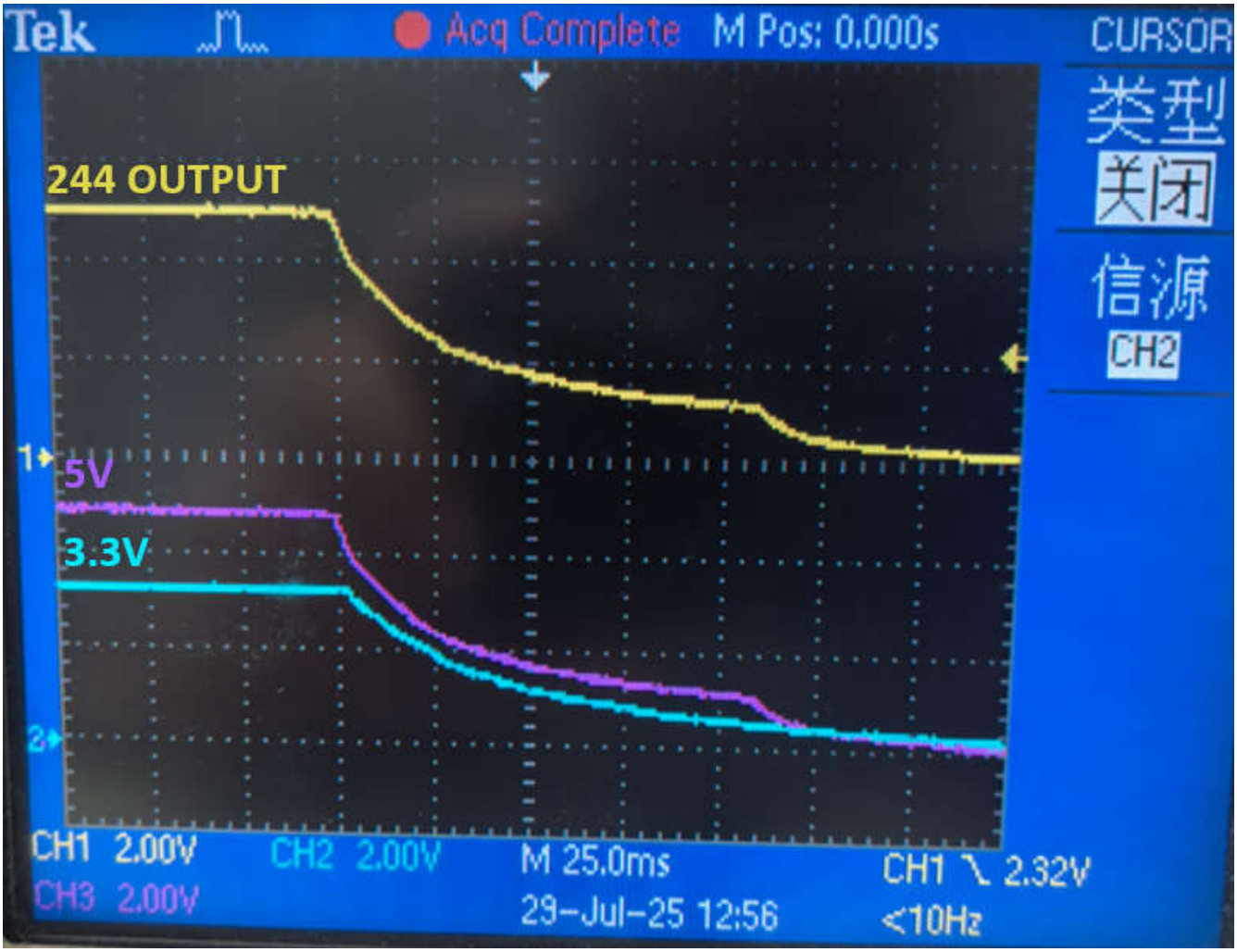

Figure 3-3. Add 220uF E-cap power-off waveform

Currently, 5V capacitor has been reduced to the minimum value required for LDO operation, and 3.3V capacitor has been increased to the maximum value allowed for 1206 package. Therefore, in this case, constrained by PCB size and reserved capacitor packages, modifying the dropout time by adjusting capacitors cannot resolve the issue. Therefore, we propose Method 2: without modifying the PCB, we discovered that upgrading a key parameter of P2P LDO can also resolve this issue.

Method 2: Make 3.3V slower to power off by implementing LDO with smaller V_{DO}

It can be seen from the abnormal waveform that Figure 3-1 if the distance Figure 3-2 between 5V and 3.3V voltage waveforms is reduced when the power is lost, this indirectly slows the rate of 3.3V voltage drop. This approach also achieves the goal of maintaining INPUT greater than V_{IL} during the power-off process. The comparison shows that LD1117 V_{DO} currently used by customers is 1.1V [2] , while V_{DO} of TI's latest generation 3.3V/1A/P2P SOT223 TLV76133DCYR is 0.9V [3] .

The measured waveforms are shown in Figure 3-4.With the replacement of the smaller V_{DO} LDO TLV76133DCYR, as 5V drops close to 3.3V, the load is small and V_{DO} is much less than 0.9V. 5V and 3.3V start to lose power almost simultaneously. The smaller voltage gap also indirectly slows 3.3V drop relative to 5V, ultimately resolving the abnormal output issue.

Figure 3-4. TLV76133DCYR power-off waveform

4 Summary

This paper describes the application scenarios of relays in inverter and the commonly used SN74ACT244 for relay driving. It details the power architecture of inverter and the block diagram of SN74ACT244 optocoupler driving a relay. The paper analyzes a relay restart issue encountered by a customer and proposes two feasible solutions: increasing or decreasing the capacitance to modify the power-off speed, and when PCB modifications are constrained, indirectly slow the power-off speed by reducing V_{DO} voltage of LDO. Both proposed methods were validated through practical testing, with experimental waveforms consistent with theoretical analysis, providing debugging insights for subsequent designers.

5 References

1. SN74ACT244 Datasheet. SNx4ACT244 Octal Buffers and Drivers With 3-State Outputs datasheet (Rev. G)
2. LD1117 Datasheet. LD1117.fm
3. TLV761 Datasheet. TLV761 18V, 1A, Fixed-Output Linear Voltage Regulator datasheet (Rev. D)

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