

SN54LVT574, SN74LVT574

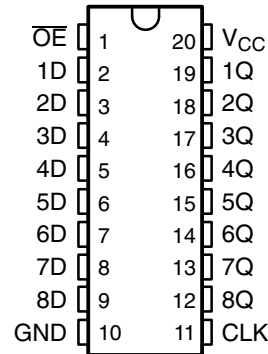
3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

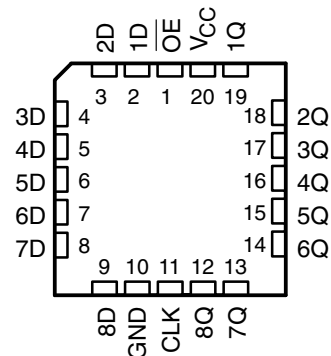
SCBS139D – MAY 1992 – REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVT574 . . . J OR W PACKAGE
SN74LVT574 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT574 . . . FK PACKAGE
(TOP VIEW)



description

These octal flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVT574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT574 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT574 is characterized for operation from -40°C to 85°C .



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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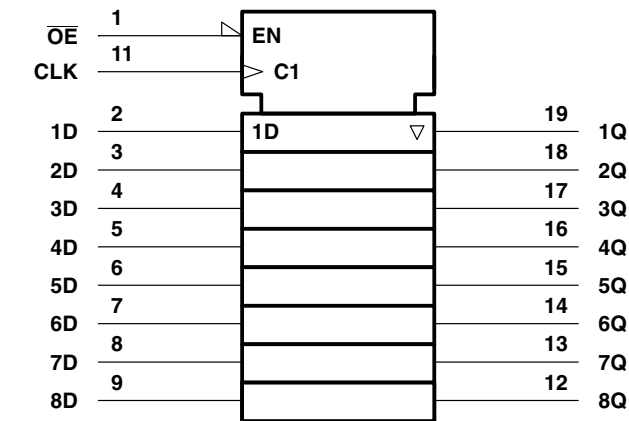
SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each flip-flop)

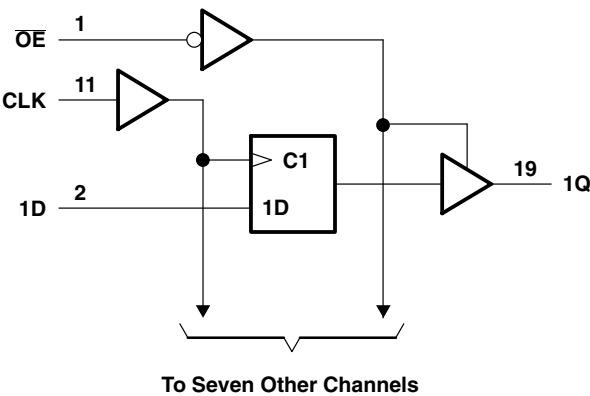
INPUTS			OUTPUT Q
OE	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT574	96 mA
SN74LVT574	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT574	48 mA
SN74LVT574	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^{\circ}\text{C}$ (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 4)

			SN54LVT574		SN74LVT574		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
V _I	Input voltage			5.5		5.5	V
I _{OH}	High-level output current			–24		–32	mA
I _{OL}	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT574		SN74LVT574		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}	V _{CC} = 2.7 V, I _I = −18 mA			−1.2		−1.2		V
V _{OH}	V _{CC} = MIN to MAX‡, I _{OH} = −100 μA			V _{CC} −0.2		V _{CC} −0.2		V
	V _{CC} = 2.7 V, I _{OH} = − 8 mA			2.4		2.4		
	V _{CC} = 3 V	I _{OH} = − 24 mA		2				
		I _{OH} = −32 mA				2		
V _{OL}	V _{CC} = 2.7 V	I _{OL} = 100 μA		0.2		0.2		V
		I _{OL} = 24 mA		0.5		0.5		
	V _{CC} = 3 V	I _{OL} = 16 mA		0.4		0.4		
		I _{OL} = 32 mA		0.5		0.5		
		I _{OL} = 48 mA		0.55				
		I _{OL} = 64 mA				0.55		
I _I	V _{CC} = 0 or MAX‡, V _I = 5.5 V			50		10		μA
	V _{CC} = 3.6 V	V _I = V _{CC} or GND	Control inputs	±1		±1		
		V _I = V _{CC}	Data inputs	1		1		
		V _I = 0		−5		−5		
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100		μA
I _{I(hold)}	V _{CC} = 3 V	V _I = 0.8 V	Data inputs	75		75		μA
		V _I = 2 V		−75		−75		
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V			1		1		μA
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V			−1		−1		μA
I _{CC}	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high	0.13	0.39	0.13	0.19	mA
			Outputs low	8.7	14	8.7	12	
			Outputs disabled	0.13	0.39	0.13	0.19	
ΔI _{CC} §	V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND			0.3		0.2		mA
C _i	V _I = 3 V or 0			4		4		pF
C _o	V _O = 3 V or 0			8		8		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVT574				SN74LVT574				UNIT
		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	150	0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	2		2.4		2		2.4		ns
t _h	Hold time, data after CLK↑	0.9		0.9		0.3		0		ns



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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT574				SN74LVT574				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f _{max}			150		150		150		150		MHz	
t _{PLH}	CLK	Q	1	5.9		6.6	1.7	3.6	5.4		6.2	ns
t _{PHL}			1	6.1		6.8	2.4	4.3	5.9		6.6	
t _{PZH}	OE	Q	0.5	5.9		7.1	1	2.9	4.8		5.9	ns
t _{PZL}			0.5	5.3		6.4	1.3	3.4	5.1		6.2	
t _{PHZ}	OE	Q	0.7	5.9		6.6	1.9	4	5.5		5.9	ns
t _{PLZ}			0.5	5.1		5.1	1.7	3.2	4.5		4.5	

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

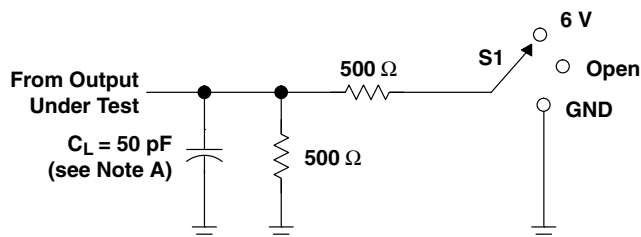
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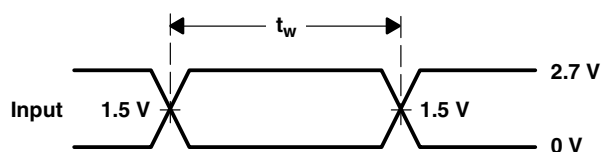
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PARAMETER MEASUREMENT INFORMATION

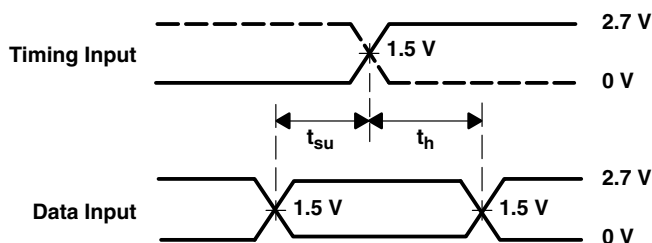


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

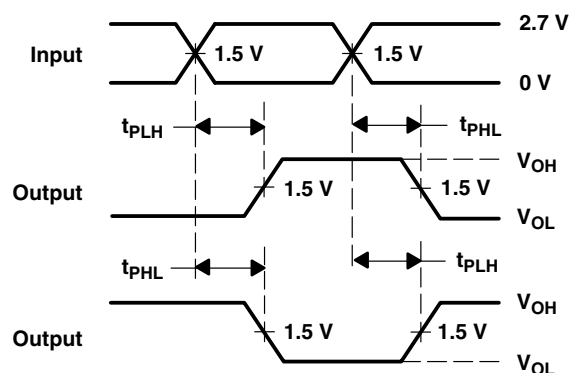
LOAD CIRCUIT FOR OUTPUTS



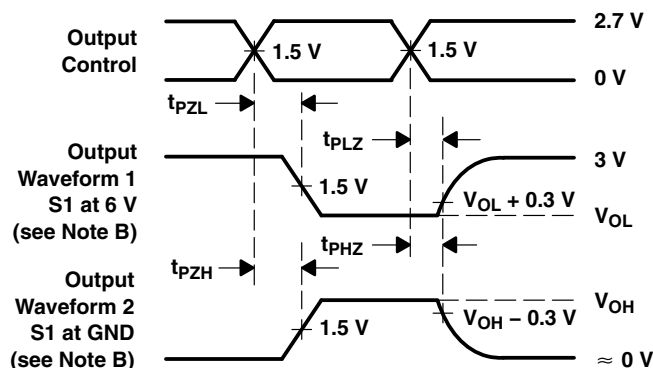
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVT574DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT574
SN74LVT574DW.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT574
SN74LVT574DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT574
SN74LVT574DWR.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT574
SN74LVT574PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX574
SN74LVT574PWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX574

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

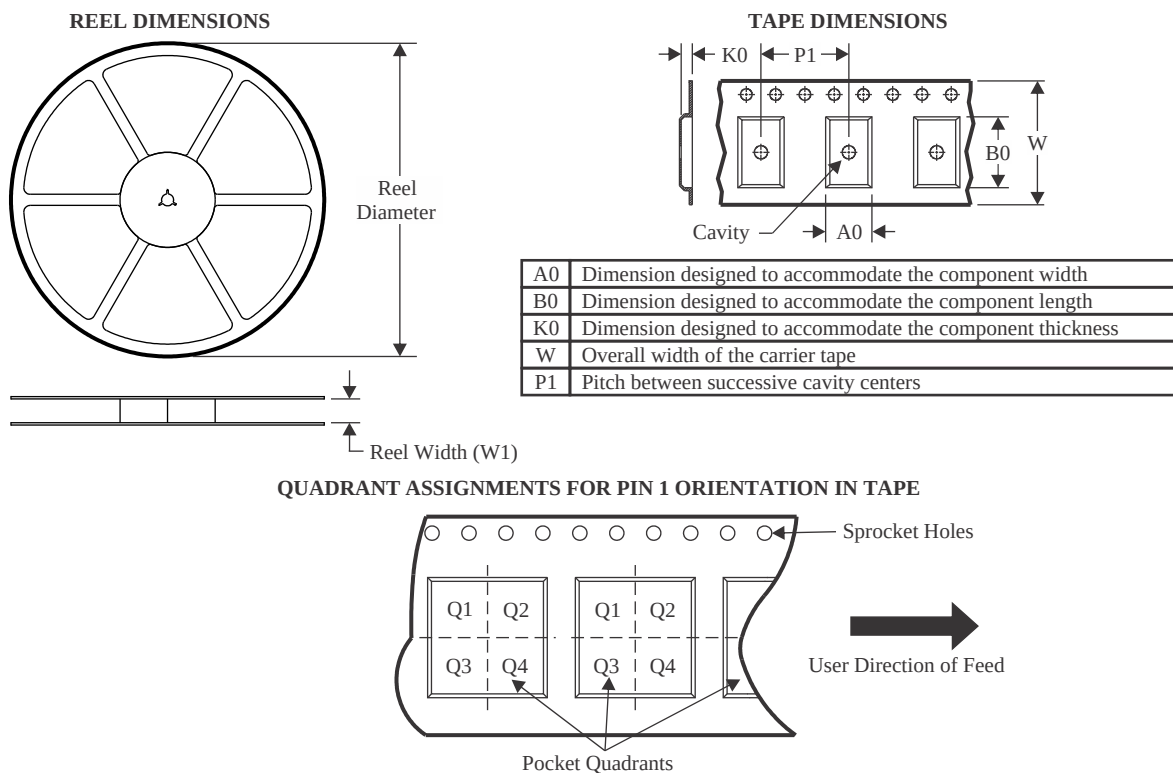
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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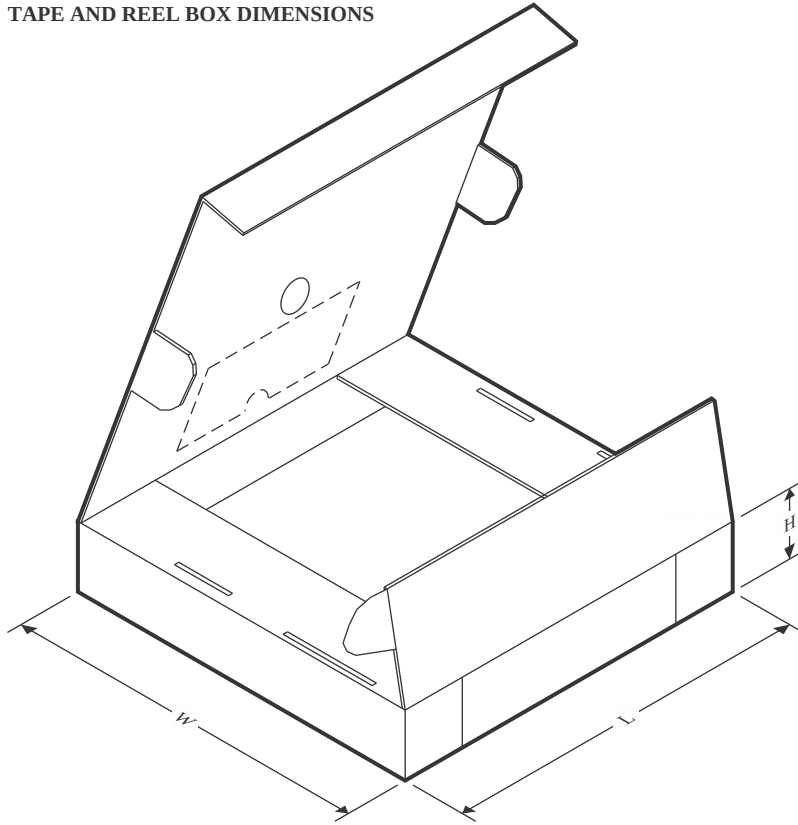
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT574DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVT574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

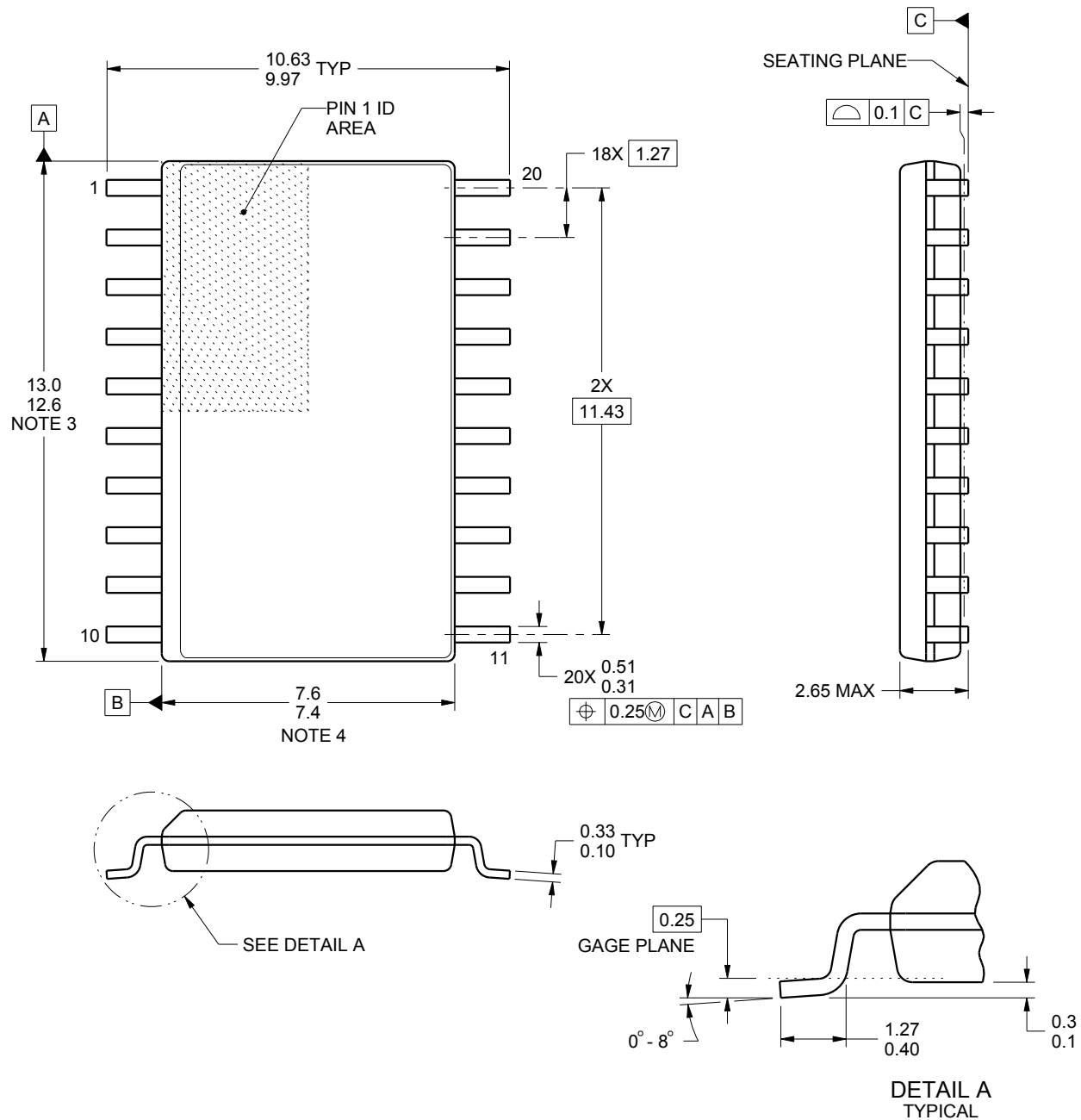
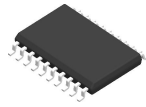
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT574DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVT574PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVT574DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVT574DW.B	DW	SOIC	20	25	507	12.83	5080	6.6



4220724/A 05/2016

NOTES:

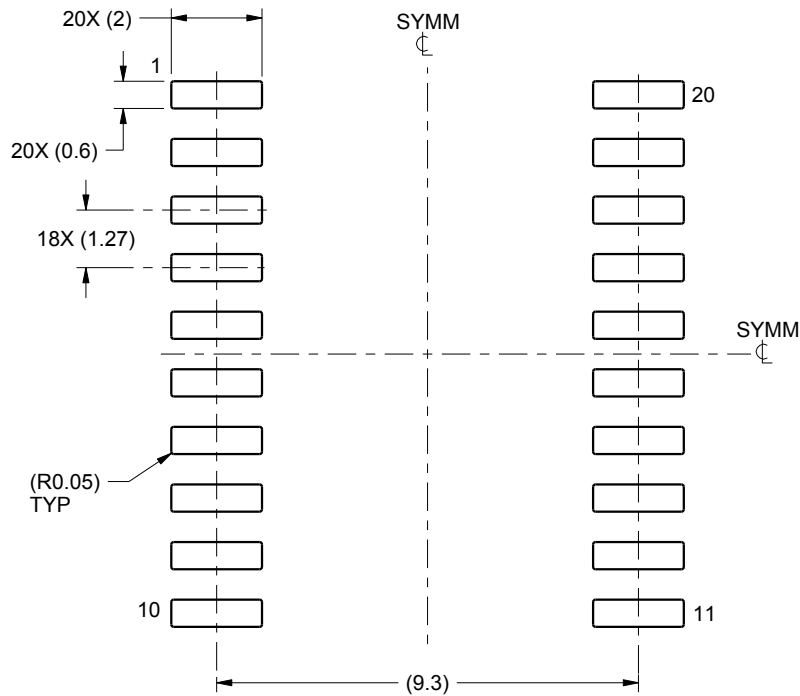
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

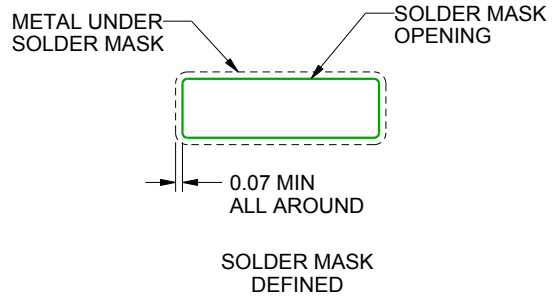
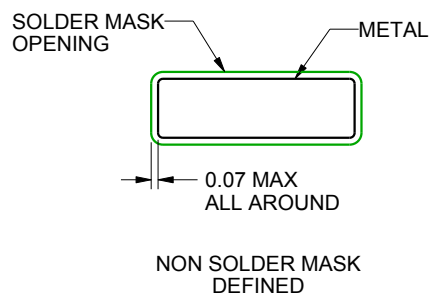
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

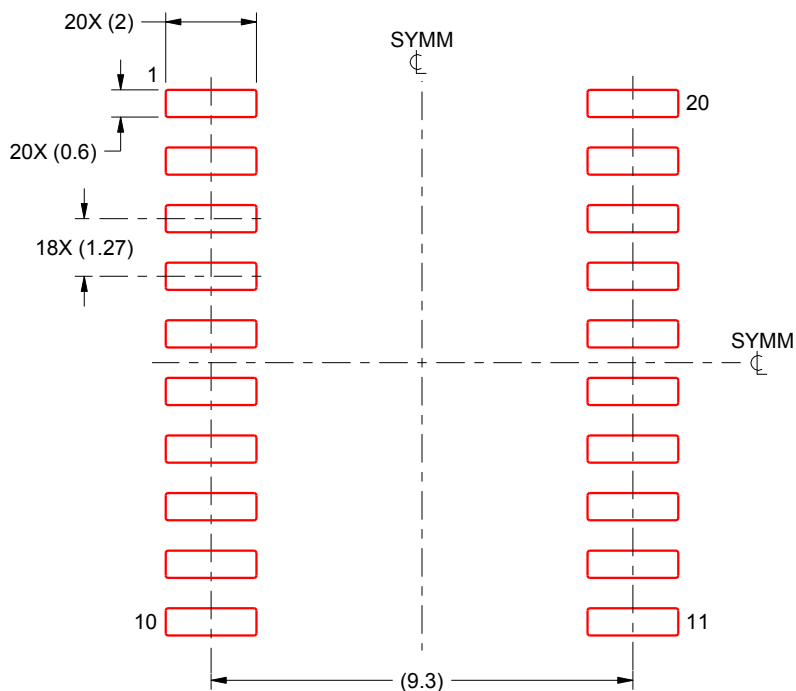
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

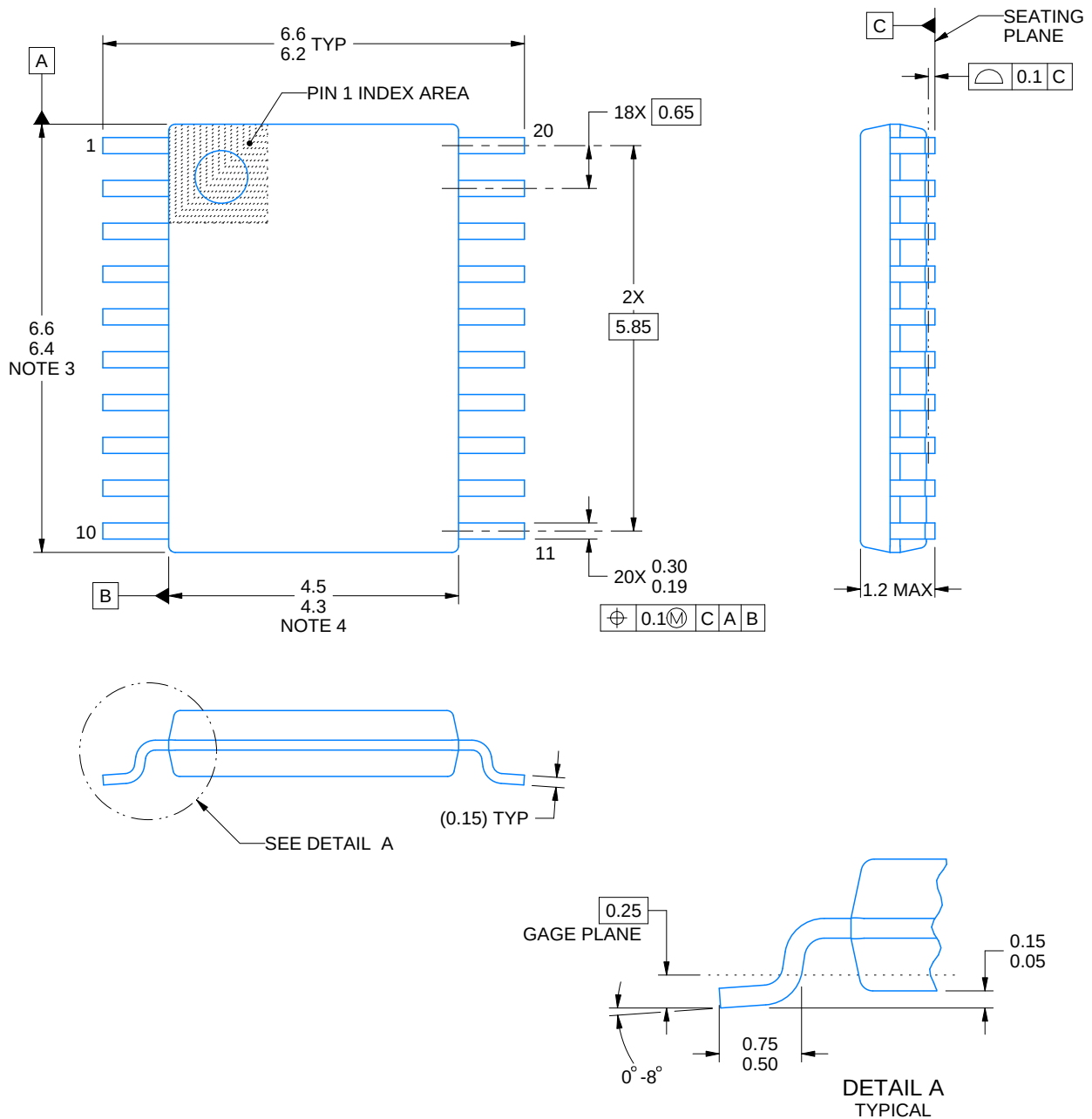
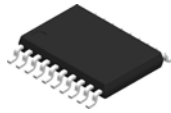


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

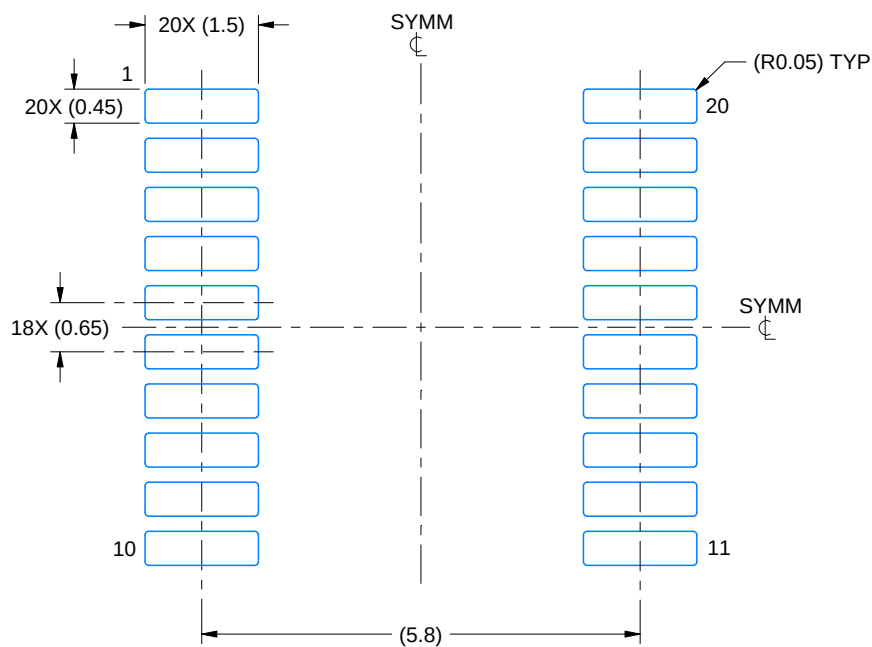
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

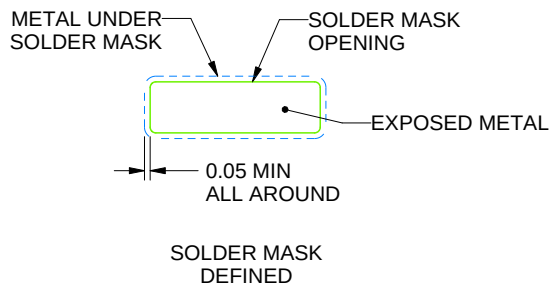
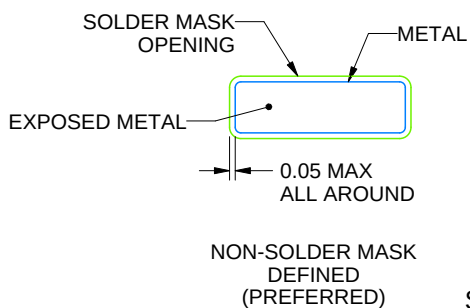
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

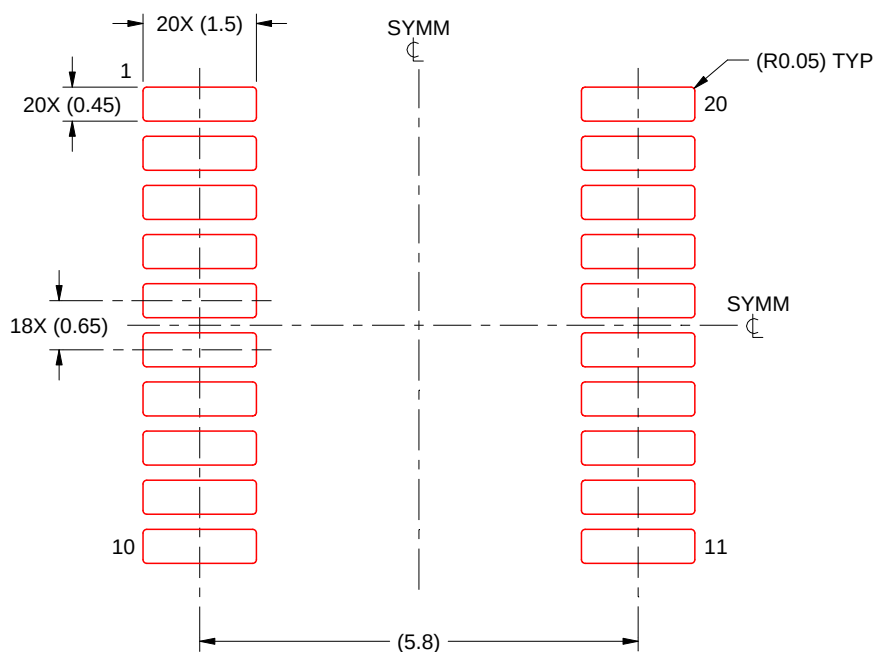
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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