TI Logic Solutions for Memory Interleaving with the Intel™ 440BX Chipset

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TEXAS INSTRUMENTS

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Abstract

Increasing performance requirements of personal computers that necessitate a larger number of SDRAMs and DIMMs can be met by an FET-switch muliplexer. Four devices for memory interleaving for the 440BX and other core-logic chipsets incorporate internal pulldown resistors, damping resistors, and make-before-break features that increase speed while maintaining minimal simultaneous-switching noise.

Introduction

Rapid advancements in hardware and software are emerging to meet the performance needs within the personal computer (PC) industry. To meet the needs of increasing memory requirements, a large number of SDRAMs are needed. Consequently, a larger number of DIMMs are needed, adding heavy loading to the memory controller and to the data lines. To reduce the loading and maintain signal integrity and reliability of the system, an FET-switch multiplexer is recommended for this application. Texas Instruments (TI™) offers four such devices for memory interleaving for the Intel™ 440BX logic chipset and for other core-logic chipsets that need interleaving capability. This report discusses TI's logic solutions using SN74CBT16292, SN74CBTLV16292, SN74CBT162292, and SN74CBTLV162292 devices.

Background

Designing a reliable, high-performance memory system forces designers to consider every detail of the system. Up to 384-Mbytes of system memory can be achieved by using 64-Mbit technology and 168-pin, 8-byte, registered SDRAM DIMMs on three double-sided DIMMs. To achieve a larger memory system with the same type of memory device, a fourth DIMM should be introduced. But, this increases loading. To reduce the loading, an FET-switch multiplexer is recommended. An FET switch on the data line splits the load and reduces it by 50%. In order to design a simple, cost-effective, reliable system, several factors must be considered during FET-switch selection. In the following section, significant information about the SN74CBT16292, SN74CBTLV16292, SN74CBT162292, and SN74CBTLV162292 devices is discussed, as well as applications of this switch on the DIMM.

Device Information

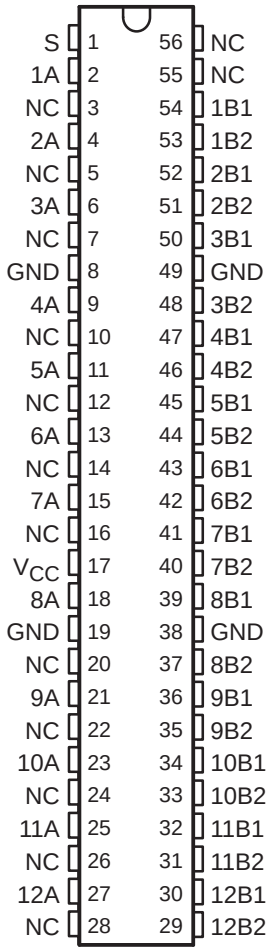
The devices discussed are members of the TI Widebus™ family, which are manufactured using TI's enhanced-performance implanted CMOS (EPIC™) submicron process. Each of these devices is a 12-bit 1-of-2 FET multiplexer/demultiplexer with 500-Ω internal pulldown resistors (R_{INT}). The pinout is the same for each device (see Figure 1). SN74CBT16292 and SN74CBT162292 are designed for 4-V to 5.5-V V_{CC} operation. SN74CBTLV16292 and SN74CBTLV162292 are designed for 2.3-V to 3.6-V V_{CC} operation. The low on-state resistance (4 Ω) of the switch allows connections to be made with minimal propagation delay. When the select (S) input is low, port A is connected to port B1 and port B2 is pulled down through R_{INT} to ground. When S is high, port A is connected to B2 and R_{INT} is connected to port B1 (see Table 1 and Figure 2).

All four devices have the same function. They are different from each other with respect to special features that are discussed in the following paragraphs.

Special Features

Internal pulldown resistors

On all four of these devices, ports B1 and B2 have an internal 500-Ω pulldown resistor connected to GND through a switch. When port B is disconnected from port A, instead of floating, port B is connected to GND through the 500-Ω resistor. If unused inputs are not connected to GND or $V_{CC,}$ they follow any stray noise on that pin, creating unpredictable circuit performance. Termination of unused inputs by connecting them with the internal pulldown resistor increases system reliability and minimizes power dissipation.



NC – No internal connection

Figure 1. Pinout for SN74CBT16292, SN74CBT162292, SN74CBTLV16292, and SN74CBTLV162292 Devices

Table 1. Function Table for SN74CBT16292, SN74CBT162292, SN74CBTLV16292, and SN74CBTLV162292 Devices

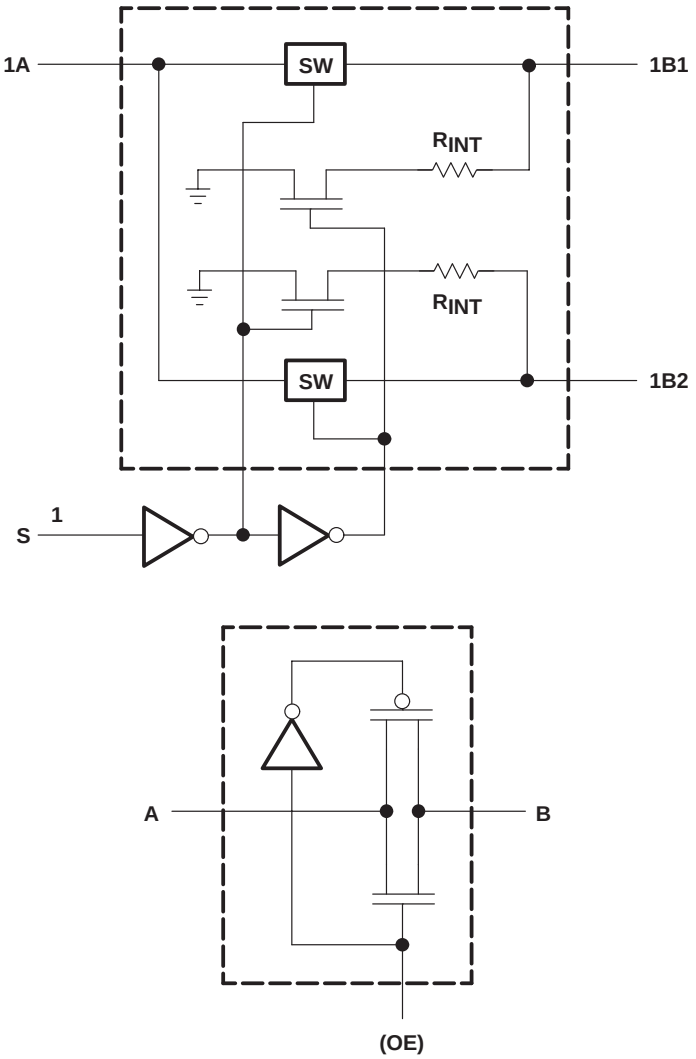
S INPUT	FUNCTION
L	A port = B1 port R_{INT} = B2 port
H	A port = B2 port R_{INT} = B1 port

Damping resistors

SN74CBT162292 and SN74CBTLV162292 have a 25-Ω internal damping resistor connected to port A inputs/outputs. This series termination resistor matches line impedance with the transmission line to reduce noise due to line reflection. It controls signal overshoot and undershoot and maintains noise at a minimum value. If a designer is concerned about the signal integrity, a series damping resistor can be added externally, if it is not incorporated into the device. By using the SN74CBT162292 or SN74CBTLV162292 devices, no external resistors are required.

Make-before-break feature

This unique make-before-break feature is available on all four of these devices. Figure 2 is the logic diagram of CBTLV16292. When S is low, 1A is connected to 1B1 and R_{INT} is connected to 1B2 through the load n channel. When S is high, 1A is connected to 1B2, and R_{INT} is connected to 1B1 through the load n channel. During this transition, the pass p channel or n channel will turn on first, then the load transistor will turn off. This feature causes port 1B1 and 1B2 (outputs) always to be connected either to GND through R_{INT} or to the input, preventing the output from floating and ensuring system reliability. The interval between these two events is known as make-before-break time (t_{mbb}). Figure 3 shows the make-before-break switching, where t_{mbb} is approximately 1.75 ns. The maximum value for t_{mbb} can be 2 ns, which means that the maximum interval between switching on the pass transistor and switching off the load transistor can be 2 ns maximum, which is very low.



Simplified Schematic of Each FET Switch

Figure 2. Logic Diagram for SN74CBTLV16292

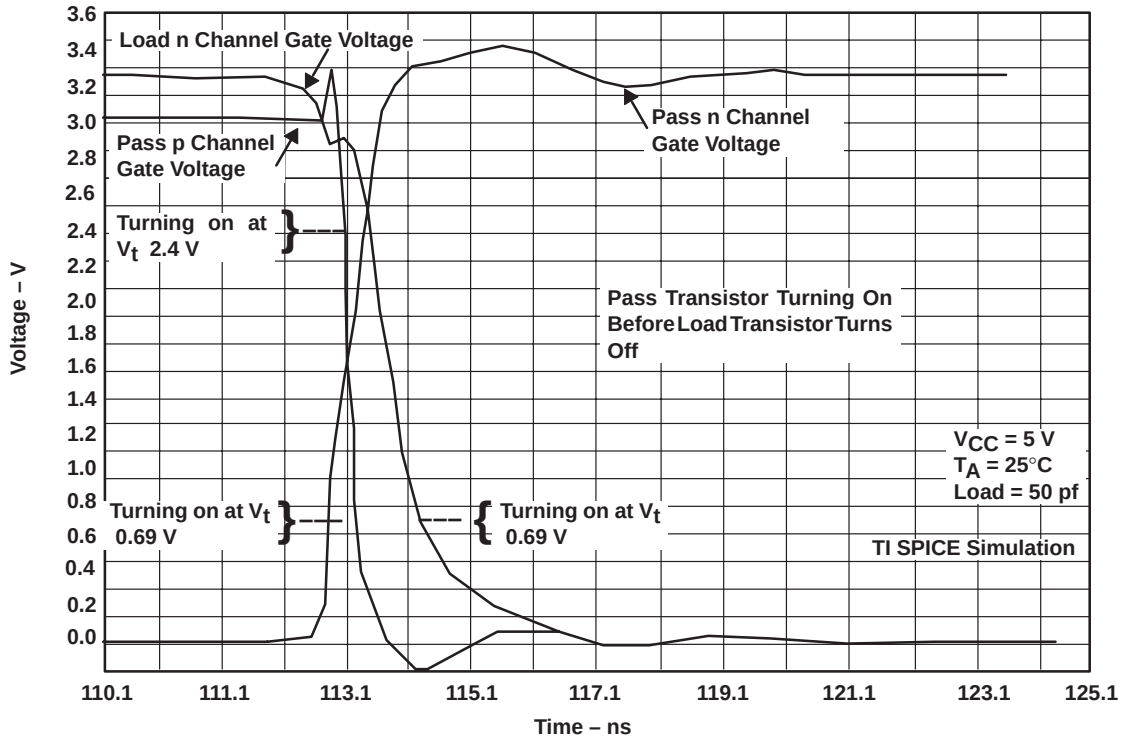


Figure 3. Make-Before-Break Switching for CBTLV16292

Tables 2 and 3 summarize the features and benefits of the CBT16292, CBT162292, CBTLV16292, and CBTLV162292 devices.

Table 2. Features of the CBT Devices

DEVICE	PINS	V_{CC} NOMINAL	I/O VOLTAGES	SERIES RESISTORS	INTERNAL PULLDOWN RESISTORS
CBT16292	56	5 V	3.3 V or 5 V	No	Yes
CBT162292	56	5 V		Yes	Yes
CBTLV16292	56	3.3 V	3.3 V only	No	Yes
CBTLV162292	56	3.3 V		Yes	Yes

Table 3. Benefits of the CBT Devices

DEVICE	SERIES DAMPING RESISTOR	UNUSED INPUTS	V_{CC}
CBT16292	External resistor necessary for impedance match	Connected to ground through 500-Ω pulldown resistor	
CBT162292	No external resistor required	Connected to ground through 500-Ω pulldown resistor	
CBTLV16292	External resistor necessary for impedance match	Connected to ground through 500-Ω pulldown resistor	3-V V_{CC} allows same power plane as memory
CBTLV162292	No external resistor required	Connected to ground through 500-Ω pulldown resistor	3-V V_{CC} allows same power plane as memory

Performance

Speed

In memory-interleaving applications, t_{en} and t_{dis} of the bus switches determine the speed of data transfer. All four of these devices have very fast enable and disable times. Figure 4 shows the enable time vs load capacitance for the four devices. The graph shows a very fast enable time over a wide range of load capacitance. At 25-pF to 30-pF load, which closely matches the DIMM loading, all the devices have t_{en} of 3 ns to 4 ns.

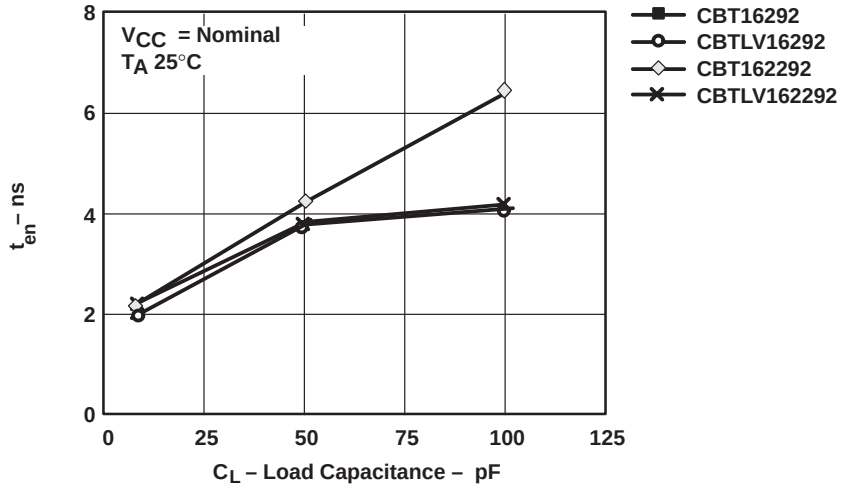


Figure 4. t_{en} vs C_L

Figure 5 shows the disable time over a wide range of load capacitance. The graph shows that, at a load of 25 pF to 30 pF, t_{dis} is between 3 and 4 ns.

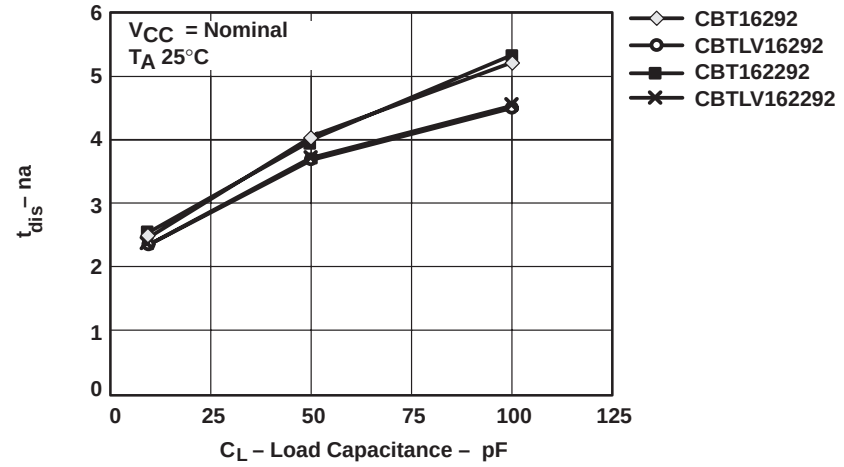


Figure 5. t_{dis} vs C_L

Simultaneous-switching noise

The effects of simultaneously switching multiple outputs of a single device can be examined using a standard procedure. The method of measuring simultaneous switching consists of holding one output low and switching all other outputs from the high state to the low state. Because of the package mutual inductance, transient current flows through the package and into the output pin that is being held low. This causes a rise in voltage and the output begins to ring. The peak of this ringing is called output low peak voltage (V_{OLP}). This is the most common and critical measure of ground bounce. Output low valley voltage (V_{OLV}) is the lowest point the low output reaches, which is usually a negative voltage.

In a similar way, a single output is held high and all other outputs are switched from the low state to the high state. Due to the package mutual inductance, the high output voltage drops, causing the outputs to ring. This valley is called output high valley voltage (V_{OHV}) and the peak is called output high peak voltage (V_{OHP}).

When V_{OLP} goes above 0.8 V, the device enters the threshold region and can switch from the low state to the high state. If V_{OHV} drops below 2 V, the device can switch from high to low. Table 4 shows the simultaneous switching data for the four CBT devices under discussion. Table 4 shows that these devices maintain a safe value for both V_{OLP} and V_{OHV}. Figures 6 through 13 show the simultaneous-switching plots for CBT16292, CBT162292, CBTLV16292, and CBTLV162292.

Table 4. Simultaneous-Switching Data

OPERATING CONDITION	DEVICE	V_{OLV} (mV)	V_{OLP} (mV)	V_{OHV} (mV)	V_{OHP} (mV)
V_{CC} = Nominal T_A= 25°C C_L = 50 pF	CBT16292	–0.12	0.44	3.64	4.36
	CBT162292	–0.08	0.24	3.44	4.00
	CBTLV16292	–0.14	0.28	3.14	3.44
	CBTLV162292	–0.06	0.24	2.98	3.24

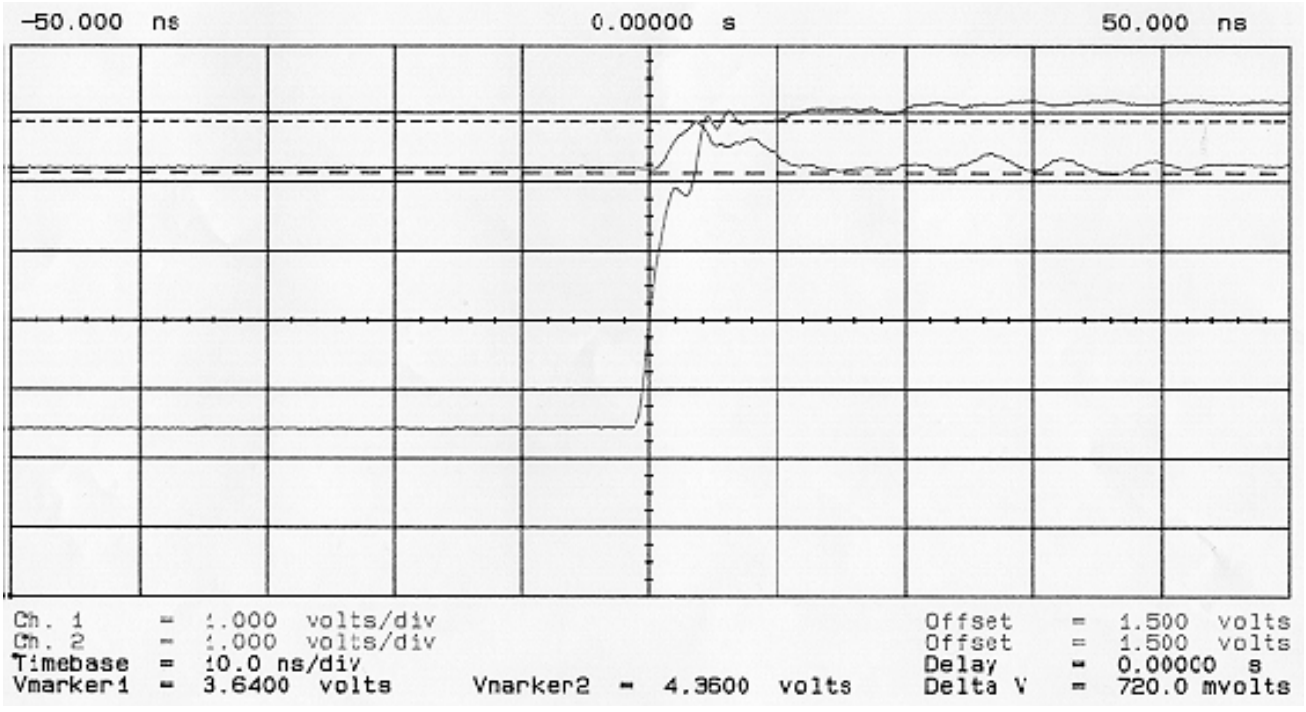


Figure 6. Simultaneous-Switching Plot for CBT16292 (V_{OHV}, V_{OHP})

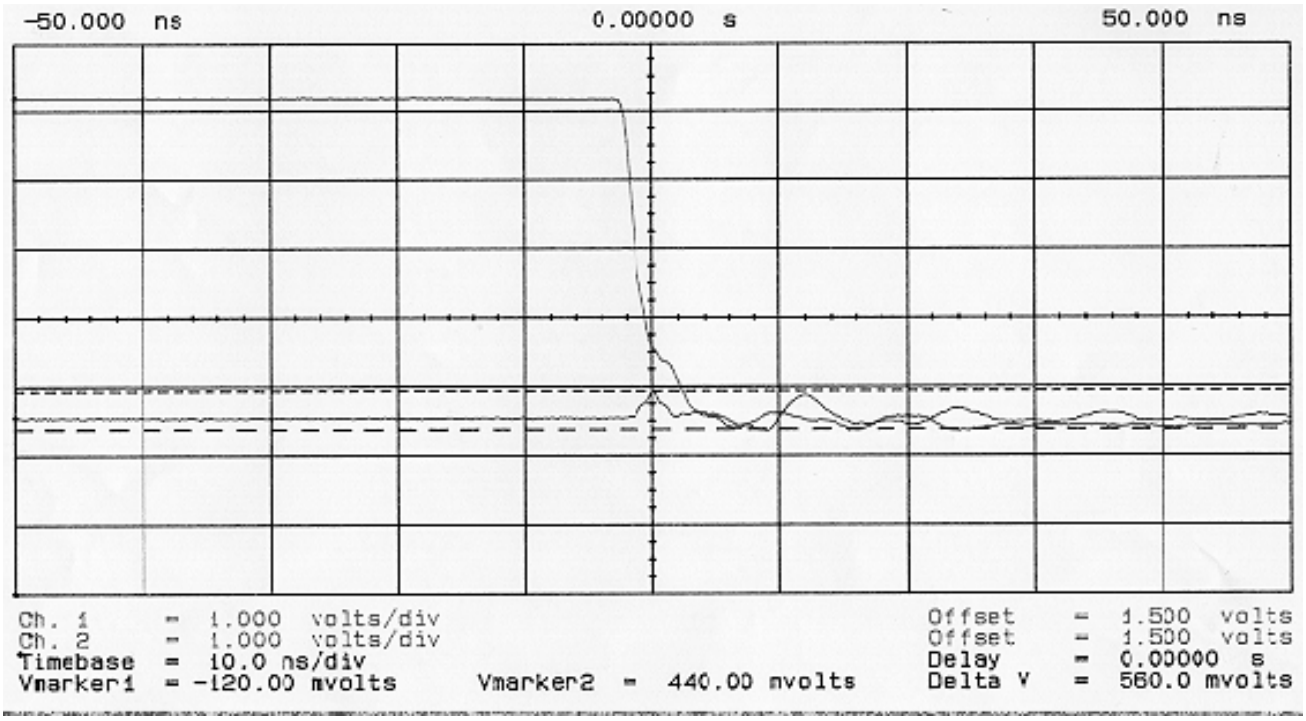


Figure 7. Simultaneous-Switching Plot for CBT16292 (V_{OLV}, V_{OLP})

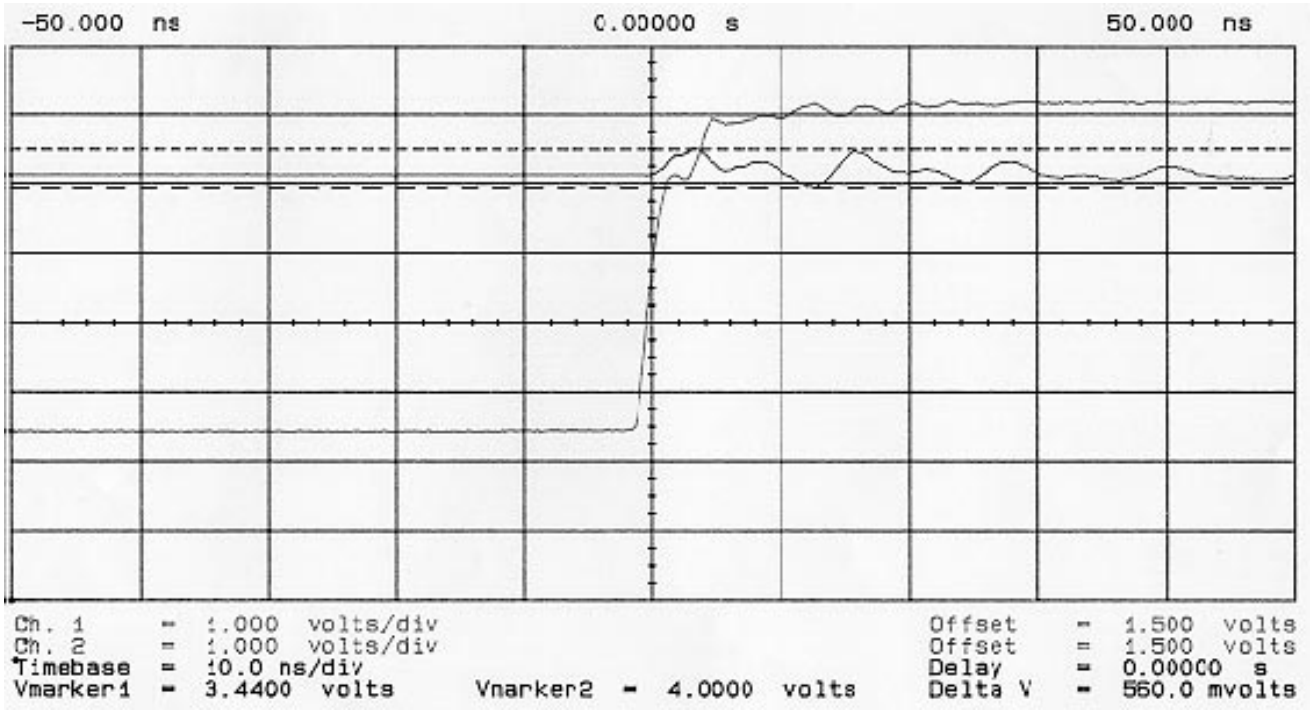


Figure 8. Simultaneous-Switching Plot for CBT162292 (V_{OHV}, V_{OHP})

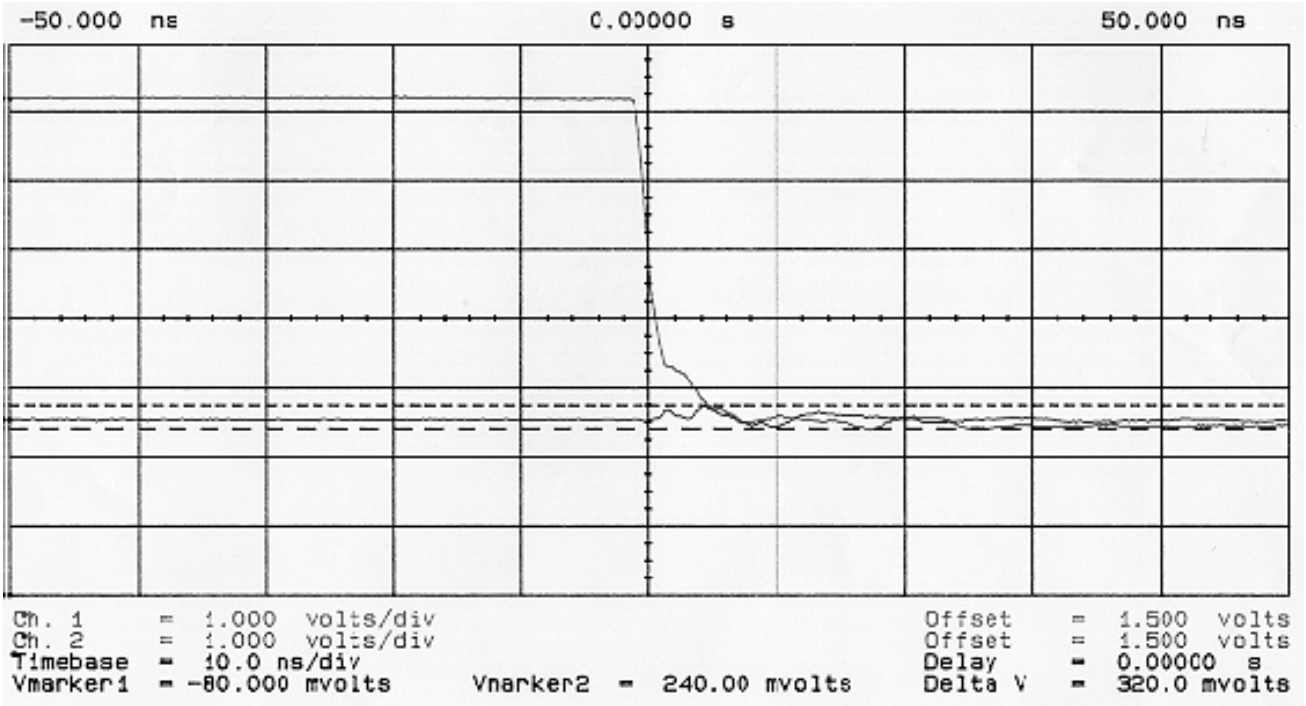


Figure 9. Simultaneous-Switching Plot for CBT162292 (V_{OLV}, V_{OLP})

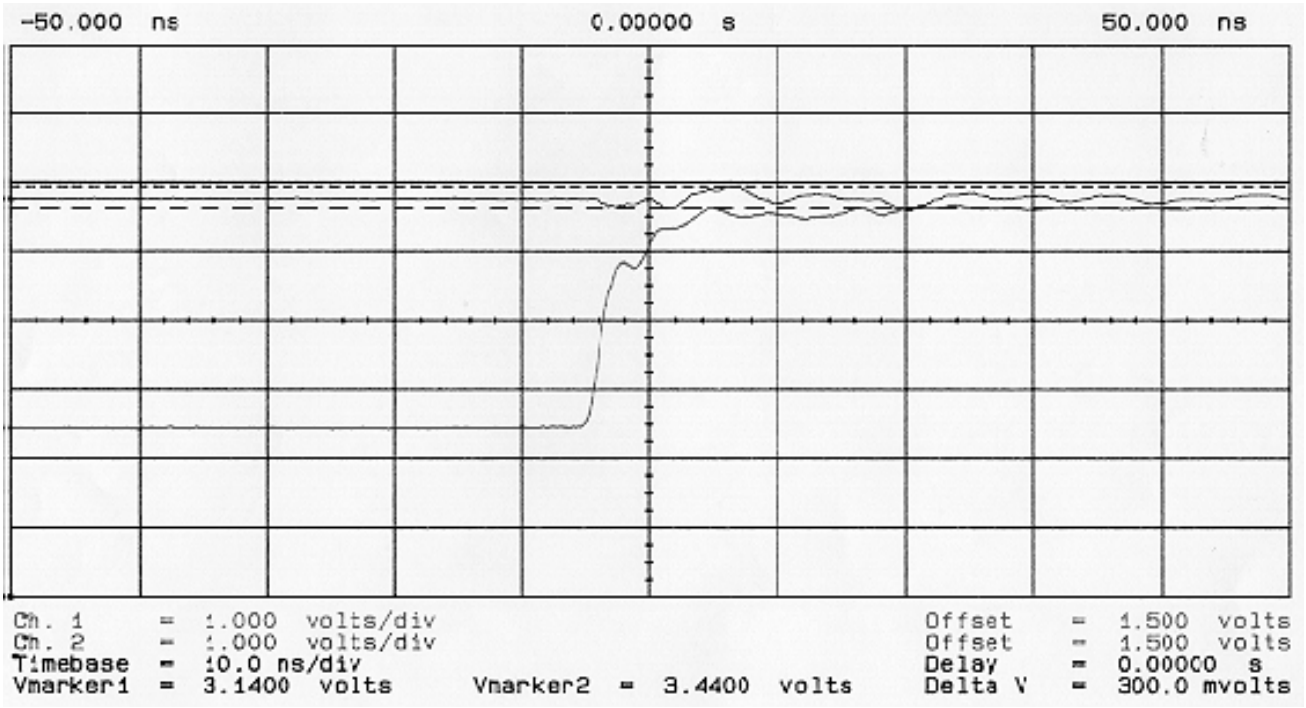


Figure 10. Simultaneous-Switching Plot for CBTLV16292 (V_{OHV}, V_{OHP})

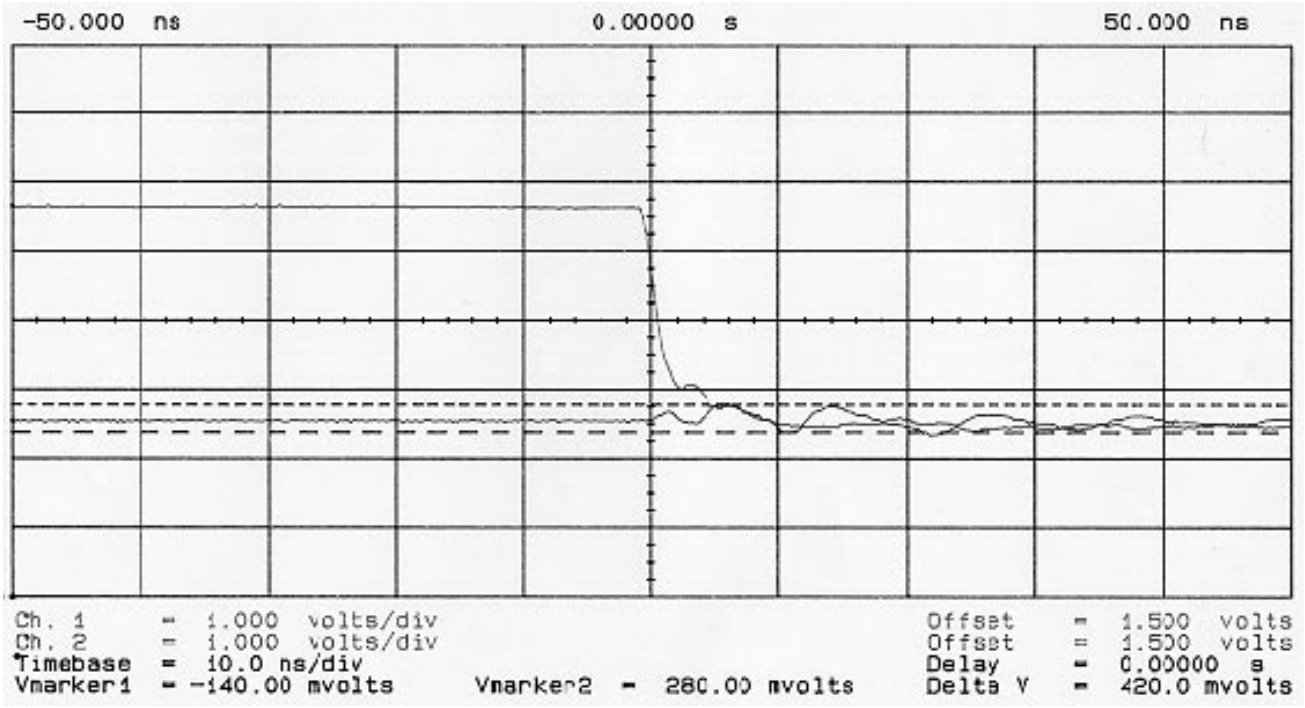


Figure 11. Simultaneous-Switching Plot for CBTLV16292 (V_{OLV}, V_{OLP})

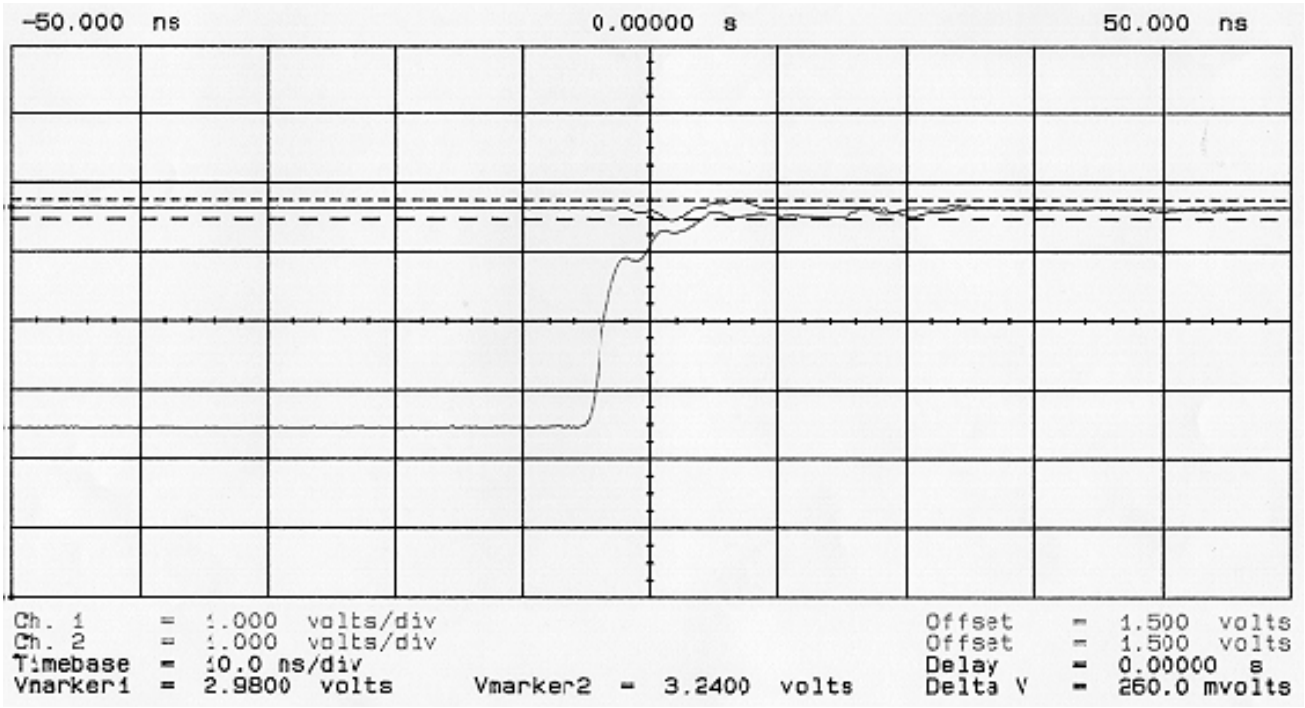


Figure 12. Simultaneous-Switching Plot for CBTLV162292 (V_{OHV}, V_{OHP})

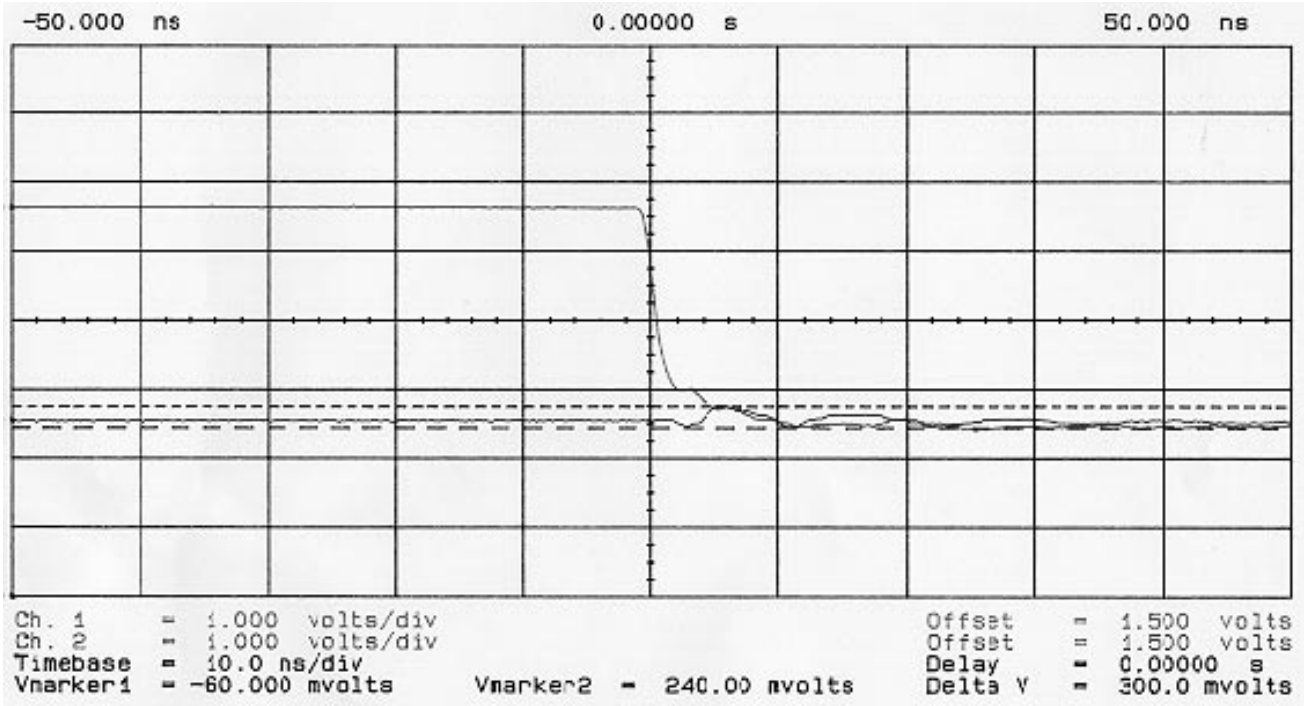


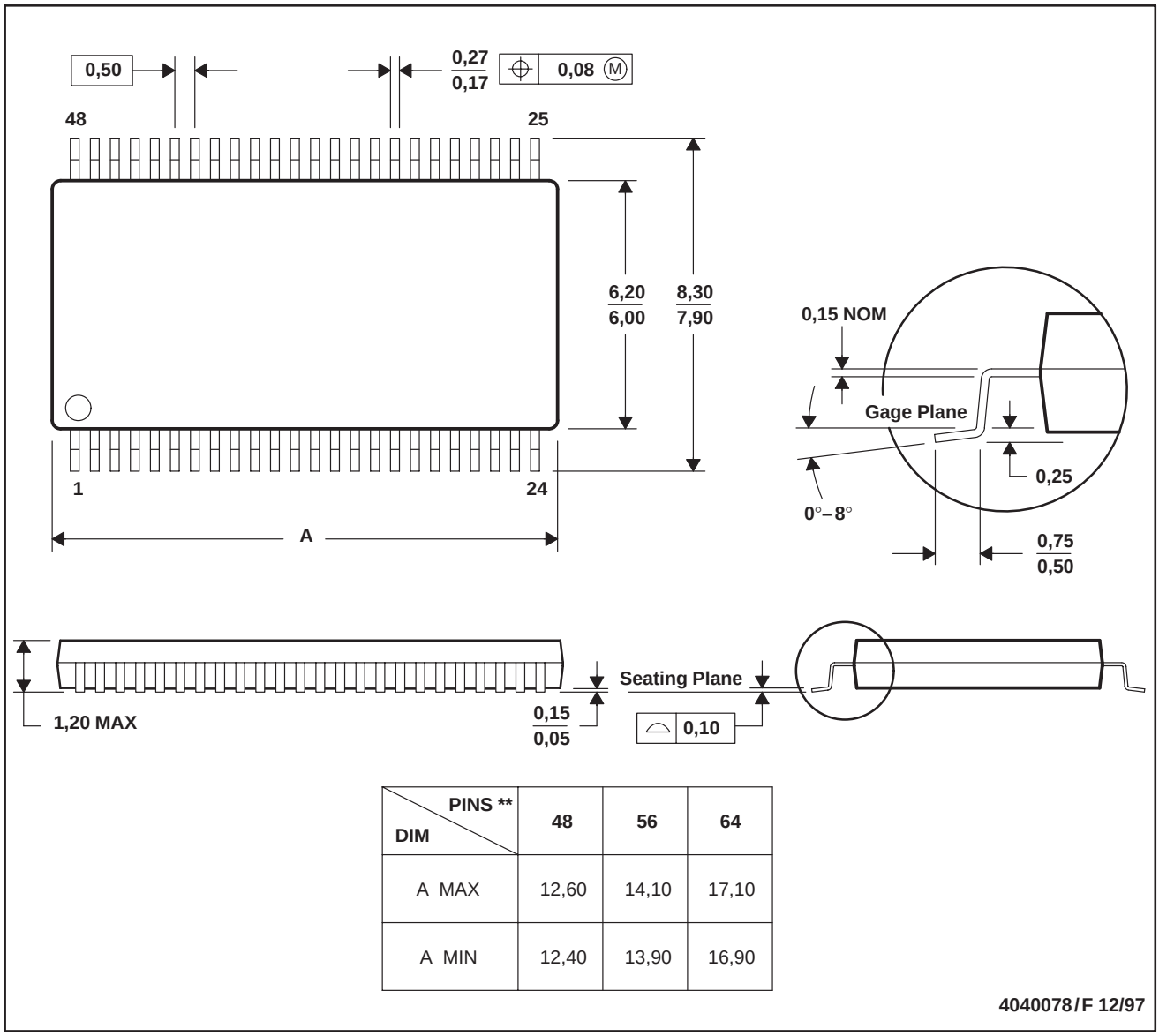
Figure 13. Simultaneous-Switching Plot for CBTLV162292 (V_{OLV}, V_{OLP})

Package Information

All of the devices discussed in this application report are available in the JEDEC-standard TSSOP (DGG) and TVSOP (DGV) packages. The mechanical data are shown in Figures 14 and 15.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



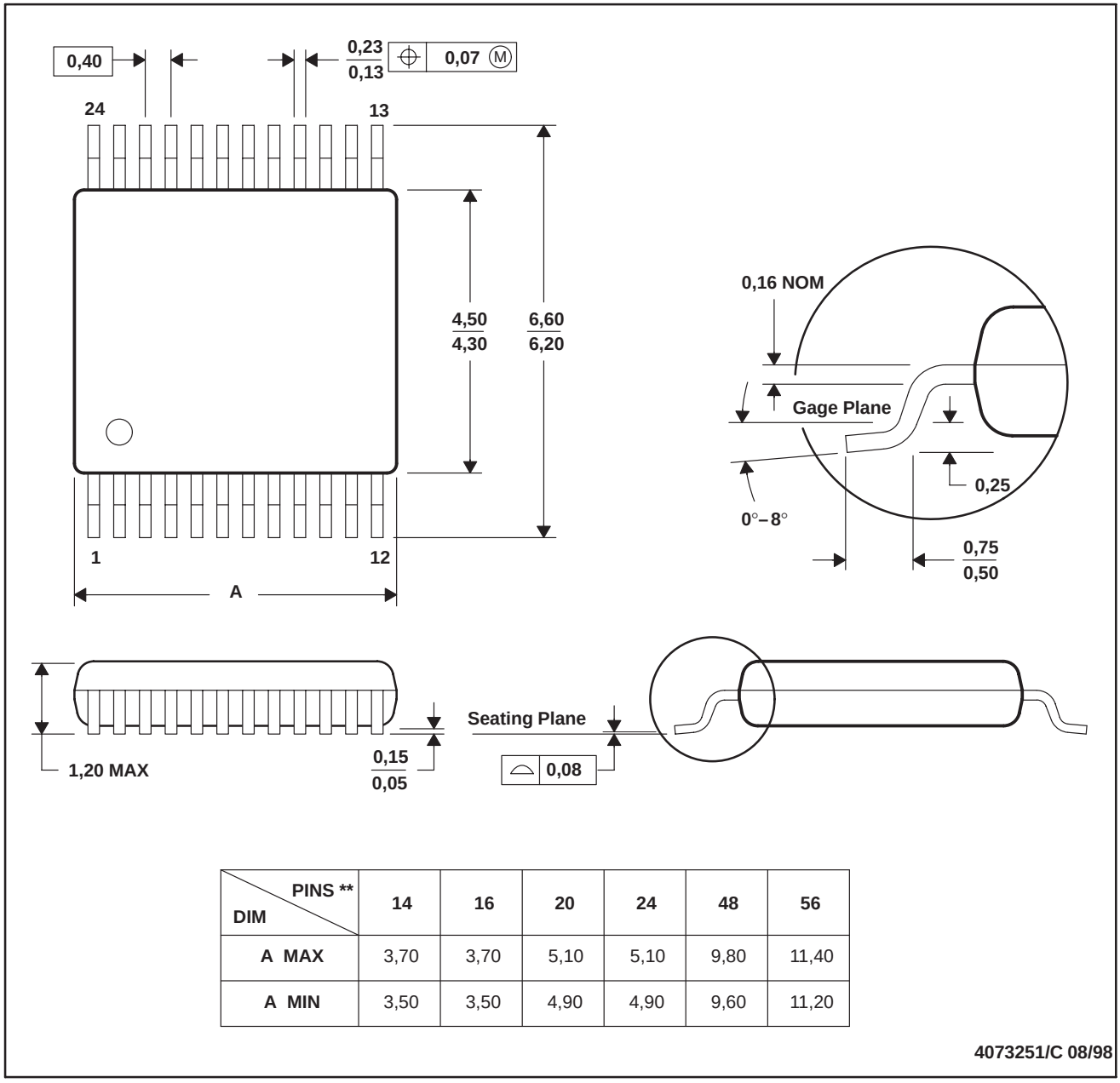
DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

Figure 14. Package Outline Diagram (DGG)

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	48	56
A MAX	3,70	3,70	5,10	5,10	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	9,60	11,20

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

Figure 15. Package Outline Diagram (DGV)

Applications

High-performance desktop computers and servers utilizing Intel Pentium II or Pentium III processors and the 440BX chipset require large amounts of memory support to run complex applications. Currently, with three double-sided DIMMs using 64-Mbit technology, a total memory size of 384 Mbyte is possible. To support 512 Mbytes, a fourth DIMM must be added. The 82443BX integrates a memory controller that supports a 64/72-bit DRAM interface and operates the interface at 66 MHz or 100 MHz, while supporting up to four double-sided DIMMs. To meet the tight 100-MHz timing requirements for a four-DIMM configuration, the CBT16292 bus switch is recommended.

The BX controller supplies two copies of memory address (MA) for effectively driving the address load and optimizing strict timing requirements placed on it by the 100-MHz address bus. The controller also supplies the FET-enable signal (FENA) to enable CBT switches. For the data bus to offset heavy loading to the data-in/data-out (DQ) line with the additional fourth DIMM, the CBT16292 (12-bit to 24-bit mux/demux with internal 500-Ω pulldown resistors) is recommended. This reduces the loading to the data bus. To the memory controller it looks like there are only two DIMMs instead of four. Figure 16 shows the application of the CBT16292. With error correction code (ECC), six devices are needed to buffer the 72-bit signals. This task also can be accomplished by using CBT162292, CBTLV16292, or CBTLV162292 devices.

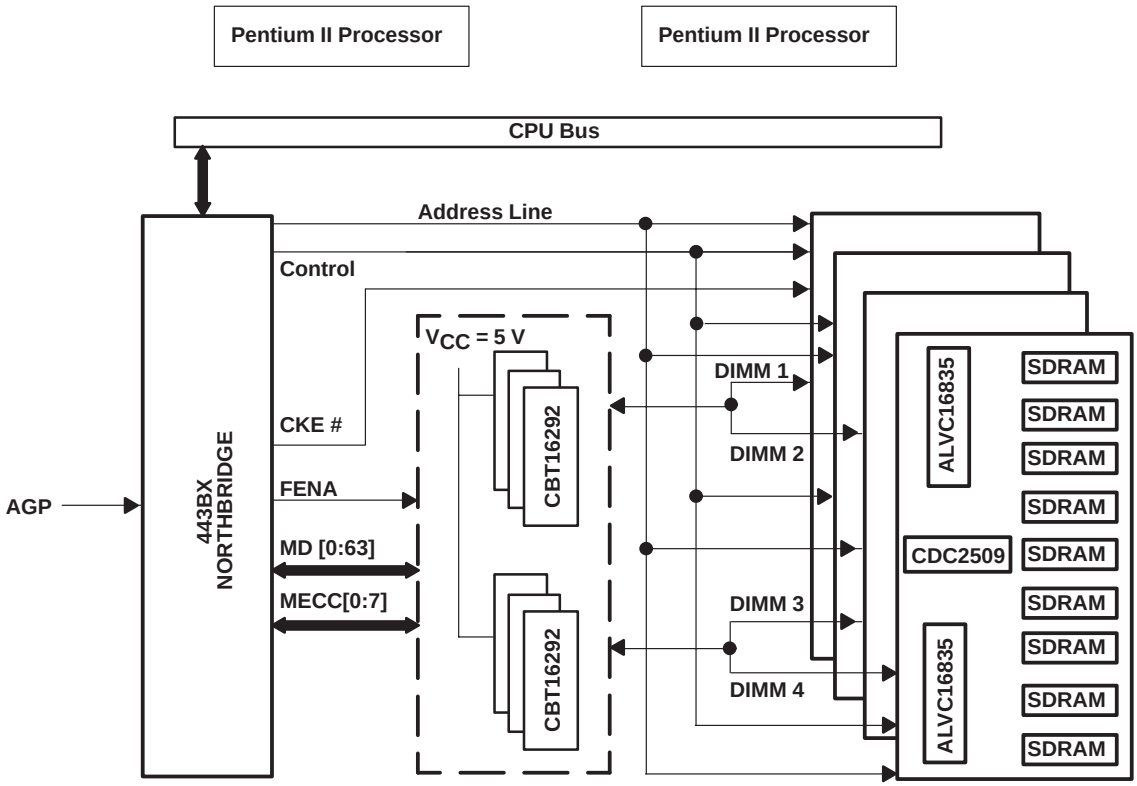


Figure 16. CBT16292 in a Four-DIMM Memory-Switching Application

Figure 16 shows that the CBT16292 plays an integral part in the overall memory solution. Layout and routing should be taken into account. Determining the optimal line length depends on different simulation methods that can accommodate strict timing requirements of a 100-MHz bus. Figure 17 is an example of a typical motherboard layout integrating CBT16292 for four DIMMs. This layout also shows that, by using the CBT16292, the design is more effective because there can be equal load distribution, which can minimize skews.

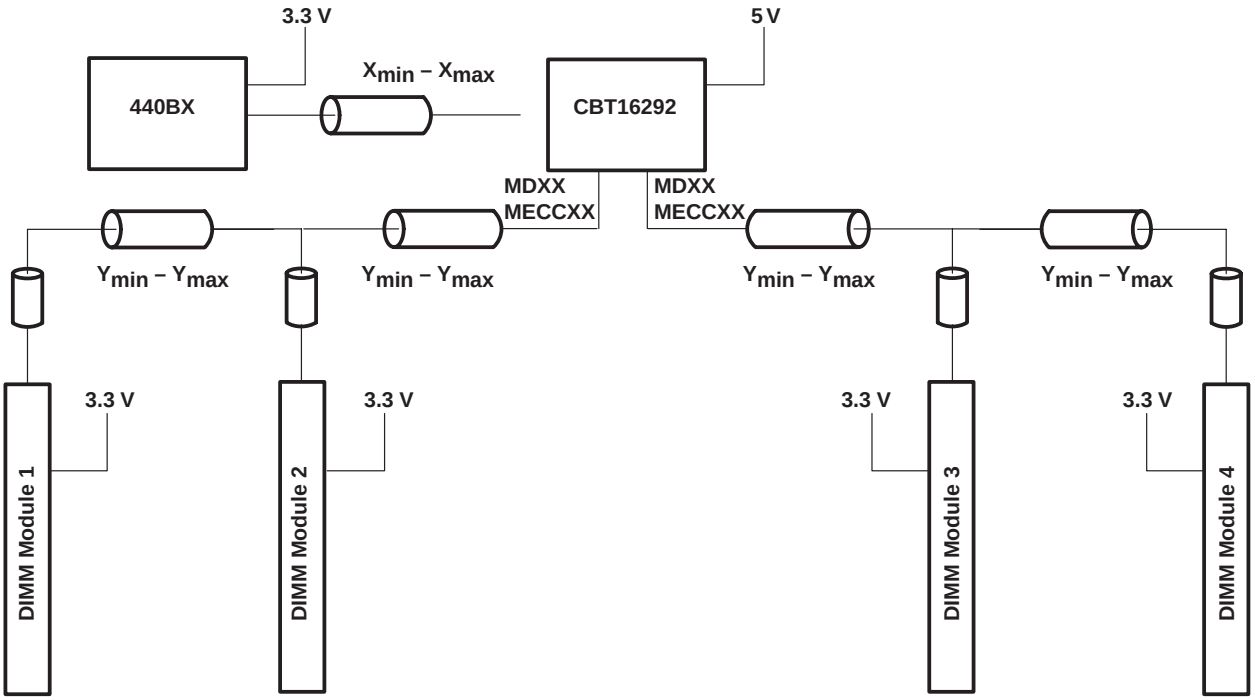


Figure 17. Typical Motherboard Layout Using CBT16292

To further optimize the layout and design shown in Figure 17, the CBTLV16292 and CBTLV162292 also are available. By using these 3.3-V FET-switch parts, all three parts of the memory solution are on the same power plane, and performance is not sacrificed.

Conclusion

TI's CBT16292, CBT162292, CBTLV16292, and CBTLV162292 bus-switch solutions allow successful 100-MHz system integration. TI's '16292 solutions reduce loading, increase reliability, and ease overall timing when integrating the devices with Intel's 440BX chipset.

Acknowledgment

The authors of this application report are Ji Park, Nadira Sultana, and Chris Cockrill.

Glossary

C

CBT	Crossbar technology
CMOS	Complementary metal-oxide semiconductor

D

DIMM	Dual in-line memory module
DRAM	Dynamic random-access memory
DQ	Data-in/data-out line

E

ECC	Error correction code

F

FET	Field-effect transistor
FENA	FET select signal

M

Mbyte	Megabyte
MA	Memory address

P

PC	Personal computer
pF	Picofarad

S

SDRAM	Synchronous dynamic random-access memory

T

TI	Texas Instruments
t_{en}	Enable time
t_{dis}	Disable time
TSSOP	Thin shrink small-outline package
TVSOP	Thin very small-outline package

V

V_{OLP}	Output low peak voltage
V_{OLV}	Output low valley voltage
V_{OHV}	Output high valley voltage
V_{OHP}	Output high peak voltage