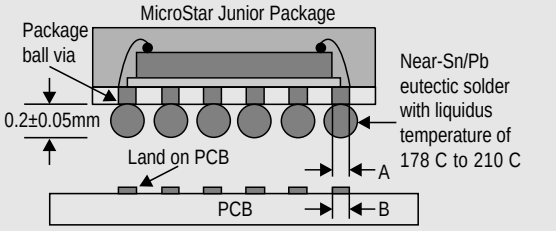
Design Summary for 56GQL (48- and 56-pin functions) MicroStar Junior™ BGA

PCB Design Guidelines

Package Via to Board Land Area Configuration

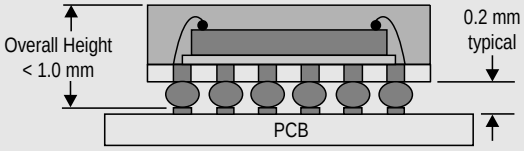


(Not to scale)

A = Via diameter on package = 0.33 mm (for 0.65-mm pitch)
B = Land diameter on PCB

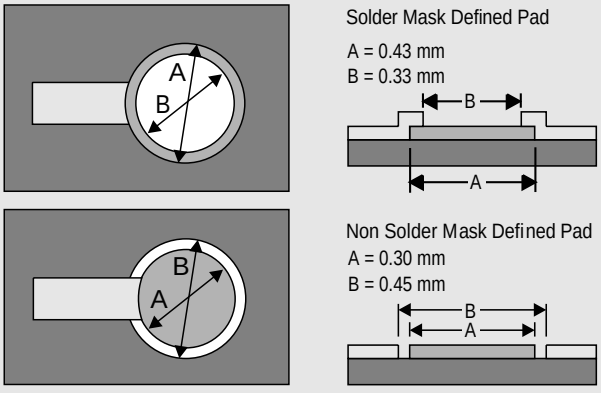
Ratio A/B should equal 1.0 for optimum reliability

Solder Ball Collapse

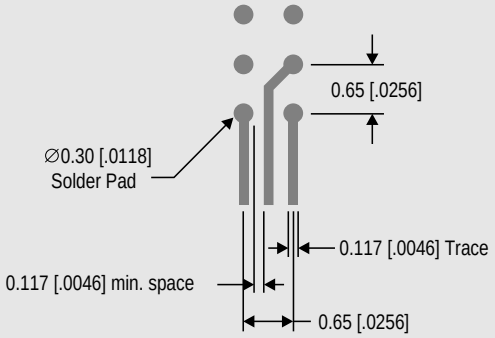


(Not to scale)

VFBGA Recommended Land Pad Design

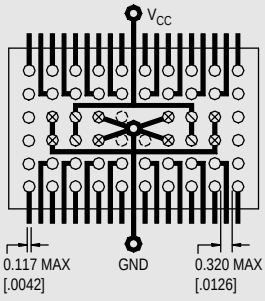


Trace Width/Spacing Dimensions (mm [in.]) Non-Solder Mask Defined Pad



Trace width/spacing for non-solder mask defined = 0.1167 [.0046]
Trace width/spacing for solder mask defined with ∅0.33 solder pad = 0.0733 [.0029]

Recommended Board Routing



Recommended Routing for VFBGA-48

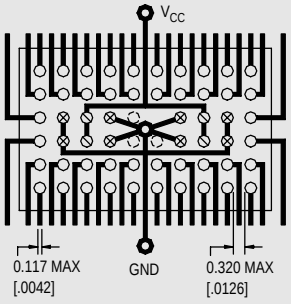
⊗ GND
⊘ V_{CC}

Note: Typical for most devices. Refer to data sheet for specific applications.

Recommended Routing for VFBGA-56

⊗ GND
⊘ V_{CC}

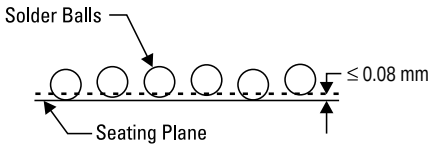
Note: Typical for most devices. Refer to data sheet for specific applications.



Geometric Dimensional Tolerances

Coplanarity

This geometric dimensioning and tolerancing (GD & T) term ⌓ 0,08 mm means that this package meets a coplanarity of 0.08 mm as shown below. Coplanarity is defined as a unilateral tolerance zone measured upward from the seating plane. (Reference ASME Y14.5-1994).



Position Tolerance

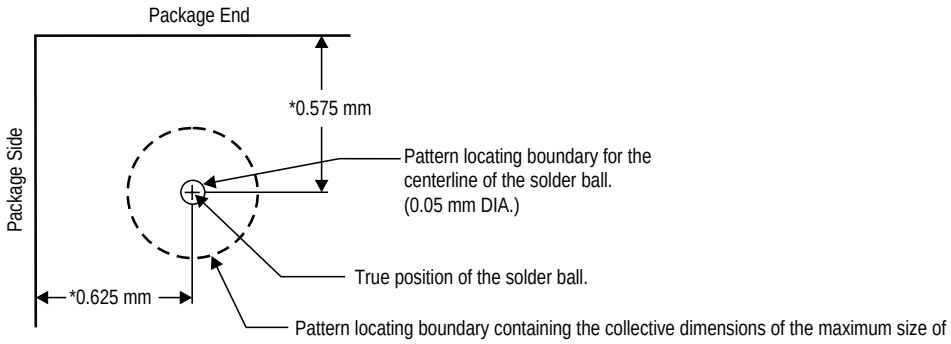
This GD & T term ⌖ ∅ 0,05 Ⓜ is described below:

⌖ This is the symbol for true position.
True position is defined as the theoretically exact centerline location of the solder ball(s).

∅ 0,05 This symbol/number represents how much the centerline of the solder ball(s) is allowed to vary from it's true position.

Ⓜ This symbol/letter is defined as the maximum material condition of the solder ball(s) which is 0.45 mm DIA.

The graphic representation is shown below for the top, left solder ball of this package.



I.E., the solder ball, regardless of size, must fall within this boundary. (Defined as ëvirtual conditioní per ASME standard Y14.5 - 1994).

Please note that a smaller diameter solder ball will have more tolerance in this boundary than the maximum diameter solder ball.

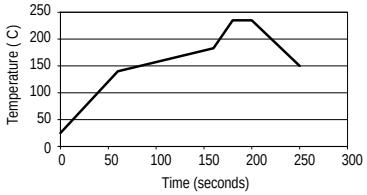
* These two dimensions are calculated based on a package with nominal body width and length dimensions.

IR Reflow Profile

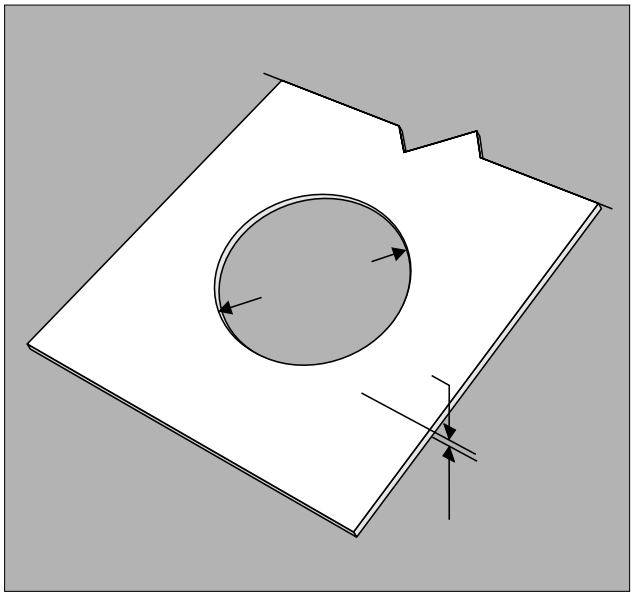
Ideal (1st and 2nd) Reflow Profile

Room Temp to 140 C:	60 - 90 sec.
140 C to 160 C:	90 - 120 sec.
Time above 200 C:	30 - 60 sec.
Peak Temp:	235 C ±5 C
Time within 5 C Peak Temp:	10-20 sec.
Ramp down rate:	1 - 3 C/sec. max.

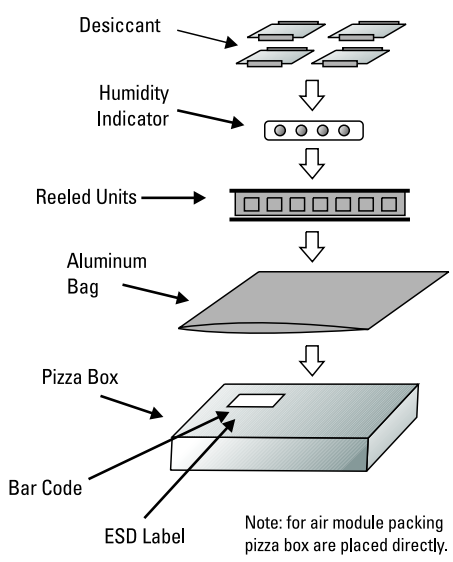
Ideal Reflow Profile



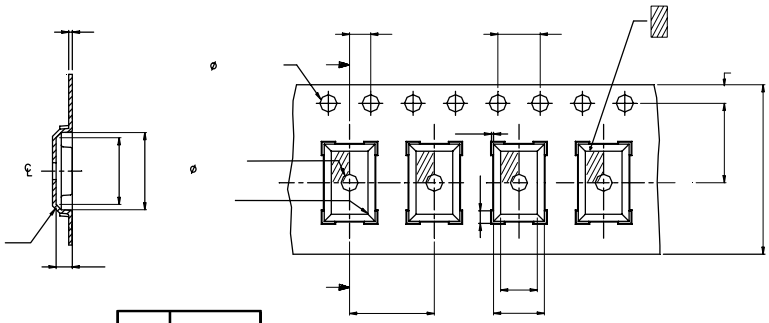
Note:
This is an ideal profile, and actual conditions obtained in any specific reflow oven will vary. This profile is based on convection or RF plus forced convection heating.

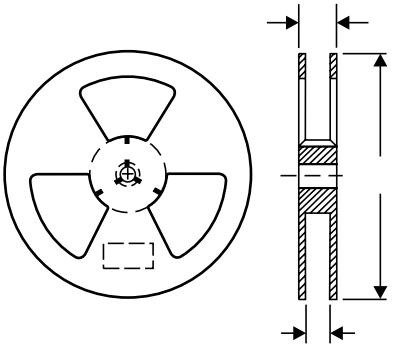


Tape and Reel Packing



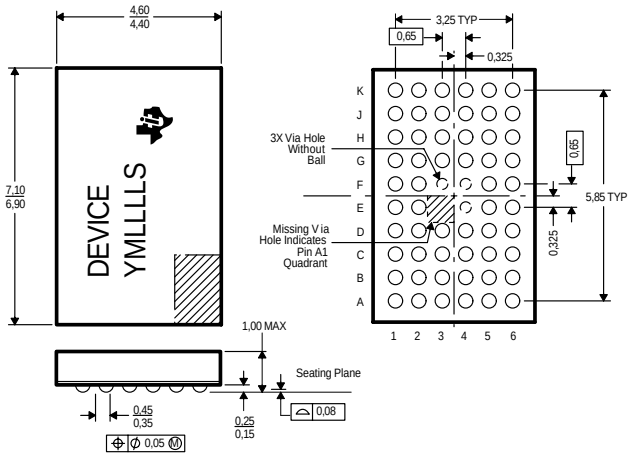
Note: for air module packing pizza box are placed directly.





48/56GQL (4.5 x 7.0 mm, 0.65 mm pitch)

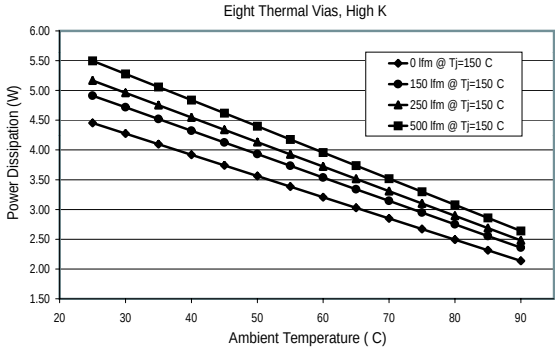
Package Outline

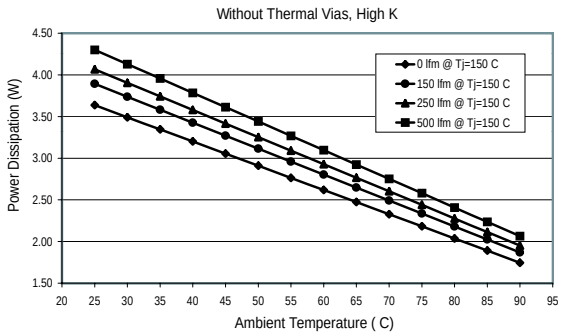


Electrical Characteristics

	R(ohms)	L(nH)	C(pF)
Min.	0.048	1.470	0.182
Mean	0.066	2.257	0.264
Max.	0.116	3.965	0.430

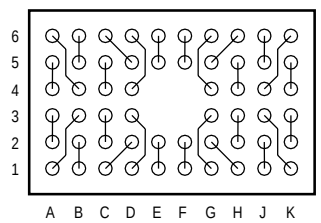
Thermal Characteristics





Daisy Chain Net List

56GQL TOP VIEW



A1-B3	J4-K6
A2-A3	K4-K5
A4-A5	K2-K3
A6-B4	J3-K1
B5-B6	J1-J2
C6-D5	G2-H1
C4-C5	H2-H3
D4-D6	G1-G3
E5-E6	F1-F2
F5-F6	E1-E2
G4-G6	D1-D3
H4-H5	C2-C3
G5-H6	C1-D1
J5-J6	B1-B2

Pinout

Pinout for 48-pin functions

	A	B	C	D	E	F	G	H	J	K
6	áA48	A46	A43	A40	A37	A36	A33	A30	A27	áA25
5	NC	A47	A44	A41	A38	A35	A32	A29	A26	NC
4	NC	*A45	ÜA42	*A39			*A34	ÜA31	*A28	NC
3	NC	*A4	ÜA7	*A10			*A15	ÜA18	*A21	NC
2	NC	A2	A5	A8	A11	A14	A17	A20	A23	NC
1	áA1	A3	A6	A9	A12	A13	A16	A19	A22	áA24

áControl *GND ÜV_{CC}

Note: This is a topside view

Pinout for 56-pin functions

	A	B	C	D	E	F	G	H	J	K
6	áA54	A51	A48	A45	A43	A42	A40	A37	A34	áA31
5	áA55	A52	A49	A47	A44	A41	A38	A36	A33	áA30
4	áA56	A53	ÜA50	*A46			*A39	ÜA35	*A32	áA29
3	áA1	A4	ÜA7	*A11			*A18	ÜA22	*A25	áA28
2	áA2	A5	A8	A10	A13	A16	A19	A21	A24	áA27
1	áA3	A6	A9	A12	A14	A15	A17	A20	A23	áA26

áControl *GND ÜV_{CC}

Note: This is a topside view

Package Reliability Data

Test Chip: ALVCH16501, 'B' Die Revision, 85 x 107 mils Preconditioning: JEDEC Level 2 (85 C/60% 168 hr + 3IRR 220 C)	Required Sample Size / #Fails	ALVCH16501GQL Actual Sample Size / # Fails
Simultaneous Switching Life Test (SSLT), 150 C, 300 Hours	39 / 0	39 / 0
Highly Accelerated Life Test (HAST), 130 C, 85% RH, 100 Hours	39 / 0	39 / 0
Temperature Cycle Test, -65 C to 150 C, 1000 Hours	77 / 0	77 / 0
Autoclave, 121 C, 96 Hours	77 / 0	77 / 0
Solderability, 8 Hours	8 / 0	8 / 0
Flammability (UL)	5 / 0	5 / 0
Flammability (IEC)	5 / 0	5 / 0
Thermal Shock	26 / 0	26 / 0
X-Ray, Top View Only	5 / 0	5 / 0
Physical Dimensions	15 / 0	15 / 0
Manufacturability	pass	pass

Board Level Reliability Data

56 GQL Package
Sample Size = 32
Temp Cycle Range -40 C to 125 C
No Underfill

Board Thickness (mm)	1.6	0.8	0.8, no Au
0 cycle	0	0	0
250 cycle	0	0	0
500 cycle	0	0	0
750 cycle	0	0	0
1000 cycle	2*	0	0
1250 cycle	15	1	0
1500 cycle	19	8	0
1750 cycle	N/A	20	1
2000 cycle	N/A	N/A	0

* First failure at 951 cycles

t = 0.8 mm, with Au, 50% failure = 1733 cycles

Sockets

Sockets and Socket Manufacturer (Ordering Information)

Yamaichi Socket Numbers: VFBGA-56 PN# IC280-056-237

Yamaichi Electronics USA, Inc.
2235 Zanker Road
San Jose, CA 95131
Phone: (408) 456-0797

Questions and Answers

Board Design/Electrical Issues

Q. Where can the decoupling capacitors go for the VFBGA package?
A. The recommended capacitance value and number of capacitors for decoupling is a 0.1 mF capacitor for each V_{CC} on the VFBGA package. The decoupling capacitors should be connected as close as possible to the GROUND and V_{CC} planes.
Q. Any EMI concerns for traces under the package and how can customers design their board to minimize EMI?
A. EMI can be controlled by minimizing any complex current loops on the PCB trace. Some helpful hints include:
- ï Solid ground and power planes be used in the design. Partitioned ground and power planes must be avoided. These ground and power partitions may create complex current loops increasing radiation.
- ï Avoid right angles or "T" crosses on the trace. Right angles can cause impedance mismatch and increase trace capacitance causing signal degradation.
- ï Minimize power supply loops by keeping power and ground traces parallel and adjancent to each other. Significant package EMI can be reduced by using this method.
- ï Use decoupling capacitors as described in the previous question.

Lead-Free

Q. Is TI developing a lead-free version of MicroStar Junior BGAs?
A. Yes, Texas Instruments is working toward eliminating lead in the solder balls to comply with lead-free environmental policies. The lead-free solder is in final evaluation. Only the solder will change, not the package structure or the mechanical dimensions. The solder system under development is based on Sn-Cu-Ag metallurgy. Check with your local TI Field Sales representative for sample availability.

Assembly Process/Yield Considerations

Q. What size land diameter for these packages should I design on my board?
A. Land size is the key to board-level reliability, and Texas Instruments strongly recommends following the design rules included in this bulletin.
Q. Can customers mount MicroStar Junior BGA packages on the bottom side of the PCB board?
A. Yes, they can and the ideal 2nd reflow profile is the same as the 1st (IR profile is recommended in the bulletin). The root causes for solder ball off are:
- ï Excess amount of solder paste during customers board assembly. TI recommends minimizing the amount of solder paste on the bottom side by using a stencil thickness of 0.15 mm with 0.33-mm aperture opening.
- ï Moisture absorption also affects the ball off issue. The package was qualified at Moisture Level 2, and has been released at Moisture Level 2A. The first and second reflow must be completed within 4 weeks.

Q. Should I use underfill?
A. No, the package qualification results show that this is not necessary and is only an added process expense.
Q. Can the boards be repaired?
A. Yes, there are rework and repair tools and profiles available (see references 4 and 7). We strongly recommend that removed packages be discarded.
Q. How do the board assembly yields of MicroStar Junior BGAs compare to TSSOPs?
A. Many customers are initially concerned about assembly yields. However, once they had MicroStar Junior BGAs in production, most of them report improved process yields compared to TSSOPs. This is due to the elimination of bent and misoriented leads, the wider terminal pitch than with 0.5-mm pitch TSSOPs, and the ability of these packages to self align during reflow. The collapsing solder balls also mean that the coplanarity is improved over leaded components.
Q. What alignment accuracy is possible?
A. Alignment accuracy for the 0.65-mm pitch package is dependent upon board level pad tolerance, placement accuracy, and solder ball position tolerance. Nominal ball position tolerances are specified at ±50 microns. These packages are self-aligning during solder reflow, so final alignment accuracy may be better than placement accuracy.
Q. Are there specific recommendations for SMT processing?
A. Texas Instruments recommends alignment with the solder balls for the CSP package, although it is possible to use the package outline for alignment. Most customers have found they do not need to change their reflow profile.
Q. Can the solder joints be inspected after reflow?
A. Process yields of 5-ppm rejects are typically seen, so no final inline inspection is required. Some customers are achieving satisfactory results during process setup with lamographic X-ray techniques.

Package (Incoming Inspection)

Q. Is package repair possible? Are tools available?
A. Yes, some limited package repair is possible, and there are some semi-auto M/C tools available. However, TI does not guarantee the reliability of repaired packages.
Q. Do the solder balls come off during shipping?
A. No, this has never been observed. The balls are 100 percent inspected for coplanarity, diameter and other physical properties prior to packing for shipment. Because solder is used during the ball attachment process, uniformly high ball attachment strengths are developed. Also, the ball attachment strength is monitored frequently in the assembly process to prevent ball loss from vibration and other shipping forces.

References

Recommended References:

1. MicroStar BGA Packaging Reference Guide - SSYZ015
2. 96 and 114 ball LFBGA Application Note - IDT, Philips Semiconductor and Texas Instruments
3. Board Level Reliability Evaluations of 40, 32 and 30 Mil Pitch Ball Grid Array Packages Over -40 to 125 C - Puligandla Viswanadham, Steve Dunford and Ted Carper, Circuit Card Assemblies Center of Excellence Raytheon Systems Co.
4. Comprehensive User's Guide for µBGA*Packages - www.intel.com/design/flcomp/packdata/297846.htm
5. Solder Paste Printing Guidelines for BGA and CSP Assemblies - Donald C. Burr, published in SMTJanuary 1999.
6. Maintaining BGA Reliability During Rework - Stuart Downes and Robert Farrell, published in SMT January 1999.
7. BGA Rework Considerations - Jennie S. Hwang, published in SMT November 1998.

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Internet

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www.ti.com/sc

TI Distributors
www.ti.com/sc/docs/general/distrib.htm

MicroStar Junior BGA Home Page
www.ti.com/sc/msjunior

Logic Overview Page
www.ti.com/sc/logic

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India	000-117	-800-800-1450
Indonesia	001-801-10	-800-800-1450
Korea	080-551-2804	-
Malaysia	1-800-800-011	-800-800-1450
New Zealand	000-911	-800-800-1450
Philippines	105-11	-800-800-1450
Singapore	800-0111-111	-800-800-1450
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