Application Note

TPLD Devices Managing Smart RGB LEDs

Gerardo Leyva-Hernandez

ABSTRACT

TPLD2001 can help to generate and translate standard logics values in time-based logic typically used in smart 24-bit RGB LEDs for scene lighting in automotive, consumer electronics and personal electronics. Moreover, users can take advantage of TPLDs internal serial communications elements to update the color of the RGB LED using standard I2C or SPI communications. A 16.7 million color RGB LED software-less application is shown as a single device design.

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1 Introduction

This application note shows how TPLD2001 can help to generate and translate standard logics values in time-based logic values and moreover, how to take advantage of the TPLDs internal elements to update the color of the smart RGB LED using standard I2C or SPI communications. In this way, TPLD can help main controllers to minimize the effort to keep updated RGB-base display or visual signals or lighting.

This application note presents to the user the design of a software–less application in a single TPLD device to control a smart 24-bits RGB LED. Additionally, this document shows how to use several timers, DFF, FSM and other elements to make the translation.

Finally, the use of the serial communication module to update the RGB LED color is addressed.

2 Smart LEDs Data and Timing Theory

The Smart LED is waiting for 24-bit color format that is present in the DIN pin after a reset period. The communication is serial, unipolar and RZ communication mode. The order of data is GRB with the most significant bit first, as is shown in Figure 2-1

G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4
R3	R2	R1	R0	B7	B6	B5	B4	B3	B2	B1	B0

Figure 2-1. Data Order in a Smart 24-Bit GRB LED

Regarding the timing for each of the color bits, it is expected that the data signal starts with a high level and returns to zero between pulses. The period of time in high of each color bit determines the value Logic 0 or Logic 1 with a full period that must be around 1200nS typically. Table 2-1 and Figure 2-2 shows the Data Transfer Time for some of the smart LED models in the market. A period larger than 200uS indicates a reset code.

Table 2-1. Timing for Data Transfer

Name	Code Period	Minimum Value	Tolerance
T0H	0 code time for Logic High	350nS	+/-150nS
T0L	0 code time for Logic Low	800nS	+/-150nS
T1H	1 code time for Logic High	700nS	+/-150nS
T1L	1 code time for Logic Low	600nS	+/-150nS
Trst	Logic low for Reset	200uS	

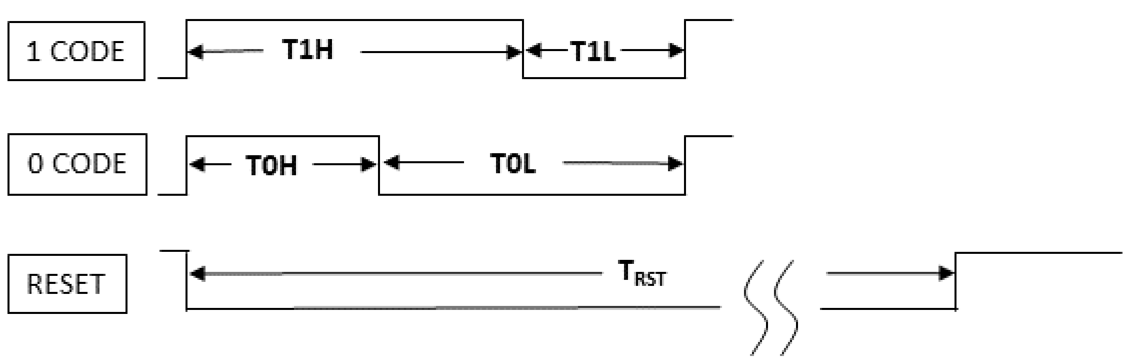

Figure 2-2. Logic Symbol Timing

3 Logic Symbols Generation

An internal 25MHz OSC is generating all the required clock signals including the 12.5MHz by the internal pre-divider OSC/2 that together with counters can generate a time base of 800KHz required by the RGB LED.

Because the clock signal is not symmetrical by design, using TPLD internal delays properly set the T0H and T1H can be generated at 350nS and 800nS, respectively. Controlling the T0L and T1L timing is not required because the required symbol period is actually generated. Figure 3-1 shows the element needed for the time base and symbol generation.

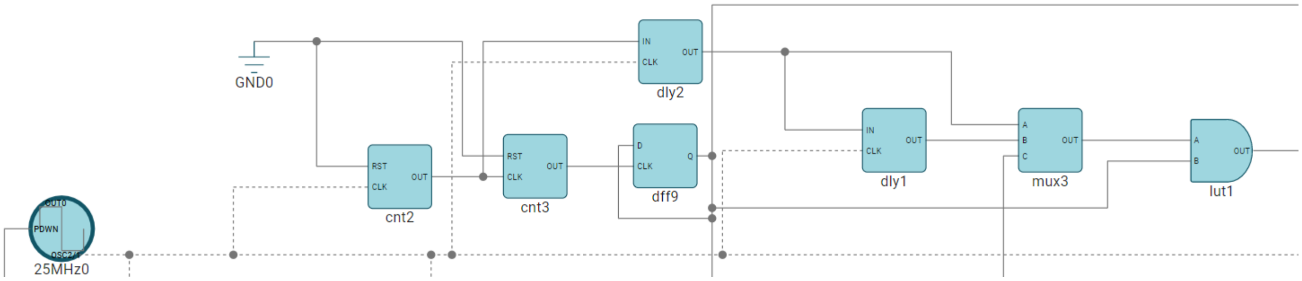

Figure 3-1. Logic Symbol Generation with TPLD

Figure 3-2 shows a screen capture from a logic analyzer of a TPLD device generating all the timing for the logic symbols. A logic multiplexer is used with both symbols as inputs and a select signal generated by other circuit section accordingly to the color that must be generated.

Figure 3-2. Screenshot of Logic High and Low Symbols

4 TPLD-Based Smart LED Controller

Managing the RGB Bits Inside TPLD

The RGB LED must receive 24 bits consecutively to generate a given RGB color as previously mentioned. Moreover, those 24 bits must be kept internally in the TPLD and also those must have the ability to be updated using a Serial Communication Module. The Built-in Finite State Machine (ASM) was selected to handle the RGB information because its ability to generate a maximum of eight states with 8-bits output each (64 bits total) and any of the values of the state can be changed by the user, that all is more than necessary to accomplish the task.

Table 4-1 shows the GRB code 0xFF000 in the State Machine Outputs section. Six states are defined using 4-bit from OUT3 to OUT0. So, the real output generated for the RGB pixel can be seen in the figure 5 that corresponds to the green color.

Table 4-1. ASM Report for the States and Values Defined by the User

State	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
ST0	0	0	0	0	1	1	1	1
ST1	0	0	0	0	1	1	1	1
ST2	0	0	0	0	0	0	0	0
ST3	0	0	0	0	0	0	0	0
ST4	0	0	0	0	0	0	0	0
ST5	0	0	0	0	0	0	0	0
ST6	0	0	0	0	0	0	0	0
ST70	0	0	0	0	0	0	0	0

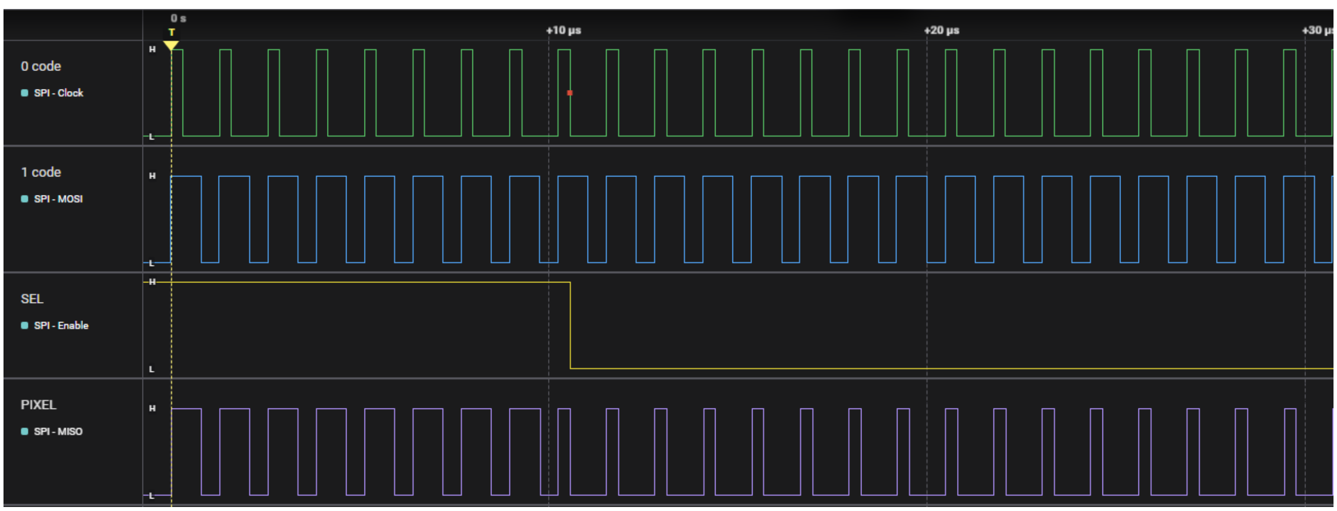

Figure 4-1. 24 Bits that Represents the Value 0xFF000 for the Green Color in the RGB LED

Parallel-Serial Shift Register

This device section is designed as a 4-bit parallel load shift register that shifts the data toward a serial output (SER3) as most classical ones function as is shown in Figure 4-2. The data is generated by the outputs of the FSM and loaded in the shift register. Finally the SER3 output is used to select the logic value trough a logic multiplexer that is a single bit for the RGB LED.

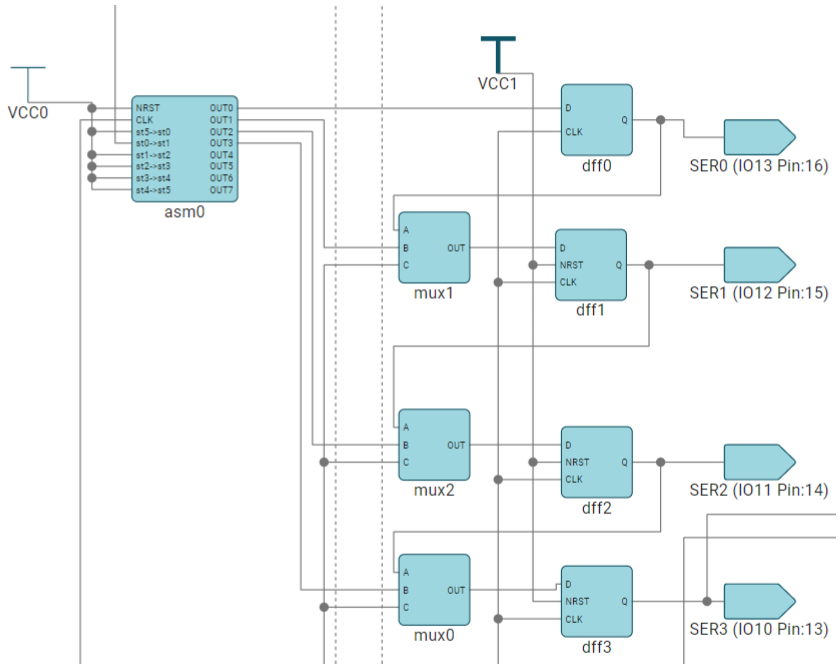

Figure 4-2. FSM and 4-Bit Shift Register

The operation of the state machine and the 4-bit shift register can be seen in Figure 4-3. For a given color represented by the Hexadecimal number 0xC30000 the FSM generates a 4-bit number in each of the clock events of the machine. Simultaneously, a shift register loads internally each new data generated by the FSM and generates a 24 bits serial number that represents a given color. The speed of the shift register is four times the speed of the FSM.

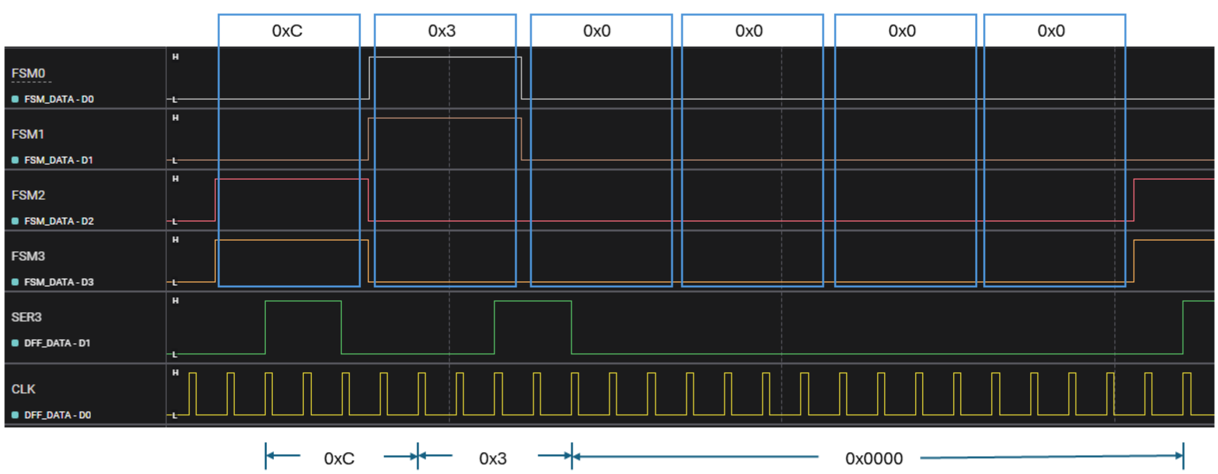

Figure 4-3. Operation of the FSM and the 4-Bit Shift Register

5 TPLD Serial Communications

TPLD2001 includes an I2C serial communication module able to read and write user registers space including the ASM. Access to the ASM is a straightforward procedure consisting of just putting the Serial Communications Element in the design and configuring the I2C peripheral address that is used to talk with the TPLD. Nothing else must be done either with internal electrical connections or additional configurations. The ASM internal addresses are from 0x50 to 0x58, and all the additional details of the FSM can be found in the TPLD2001 datasheet. A change in the color of the RGB LED can be achieved by modifying the value if the FSM registers, so any of the 16.7 million colors can be generated.

Figure 5-1 shows the I2C module and the parameters available. In this example, the I2C address is set to 0x7.

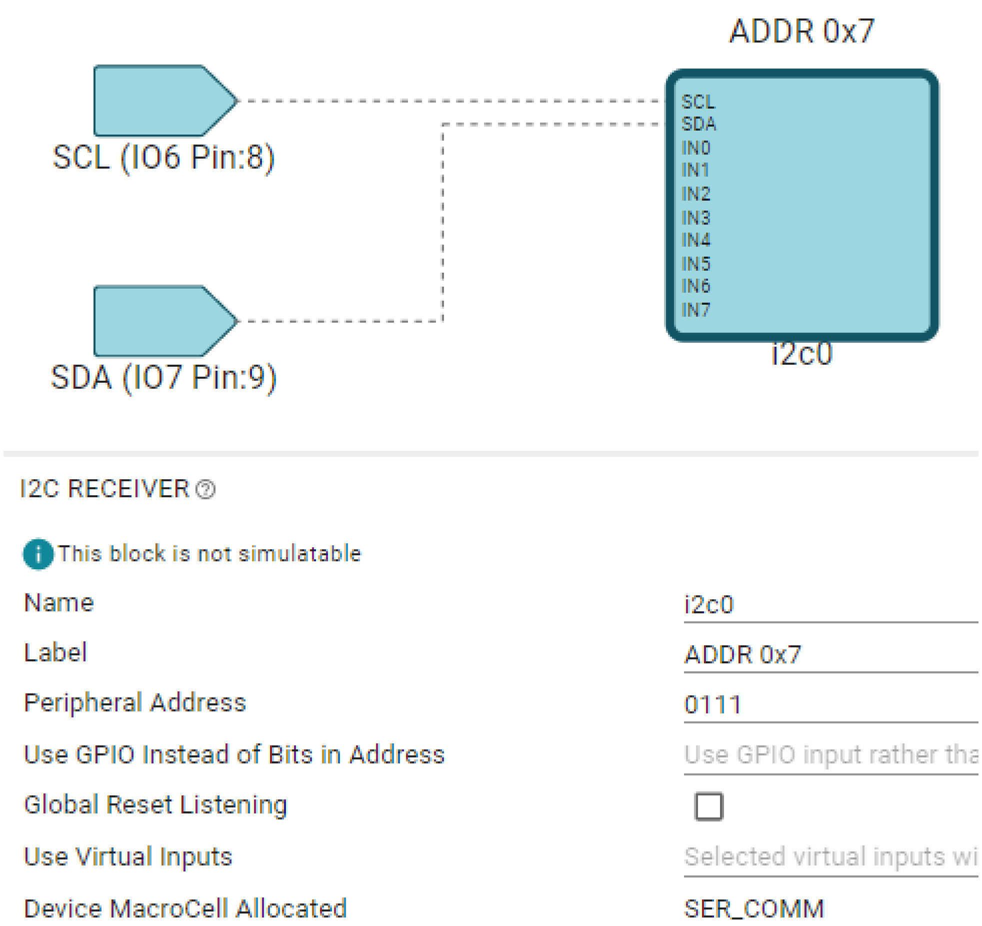

Figure 5-1. I2C Module and Parameters

6 Summary

TPLD2001 can help to generate and translate standard logics values in time-based logic typically used in Smart RGB LEDs. Using multiple elements such as integrated oscillators, D-type flip-flops, counters, delays, general purpose I/Os, and Synchronous Finite State Machines, TPLD can help to integrate complex designs in a single chip design with zero non-recurrent engineering. Moreover, the values of the internal TPLD elements can be updated using standard I2C or SPI communications. Finally, as a design example, a software-less application in a single device design is shown.

7 References

- Texas Instruments, TPLD, product page.
- Texas Instruments, *TPLD2001 Programmable Logic Device with 18-GPIO and Selectable I2C/SPI*, datasheet.
- Texas Instruments, *Using Serial Communications Within TPLD*, application brief.

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