Texas Instruments
XIO2000
EVM Guide

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Document History

Revised by	Date	Document Name	Revision Comments
CSH	9/23/04	XIO2000 EVM Guide – Version 1.00	

1 Overview

The XIO2000 Evaluation Board (EVM) implements a Peripheral Component Interconnect (PCI) Express to PCI bridge circuit using the Texas Instruments XIO2000 PCI Express to PCI Bus Translation Bridge. Designed as an x1 add-in card, it is routed on FR4 as a standard 4-layer (2 signals, 1 power, and 1 ground) board with a 100-Ω differential impedance (50-Ω single-ended) using standard routing guidelines and requirements.[1]

Power for the XIO2000 EVM and any PCI add-in card connected to the EVM is provided or derived from the standard voltages provided on the PCI Express connector. Power for the 3.3-V and 12-V rails is provided directly from the add-in connector, while regulators are present to derive 1.5-V (for the XIO2000) and 5-V and -12-V (for the PCI slots).

Upon request, gerber files for the EVM can be provided that illustrate techniques that achieve fan-out (of the μ*BGA), use of split power planes, placement of filters and other critical components, and methods used to match lengths on PCI and PCI Express signals on a standard 4-layer board.

Schematics and a Bill of Materials are provided to illustrate the design of this particular EVM.

Note: Observe proper ESD procedures when handling the EVM. Failure to observe proper procedures may result in damage either to the EVM or the XIO2000 silicon which may cause the board to malfunction.

[1] As specified in the *PCI Express Electromechanical Specification,* revision 1.0a and the *PCI Local Bus Specification*, revision 2.3

2 EVM Features

2.1 PCI Express Connector

The EVM is designed as a half-width PCI Express add-in card. The card fits into any standard x1, x2, x4, x8, or x16 add-in connector that is compliant with the *PCI Express Electromechanical Specification* revision 1.0a. In addition to the standard transmit-and-receive pairs, the connector must supply 3.3 V, 12 V, $\overline{\text{PERST}}$, a 100-MHz differential clock, and V_{AUX}. The $\overline{\text{WAKE}}$ signal is also supported by the EVM although, as an optional pin, the system is not required to support this signal.

The height of the board is nonstandard due to the presence of PCI slots. Inserting PCI add-in cards into the EVM will, in most cases, prohibit the EVM from being placed in a case. If possible, provide some mechanical support to the EVM. Otherwise, the weight of PCI add-in cards can strain the board in the PCI Express add-in slot and may result in the board making poor contact with the connector. Poor connector contact can lead to signal integrity issues.

2.2 PCI Add-In Slots

The XIO2000 EVM provides three standard PCI add-in slots. While reversible, these slots, as shipped, are keyed as 5-V slots and provide a 5-V VIO clamping voltage that provides accessibility to any 5-V or universally keyed PCI add-in cards. All standard voltages (3.3 V, 5 V, 12 V, and -12 V) are provided through the PCI connectors, enabling standard PCI add-in cards to function without requiring external power.

Cards placed into the PCI add-in slots must be inserted into the slots in accordance with labeling on the EVM. Referencing the component side of the EVM as front and the PCI express edge connector as down, boards must be inserted with the component side of the board down and the mounting bracket to the left of the EVM.

WARNING: Inserting either a 3.3-V card or a universally keyed card into the EVM backwards will damage the EVM and possibly the add-in card as well.

The PCI bus operates at 66 MHz only when 66-MHz-capable PCI add-in cards are placed in the socket. If a 33-MHz card is inserted into the socket, then the XIO2000 detects the presence of the lower speed device and automatically sets the bus speed to 33 MHz. If 66-MHz operation is desired, place no more than two add-in cards into board slots. (This limitation is due to bus loading issues inherent to the PCI specification.) If a third 66-MHz device is added to the bus, signal

integrity may still permit proper functioning of the interface, but such functionality cannot be assured and is beyond the scope of this document.

Two of the reserved pins on the PCI add-in connectors are used to route $\overline{\text{PME}}$ and V_{AUX} to any add-in cards. These assignments, while not part of the *PCI Local Bus Specification*, are used by many in the industry as de facto standards and must not interfere with any add-in cards. If cards are used that use these terminals for other purposes, the following modifications may be made to the EVM to isolate the signals from the PCI add-in connectors:

- $\overline{\text{PME}}$ (routed to reserved terminal A19 on each connector). Remove resistors R55, R53, and R54 (for slots 0, 1, and 2, respectively).
- V_{AUX} (routed to reserved terminal A14 on each connector). Remove resistors R50, R51, and R52 (for slots 0, 1, and 2, respectively).

2.3 EEPROM Interface

Each XIO2000 EVM provides an on-board EEPROM. As shipped, each EEPROM is programmed with values that will allow the EVM to function in most systems. The EEPROM interface is left as programmable (not write-protected) so that EEPROM contents may be modified for testing other optional settings. TI recommends that you do not change the EEPROM values. To change EEPROM contents, use the EEPROM access registers as detailed in the XIO2000 data manual or request the TI EEPROM access tool.

2.4 Test Header

Each XIO2000 EVM provides accessibility to the GPIO pins on the XIO2000. From header J1, all eight GPIOs have external visibility and can be used in any manner consistent with their functionality as detailed in the XIO2000 data manual. All GPIO signals are labeled on the header and are terminated with an on-board pullup resistor.

If the EEPROM interface detailed in the previous section is in use, then GPIO4 and GPIO5 can be configured and used for this purpose. The EEPROM interface can be removed from the XIO2000 by removing resistors R28 and R29. This allows these GPIO pins to be used for another purpose, although any configuration done by the EEPROM will then have to be done in some other fashion. While removing R28 and R29 will physically disconnect the EEPROM from GPIO4/GPIO5, in order to release the pins from this functionality, GPIO5 must be held low at the deassertion of $\overline{\text{PERST}}$. As no pulldown is available for this purpose, the pin must be externally shorted at boot time (deassertion of reset) by shorting J1 pin 8 to J1 pin 11. Once the system has booted, this short may be removed and GPIO4 and GPIO5 will be available for other uses.

Pin 9 on the J1 header is a global reset ($\overline{\text{GRST}}$) for the XIO2000. Driving this pin low will cause all registers and state machines within the XIO2000 to return to a default power-up state. This pin generally must remain disconnected.

Pin 12 is an access point for the $\overline{\text{PME}}$ signal and may be used to externally wire this signal to any PCI add-in card that has the signal available but does not route the signal to pin A19 on the PCI expansion connector.

Pin 2 on the connector is a 3.3-V test point and pin 11 is a ground test point. These signals may be used to externally toggle GPIOs for any required testing.

2.5 $\overline{\text{CLKRUN}}$

The $\overline{\text{CLKRUN}}$ (clock run) signal is a power-saving mechanism (defined in the *PCI Mobile Design Guide*) which functions to stop the PCI bus clock when the bus is idle. Because devices which do not support this protocol are unable to restart the system clock, this feature is disabled by default on the XIO2000 EVM. This feature may be enabled to function with PCI add-in cards that also support this feature.

Enabling $\overline{\text{CLKRUN}}$ requires that resistor R24 be populated with a 0805 form factor 10-kΩ resistor. When this option is populated at the de-assertion of the reset pin, GPIO1 will internally map to $\overline{\text{CLKRUN}}$. When this happens, GPIO1 will be unavailable for other purposes. An external wire must then be connected from GPIO1/$\overline{\text{CLKRUN}}$ (available on J1 pin 2) to all add-in cards being tested with this functionality.

2.6 LEDs

The XIO2000 EVM has LEDs onboard to indicate availability of power and status of certain control signals. The onboard LEDs are as follows:

- D1 – 5-V power indicator
- D2 – 1.5-V (**Note:** this LED will generally not light due to absence of LED with $V_f \leq 1.5$ V)
- D3 – 3.3-V power indicator
- D4 – 12-V power indicator
- D5 – PCI Express $\overline{\text{PERST}}$ indicator (power on, reset asserted)
- D6 – PCI Express $\overline{\text{WAKE}}$ indicator (power on, $\overline{\text{WAKE}}$ asserted)
- D7 – PCI $\overline{\text{PME}}$ indicator (any PCI add-in card that has $\overline{\text{PME}}$ line asserted)

3 FAQ/Troubleshooting

To use the EVM:

1. Plug the PCI add-in cards into the EVM, oriented as indicated on the board
2. Place the EVM into a PCI express add-in slot
3. Turn the system on

From the operating system perspective, the XIO2000 appears to be a standard PCI-to-PCI bridge (PCI header type 1) and the OS will configure the bridge and any devices behind the bridge accordingly using legacy PCI configuration transactions. Following sections of this chapter describe issues that may impair use of the bridge in a system.

3.1 BIOS Fails to Assign Memory Window to Bridge.

Microsoft operating systems generally attempt to respect the resource allocations made by system BIOS. The XIO2000 requires a memory window in order to access some registers used by the device. If the Microsoft OS determines that the BIOS failed to assign a memory window to the XIO2000, it will assume that one cannot be assigned and that the device is nonfunctional. The OS will then assume the bridge is not functional and will not enumerate devices behind the bus. Consequently, these devices will never be configured or assigned resources.

This failure can be determined by examining device manager in the OS. If failure has occurred, the bridge will appear “banged out” and if the bridge properties are examined, the OS will reveal this device cannot find enough free resources .

3.2 x16 slots Only Support $\overline{\text{INTA}}$

As the x16 PCI express add-in slots are designed as a graphics expansion port, many only support a single interrupt ($\overline{\text{INTA}}$), as this is the only interrupt that will be required by a graphics card. The XIO2000 EVM supports all interrupts and balances interrupt loading by rotating the interrupts to each add-in slot as required by the *PCI Local Bus Specification*. Accordingly, any PCI add-in card behind the bridge that asserts an interrupt other than $\overline{\text{INTA}}$ will not be serviced as the interrupt is not supported by the chipset. Consequently, the add-in card will fail. Any devices that do not require interrupts or that only assert $\overline{\text{INTA}}$ (as routed to the specific slot they are placed in) will still function normally.

3.3 System Turns On When PCI Card Is Inserted Into EVM Or When EVM Is Plugged Into Slot

As mentioned previously, $\overline{\text{PME}}$ is routed on the EVM to the various PCI slots through a reserved pin that many PCI add-in cards use for this purpose. On occasion, when a PCI card is inserted into the EVM (while the EVM is plugged into a board), the add-in card may be inserted in such a way as to pull the $\overline{\text{PME}}$ line low on the EVM. When this happens, the XIO2000 sees a PCI device trying to wake the system and will appropriately assert $\overline{\text{WAKE}}$, which may cause the system to turn on.

Similarly, when the EVM is inserted into the slot, V_{AUX} from the connector may not have had enough time to pull the $\overline{\text{PME}}$ line high (as the on-board pullup resistors dictate), yet V_{AUX} may have powered the XIO2000 which now samples $\overline{\text{PME}}$ as low and again wakes the system. This is a limitation of the inability to appropriately power the pullup resistors before the XIO2000 is powered. If this occurs, turn power to the system off and reboot to ensure the EVM receives a clean reset from the system.

3.4 What To Do If EVM Is Not Working

3.4.1 Check EVM Power

Diodes D1, D3, and D4 show the status of the 5-V, 3.3-V, and 12-V rails, respectively. 1.5 V may be probed on the top pad of C44 (directly next to U3), and -12 V may be probed from the bottom pin of C101 (at the top of the board). A ground reference is available at J2 pin 11. If any of these voltages fail, a problem is likely to occur with EVM functionality. The XIO2000 requires 3.3 V and 1.5 V, other voltages are supplied for use by PCI add-in cards, and PCI VIO is by default 5 V (which will cause the entire PCI bus to be clamped to 0.7 V if this voltage is not present). If any of these voltages fail, it is likely that the EVM won't function because:

- The XIO2000 will not be powered
- The add-in card will not be powered
- Neither the XIO2000 or the ads-in card will be powered

All voltages have resettable fuses to prevent overcurrent conditions, so if a particular power rail fails:

1. Detach all devices from the EVM
2. Remove the EVM from the system
3. Wait for 30 minutes before trying again

3.4.2 Check If Bridge Is Link Training

If the system does not boot, remove all PCI add-in cards from EVM and try again. If the system hangs before the OS loads, then probably the system and the EVM are having difficulty completing link training (probably an issue with signal integrity on the differential pairs). If a PCI Express analyzer is unavailable, then try a different express slot or a different system if possible. Re-check the 1.5-V rail and examine the differential clock on an oscilloscope to ensure it is clean.

If link training successfully completes, the system will boot and the XIO2000 will appear in the device manager. If the bridge does not appear in the device manager, then the system may not have detected the presence of the bridge, perform the previous checks again.

Also, if the PCI add-in cards have enough weight and there is no mechanical support, the EVM may flex and some components may crack or become disconnected. Check the coupling capacitors on the EVM transmit lines (C40 and C41). These 0.1-μF 0402 components have a tendency to crack if enough weight is put on the board; they will need to be replaced if they are damaged.

3.4.3 Check If Bridge Has Been Configured

Once the bridge is communicating with the system, the BIOS and/or the OS are expected to configure the bridge for proper operation. As the bridge appears to software to be a standard PCI-to-PCI bridge, most existing BIOS and OS software must be capable of configuring the bridge with no special considerations for PCI Express. In addition to the memory window the bridge requests for internal resources, the following items are required for bridge operation:

- Command register – PCI offset 0x4 : The bus master enable (bit 2), memory enable (bit 1), and I/O enable (bit 0) must be set to enable the bridge to send upstream transactions.

- Cache line size register – PCI offset 0xC : Must be set to the cache line size for the system. Failure to set this bit will not cause the bridge to fail but will cause the bridge to limit all upstream transactions to 1 DWord.

- Primary, secondary, and subordinate bus numbers – PCI offsets 0x18, 0x19, and 0x1A : The bridge must have the bus numbers configured so that it can determine which transactions are targeting the bridge, which transactions are targeting devices directly attached to the bridge, and which transactions are farther downstream from the bridge.

- I/O base and limit registers and I/O base upper 16 bits and I/O limit upper 16 bits registers – PCI offsets 0x1C, 0x1D, 0x30 and 0x32: If any devices downstream from the bridge require I/O resources, the bridge must be programmed with a window that contains the I/O resources of all devices

downstream. Failure to program these windows will cause the bridge to respond to I/O transactions with a response of Unsupported Request. Any transactions initiated on the secondary side of the bus that fall within this range will not be claimed by the bridge. The I/O window for the XIO2000 has a minimum size of 4 KBytes and is naturally 4K-aligned. Typically, most systems use only 16-bit addressing for I/O transactions, so the upper base and limit registers remain 0.

- Memory base and memory limit registers – PCI offsets 0x20 and 0x22 : Similar to the I/O base and limit registers, the bridge must be programmed with a memory address window containing the nonprefetchable memory resources of all downstream PCI devices requiring nonprefetchable memory. Memory windows have a minimum size of 1 MByte and are naturally 1M-aligned. The bridge does not claim either a memory transaction initiated from upstream that does not fall within its memory window nor memory transactions initiated downstream that do fall within its memory window.

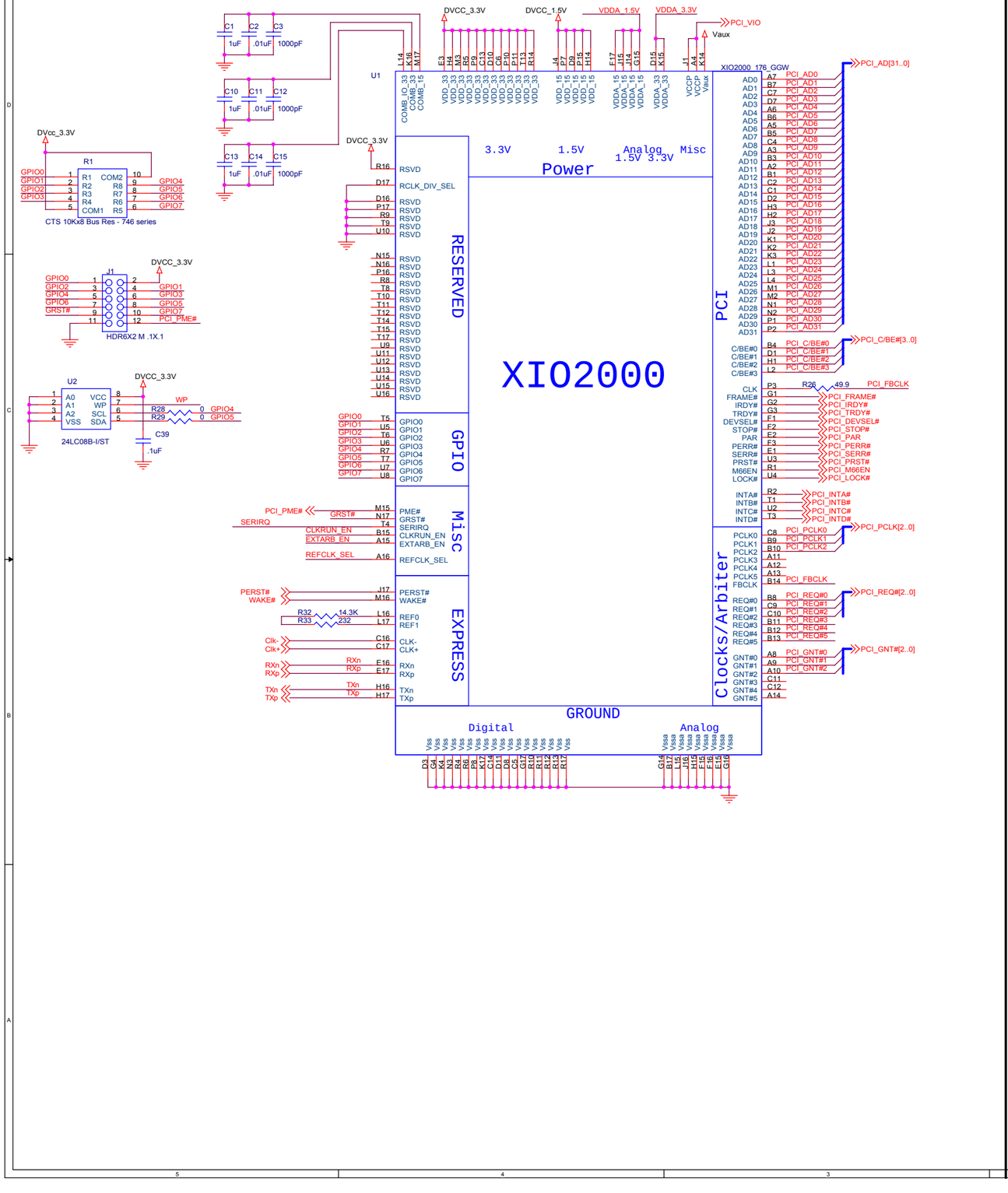
- Prefetchable memory base, prefetchable memory limit, prefetchable base upper 32-bit, and prefetchable limit upper 32-bit registers – PCI offsets 0x24, 0x26, 0x28, and 0x2C : Identical to the memory base and limit registers but for prefetchable memory resources.

Depending on desired functionality, other PCI registers on the XIO2000 may have to be configured. Consult the XIO2000 data manual for a description of the previous registers, or for any other XIO2000 registers.

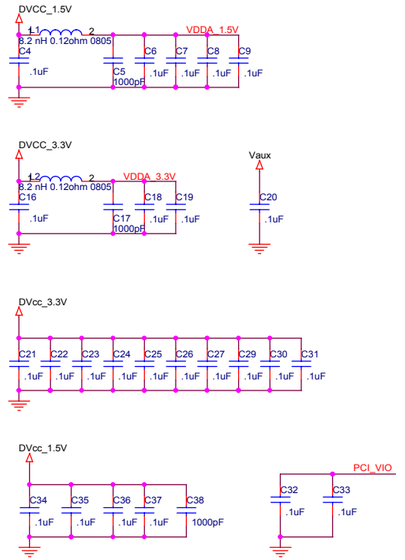
3.4.4 Check Devices Downstream From Bridge

Once the bridge is communicating and is properly configured, check if devices downstream from the bridge have been configured as required. Check the Windows Device Manager to determine if the device drivers have been loaded or if other problems exist with the device. Once you have performed these checks, you can perform PCI transactions on the bus and examine them with any standard PCI analyzer.

4 EVM Schematics

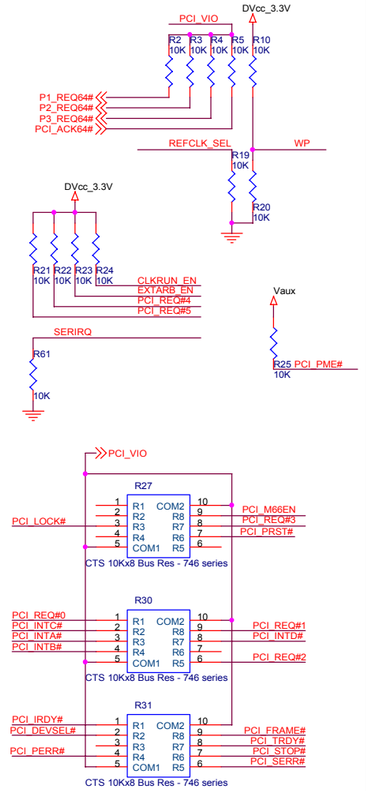


Bridge Power Filtering/Decoupling



NOTE: C38 should go directly under the pin H14 on U1

Pull Ups/Pull Downs



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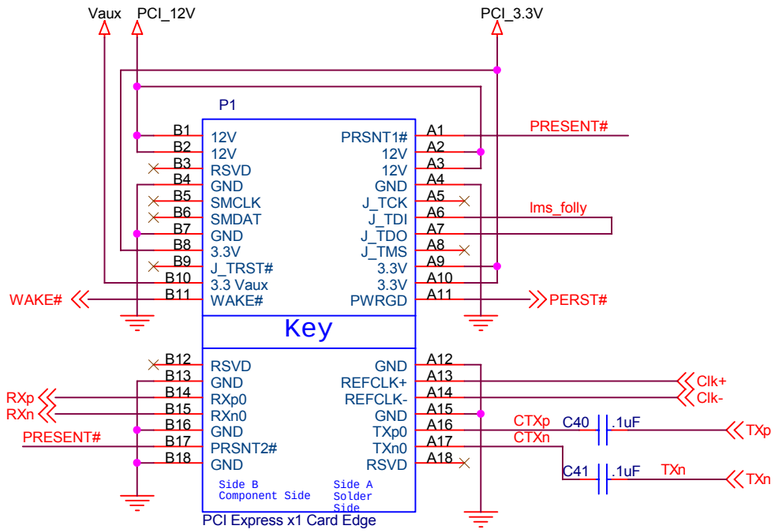
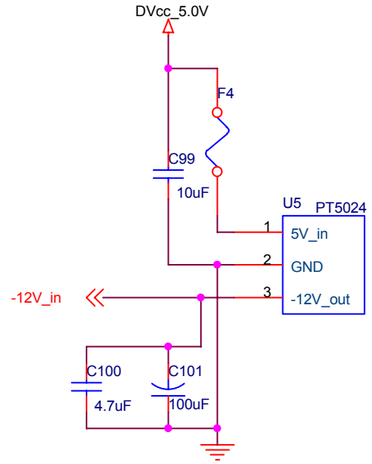
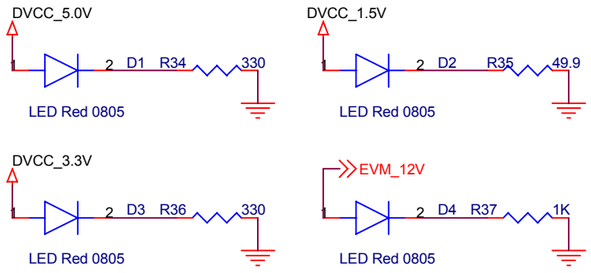
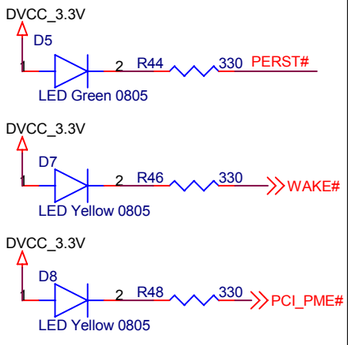


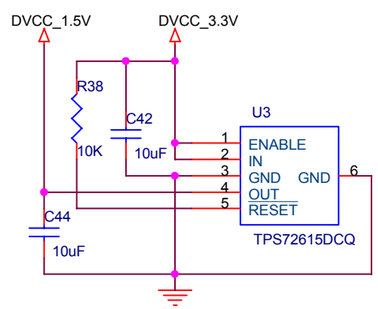


LEDs





Power



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5 EVM Bill of Materials

Evaluation board bill of materials as assembled. Unused options (e.g., 3.3-V VIO) are not populated and not listed.

Item	Qty	Reference	Part	Manufacturer	Part #	Package	Tolerance
1	3	C1, C10, C13	1-µF capacitor			402	10%
2	3	C2, C11, C14	0.01-µF capacitor			402	10%
3	4	C3, C12, C15, C38	1000-pF capacitor			402	10%
4	2	C4, C16	0.1-µF capacitor			805	10%
5	2	C17, C5	1000-pF capacitor			805	10%
6	74	C6, C7, C8, C9, C18,	0.1-µF capacitor			402	10%
		C19, C20, C21, C22,					
		C23, C24, C25, C26,					
		C27, C29, C30, C31,					
		C32, C33, C34, C35,					
		C36, C37, C39, C40,					
		C41, C51, C52, C53,					
		C54, C55, C56, C57,					
		C58, C59, C60, C61,					
		C62, C63, C64, C65,					
		C66, C67, C68, C69,					
		C70, C71, C72, C73,					
		C74, C75, C76, C77,					
		C78, C79, C80, C81,					
		C82, C83, C84, C85,					
		C86, C87, C88, C89,					
		C90, C91, C92, C93,					
		C94, C95, C96, C97,					
		C98					
7	4	C42, C44, C50, C99	10-µF capacitor			805	10%
8	1	C43	100-µF capacitor			1812	10%
9	3	C45, C48, C49	22-µF capacitor			6032	10%
10	2	C47, C46	0.047-µF capacitor			1206	10%
11	1	C101	100-µF capacitor			Radial	20%
12	4	D1, D2, D3, D4	LED Red 0805	Lumex	SML_LX0805SRC	805	
13	1	D5	LED Green 0805	Lumex	SML_LX0805GC	805	
14	1	D6	Diode - Schottky	Diodes Inc.	MBRD835L-T		
15	2	D7, D8	LED Yellow 0805	Lumex	SML_LX0805YC	805	
16	4	F1, F2, F3, F4	SMD250 Fuse	RAYCHEM	SMD250		
17	1	J1	HDR6X2 M .1X.1	AMP	103322-6		
18	2	L2, L1	8.2 nH 0.12 Ω 0805	AVX	L08058R2DEWTR	805	
19	1	L3	10 uH	Coiltronics	UP4B-100		

Item	Qty	Reference	Part	Manufacturer	Part #	Package	Tolerance
21	3	P2, P3, P4	PCI Connector	AMP	145098-1		
22	4	R1, R27, R30, R31	10kx8 Bused resistor	CTS	746X101103J		
23	11	R2, R3, R4, R5, R19,	10-kΩ resistor			805	10%
		R20, R21, R22, R25,					
		R38, R61					
24	2	R35, R26	49.9-Ω resistor			402	10%
25	2	R28, R29	0-Ω resistor			402	5%
26	1	R32	14.3-kΩ resistor			805	1%
27	1	R33	232-Ω resistor			805	1%
28	5	R34, R36, R44, R46,	330-Ω resistor			402	10%
		R48					
29	1	R37	1-kΩ resistor			402	10%
30	1	R45	18.7-kΩ resistor			805	1%
31	1	R47	6.19-kΩ resistor			805	1%
32	1	R49	2-kΩ resistor			805	10%
33	7	R50, R51, R52, R53,	0-Ω resistor			805	5%
		R54, R55, R57					
35	3	R58, R59, R60	100-Ω resistor			805	5%
36	1	U1	XIO2000_176_GGW	Texas Instruments	XIO2000	176 pin GGW	
37	1	U2	EEPROM	Microchip	24LC08B-IST	8-pin TSSOP	
38	1	U3	1.5-V regulator	Texas Instruments	TPS72615	6 pin DCQ	
39	1	U4	5-V step-up regulator	Linear Technology	LT1370CR	R package	
40	1	U5	5-V to -12-V regulator	Texas Instruments	PT5024C		
41	1	C100	4.7-μF capacitor			1812	10%

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