JTAG-Compatible Devices Simplify Board-Level Design for Testability

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Introduction

A specification for an integrated circuit (IC) test bus and boundary scan architecture has been developed by the Joint Test Action Group (JTAG).[1,2] This specification has been endorsed by the IEEE 1149 Standards Committee. This testability standard, referred to as IEEE 1149.1, promises to significantly improve IC and board level testing.[3,4,5] However, before the industry truly can evaluate the benefits of 1149.1, hardware components supporting the standard must be made available.

Texas Instruments (TI), a participant in the development of the JTAG standard specification, has taken an active role in producing 1149.1-compatible devices required to implement the standard. These devices are members of TI's System Controllability, Observability, and Partitioning Environment (SCOPE) family of testability products. While all SCOPE products conform to 1149.1, some include extensions to improve the ability to perform scan and test operations further at the IC through system levels. The SCOPE products previewed in this paper include an 1149.1 Test Bus Controller (TBC) IC, scan path support IC, a series of SCOPE octal ICs, and a Digital Bus Monitor (DBM) IC. While products presented in this paper are described in detail, the exact implementation and/or operation are subject to change.

Elements of an 1149.1-Based Design

When implementing 1149.1 into a product, designers must have access to a range of test hardware building blocks. Application-Specific Integrated Circuit (ASIC) designers need a library of test cells to implement 1149.1 efficiently at the IC level. Similarly, board and system designers need a variety of off-the-shelf test components to implement 1149.1 at higher levels of assembly. While SCOPE provides both ASIC cells and standard components supporting 1149.1, the latter is the subject of this paper.[6,7] The SCOPE products presented in this paper fall under two categories: products supporting the design of system scan path architectures (TBC and scan path support ICs), and products supporting board-level design for testability (test octals and DBM ICs).

SCOPE Test Bus Controller (TBC) IC

One of the key features provided by the 1149.1 standard is a common IC-level serial testability bus. This four-wire test bus forms the common thread through which different merchant ICs may be linked together at the board level to effect testing. With the realization of a standard IC-level test bus, a need has arisen to develop test bus controller ICs to support efficient transfer of serial data and control to and from target devices on the serial test bus.[8]

Figure 1 shows an example application of the TBC. The TBC provides the hardware link between a host processor and target devices on the serial scan path. To the processor, the TBC is a peripheral mapped into a particular area of the processor's external memory space. The TBC operates to transfer data and control between the parallel processor and target devices on the serial test bus. The TBC's processor interface consists of a 16-bit-wide bidirectional data bus; inputs for address, read/write, and chip select signals; and an interrupt output signal.

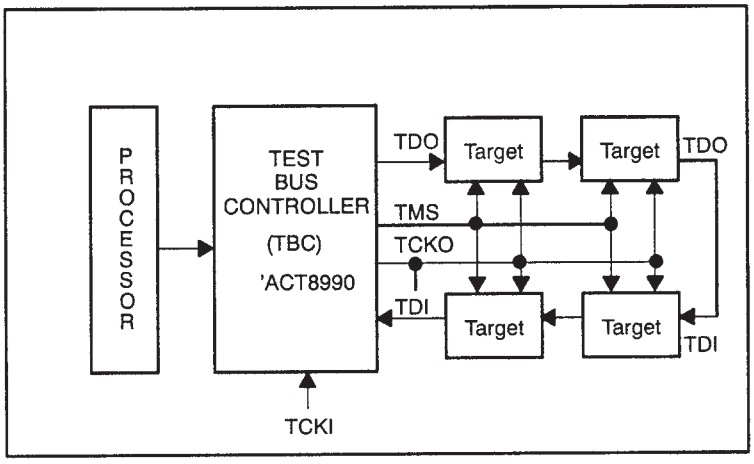

Figure 1. Test Bus Controller Example

The TBC's test bus interface consists of a Test Data Output (TDO), Test Data Input (TDI), Test Mode Select (TMS) outputs, and a Test Clock Input (TCKI), and Test Clock Output (TCKO). The TMS outputs allow the TBC to support separate scan paths. TDO is a serial-data output from the TBC that drives the TDI input of the first target device in the scan path. TDI is a serial-data input to the TBC that receives the TDO output from the last target device in the scan path. The TMS signals are serial control outputs from the TBC that drive TMS inputs of target devices in the scan path. The TMS output from the TBC conforms to the protocol described in the 1149.1 standard to cause target devices on the scan path to shift data from their TDI input to their TDO output. The TCKI signal is generated externally and is input to the TBC, and is distributed via TCKO to each target device on the scan path. In addition to the required 1149.1 test bus signals, the TBC interface includes an output signal for initialization of target devices and input signals for receiving test-related interrupts from target devices.

Before a scan operation, the TBC receives the parallel data input from the processor that is to be transmitted serially to the target devices in the scan path. Also, the processor inputs a count value into an internal TBC counter, specifying the number of serial data bits to be transferred. After the data and count values have been set up, the TBC receives a command from the processor to initiate the scan operation. During scan operations, the TBC outputs serial data and control signals to the target devices via the TDO and TMS output signals and receives serial data from the target devices via the TDI input signal. By reading status bits from the TBC, the processor determines when the TBC requires additional read and write operations to maintain the flow of serial data to the target devices in the scan path. When the TBC's internal counter reaches a minimum value, the TBC outputs an interrupt to the processor, indicating that the required number of serial data bits has been shifted through the scan path.

In addition to controlling scan operations, the TBC simplifies the execution of Built-In Self-Test (BIST) features incorporated in the target device shown in Figure 1. The 1149.1 test bus protocol state diagram includes a steady state, referred to as run test/idle, in which BIST operations may be executed. If a target device includes a BIST capability, an instruction invoking the BIST operation can be scanned into the device. After the target device receives the BIST instruction, execution of the test occurs when the TBC transitions the test bus into the run test/idle state. As described in the 1149.1 specification, the length of a BIST operation is defined by a number of TCK inputs applied while the test bus is in the run test/idle state.

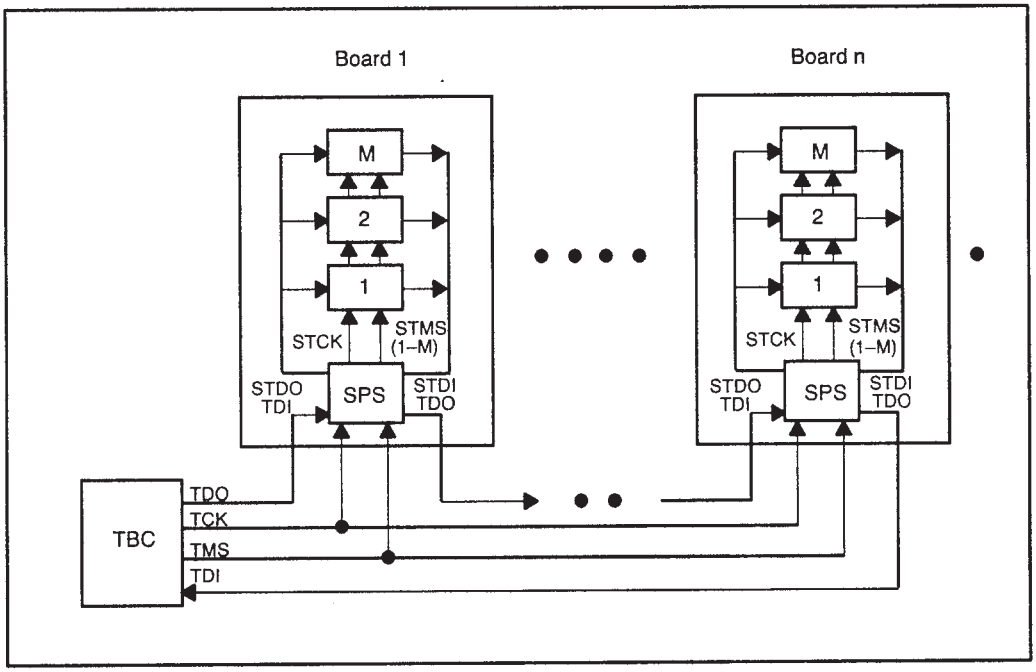

Figure 2. Scan Path Selector Example

To simplify the execution of 1149.1 BIST operations, the TBC contains two types of run test commands. Both command types are executed while the test bus is in the run test/idle state. The first type of run test command uses the TBC's internal counter to count the number of TCKs applied while the test bus is in the run test/idle state, supporting the BIST procedure detailed in the 1149.1 specification. When the counter reaches a minimum value, the TBC transitions the test bus from the run test/idle state into either a scan or pause state to terminate the execution of the BIST operation. The second type of run test command uses the TBC's interrupt inputs to determine the length of time the test bus is in the run test/idle state. This command differs from the first in that it assumes the target devices have additional test pins from which an end-of-test interrupt may be issued to the TBC. When the TBC receives an end-of-test interrupt, the TBC transitions the test bus from the run test/idle state to either a scan or pause state to terminate the execution of the BIST operation.

TBC ICs will be available in 44-pin PLCC (Plastic Leadless Chip Carrier). The TBC supports a maximum scan rate of 30 MHz. At higher scan rates, the TBC may require pausing the test bus for the processor to load and unload data. In addition to its 1149.1 capabilities, the TBC also supports the test interface required for in-circuit emulation of TI's microprocessor ICs.

SCOPE Scan Path Selector (SPS) IC

The SPS IC is a first in the series of devices that simplify the design of system-level scan path architectures. The SPS IC provides programmable scan access to multiple boards in a system design. It selectively routes the test bus through different scan path channels without requiring the use of multiple TMS control signals.

As shown in Figure 2, the SPS IC provides a method of coupling and decoupling board-level secondary scan paths to a primary scan path. The primary scan path is defined as the system scan path directly coupled to the TBC IC or other test bus-controlling source. The secondary scan path is defined as one or more selectable board-level scan paths directly coupled to the SPS IC. In some instances, an SPS may be considered a test-controlling source if it issues control to another SPS residing in one of its selectable secondary scan paths. In this case, the scan path output from the controlling SPS is considered a primary scan path, and the scan path output of the SPS being controlled is considered a secondary scan path. This scenario can be replicated to create a vertical, as well as a horizontal, hierarchy of primary and secondary scan path networks throughout a system scan path architecture.

As shown in Figure 2, SPS ICs existing on a primary scan path can be set by the TBC to select one of the board-level secondary scan paths (1-M), or bypass the board scan paths entirely.

The ability to select or deselect secondary scan paths onto the primary scan path allows optimizing the length of the primary scan path to suit a particular test operation. Being able to traverse a system-level primary scan path configuration in the shortest possible time reduces the overall test time of the system and lowers the system test and maintenance cost.

In Figure 2, if a board scan path is selected, the primary scan path is input to the SPS via the TDI input, then passes through the SPS to be output to a selected board scan path via the Secondary TDO (STDO) output. The scan path passes through the selected board scan path and is input to the SPS via the Secondary TDI input (STDI), then passes through the SPS to be output onto the primary test bus via the TDO output. If a board scan path is not selected, the primary scan path enters the SPS via the TDI input, then passes through the SPS and is output on the primary scan path via the TDO output.

Figure 3 illustrates the advantages of using SPS ICs to select or deselect secondary scan paths over another technique that achieves the same goal. In Figure 3, a TBC is shown connected to "n" board designs, with each board, in turn, having "M" selectable scan paths. To gain access to one of the scan paths (1, 2, . . . M) in each board design (1, 2, . . . n), the TBC must have a number of TMS output signals equal to the sum of the total scan paths of each board in the system, i.e., the number of TMS output signals equals ($M_1 + M_2 + M_3 + \ldots M_n$). For example, if a system has 20 boards, with each board having five individually selectable scan paths, the total number of TMS output signals required from the TBC would take up 100 of the IC's package pins. To make matters worse, the number of interface signals to perform scan access to each board would require a test interface cable and connector bus width of 103 wires, 100 for the TMS signals and three for the TCK, TDI, and TDO signals.

By using the SPS IC to design the system scan path architecture, as shown in Figure 2, a TBC with only a single TMS output signal can gain individual access to each scan path (1, 2, . . . M) of each board design (1, 2, . . . n) in the system. This is possible because the SPS IC contains control circuitry and internal switches that respond to a command input from the TBC to couple the primary TMS input signal to a selected board scan path via one of the SPS IC's Secondary TMS (STMS) output signals, (1, 2, . . . M). This results in a scan path selection system equal in flexibility and operation to the one shown in Figure 3, while requiring only a single primary TMS output signal from the TBC IC. This capability allows a sophisticated system scan path architecture to be supported by the minimum 1149.1 four-wire test bus and related cabling and connector interconnections.

In addition to its ability to maintain a minimum test interface to the system being tested, the SPS provides the basis for an inherently fault-tolerant scan path network. In Figure 2, the SPS IC buffers all signals between the primary and selectable secondary scan paths. This buffering action isolates faults in one or more of the secondary scan paths that could have an adverse effect on the primary scan path. For example, in Figure 2, if an open-circuit or short-to-ground fault condition were to occur on any of the SPS's secondary scan path output signals (STMS, STCK, STDI, or STDO), the shifting of serial data into the secondary scan path would be inhibited. Faults of this nature could be tolerated until repaired by simply deselecting the faulty board from the primary scan path so that the primary scan path only passes through the SPS from the primary TDI input to the primary TDO output. In this way, a faulty section in a system scan path network can be bypassed effectively to maintain access to other scan paths in the system. In the example scan path select scheme shown in Figure 3, a board-level scan path short- or open-circuit fault would disable the operation of the entire system scan path network since no means of bypassing a board is available.

The SPS IC will be available in 28-pin DIP and SOIC, or 28-pin LCC. The SPS includes an 8-bit bidirectional data base that serves as both a board identification input and communications port between a board resident test processor and the TBC. A second device is the Scan Path Linker (SPL). The SPL is similar to the SPS, except that the SPL can select any of the four secondary scan paths together.

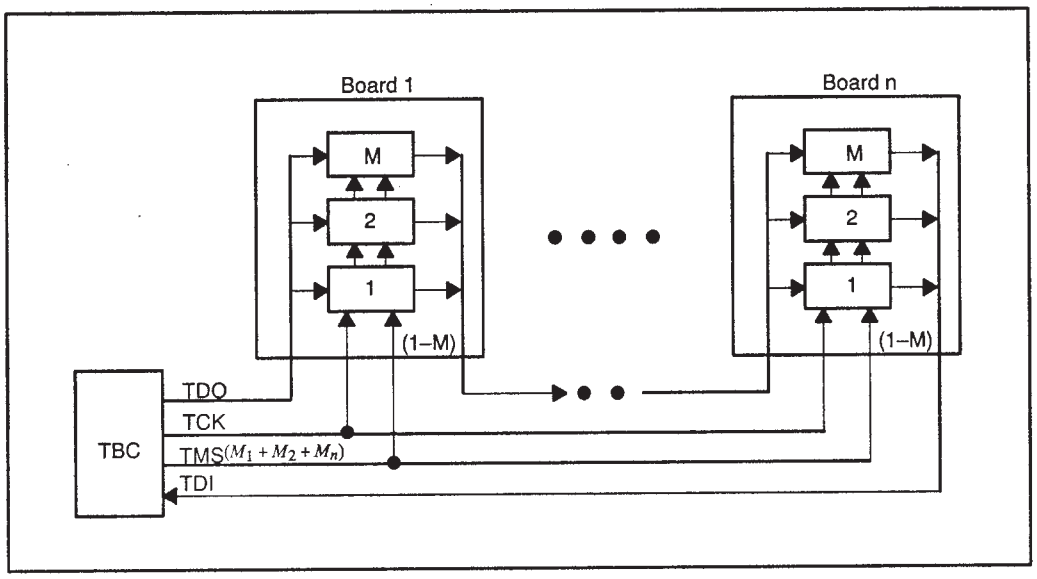

Figure 3. Alternate Scan Path Configuration Example

SCOPE Octal ICs

The SCOPE octals are the first in a series of standard components to be offered by TI that blend functionality with embedded board-level testing features.[9] The initial products include an octal register type 374, latch type 373, buffer type 244, and transceiver type 245. Along with the normal function pins associated with each part, four pins are added to support the 1149.1 test bus interface signals: TDI, TMS, TCK, and TDO. These devices can be substituted for their nontesting counterparts in a variety of board-level design applications such as pipeline registers, board I/O buffers, address and data buffers/transceivers, and finite state machine designs.[10]

An architectural illustration of the 374 octal register type is shown in Figure 4. The functional architecture of the 374 octal consists of an 8-bit register (REG), 8 data inputs (IN), 8 data outputs (OUT), a clock input (CK), and an tristate output control input (OC). The 1149.1 architecture consists of a Test Access Port (TAP) controller, an instruction register (IREG), and a data register section. The data register section consists of a bypass register, a Boundary Control Register (BCR), and a boundary scan register. The boundary scan register consists of SCOPE test cells 1 and 2 (TC1, TC2) coupled to the CK and OC inputs, SCOPE test cell register 1 (TCR1) coupled to the IN inputs, and SCOPE test cell register 2 (TCR2) coupled to the OUT outputs. The other SCOPE octals have a similar 1149.1 test architecture placed around buffer, transceiver, and latch functions.

The TAP controller receives external input from the TMS and TCK signals and outputs internal control to either the IREG or a selected data register, causing a shift operation from the TDI input to the TDO output. The IREG stores a test instruction to be executed by the IC. The bypass register shortens the scan path length through the IC to a single bit during data register operations. The BCR stores boundary configuration control bits to extend the test capabilities of the boundary scan register. The boundary scan register provides the mandatory test features required for 1149.1 compatibility, as well as extended test features developed for SCOPE products.

Normal Mode Operation

During normal operation, the boundary scan register is transparent, allowing input and output signals to pass freely through the test cells and enabling the device to perform its intended function. While in normal operation, the TAP can receive control from the TMS and TCK inputs to shift data through the device from the TDI input to the TDO output. Three test instructions can be executed while the device is in normal mode: 1149.1 sample and bypass instructions and a SCOPE cell self-test instruction. The sample instruction allows the data flowing through the boundary to be sampled and then shifted out for inspection. The bypass instruction selects the bypass register to be shifted during data register scan operations, reducing the scan path length through the device to 1 bit. The self-test instruction executes a self-check of each SCOPE cell in the boundary scan register. While the sample instruction at first may appear very attractive, the user of these

and other 1149.1-compatible devices must know when to sample to obtain meaningful data.

Test Mode Operation

When placed in an off-line test mode, the normal operation of the SCOPE octal is inhibited. In test mode, instructions can be input to the device to perform all mandatory 1149.1 instructions, as well as an extended set of test instructions designed for SCOPE products. The test mode instructions incorporated into all SCOPE octals are described below. Before loading these test mode instructions, the boundary scan path should be set so that a desired first test control pattern is applied to the REG inputs, tristate buffers, and device outputs (OUT). This procedure ensures that the device will be in a known state when the test mode is entered.

When either an external or internal 1149.1 boundary scan test (EXTEST or INTEST) instruction is input to the device, the boundary scan register is set to allow simultaneous observation of signals input to the test cells and control of signals output from the test cells. Simultaneous control and observation is achieved by the design of the SCOPE cells. Each SCOPE cell contains two memories (flip-flops), one to observe input data and the other to control output data. During EXTEST or INTEST the TAP receives external input causing the boundary scan register to capture data on the CK, OC, IN, and REG output signals. After the data are captured, the TAP receives input to shift the captured data out via the TDO output. While captured data are shifted out, the next test control pattern to be applied from the boundary scan register is shifted in via the TDI input. The outputs from the boundary scan register are not allowed to change until the shift operation is complete and the TAP receives input to apply a new test control pattern from the boundary scan register outputs. This procedure of capturing input data, shifting the boundary scan path to extract captured data and load new test control data, followed by applying the new test control data from the boundary scan register outputs, is repeated a required number of times to perform an EXTEST or INTEST operation.

When a tristate and bypass (TRIBYP) test instruction is input to the device, the outputs are placed in a high-impedance state. This instruction is designed primarily to facilitate a blend of in-circuit and boundary scan testing. By disabling the outputs of the device, an in-circuit tester can drive the inputs of another device coupled to the outputs of the octals without damaging the octal's output buffers. While this instruction is in effect, the bypass register is selected to provide a minimum data register scan length through the device.

When a set and bypass (SETBYP) test instruction is input to the device, the boundary outputs are set to a prescanned combination of logic 1's and 0's. This instruction allows the boundary test cells to output a prescanned control pattern to the REG inputs, tristate buffers, and device outputs (OUT). The SETBYP instruction allows placing the octal device in a preferred static input and output state while testing of neighboring components is being performed. While this instruction is in effect, the bypass register is selected to provide a minimum data register scan length through the device.

To support a boundary BIST approach, a run boundary test in test mode (RBTTM) instruction was developed for SCOPE devices. The RBTTM instruction executes the boundary BIST operation setup by control-bit settings in the BCR of Figure 4. The control bits in the BCR must be set before inputting the RBTTM instruction. The four types of RBTTM instructions included in the SCOPE octal devices are 16-bit Parallel Signature Analysis (PSA) of the IN inputs, 16-bit Pseudo-Random Pattern Generation (PRPG) from the OUT outputs, simultaneous PSA of IN inputs and PRPG of OUT outputs, and simultaneous sample of IN inputs and toggle of OUT outputs.

During the 16-bit PSA RBTTM instruction, the 8-bit TCR1 and TCR2 boundary sections are linked to form a single 16-bit Linear Feedback Shift Register (LFSR). The parallel inputs to TCR1 are enabled to accept data from the IN bus, and the parallel inputs to TCR2 are disabled. In this configuration, TCR2 acts as an 8-bit LFSR extension to TCR1. During test, the parallel inputs from the IN bus are compressed into the 16-bit LFSR on the rising edge of TCK. Linking TCR1 to TCR2 allows the SCOPE octal to receive an extended sequence of 8-bit patterns from the IN bus. At the end of the PSA operation, the 16-bit signature can be shifted out of TCR1 and TCR2 for inspection. While TCR1 and TCR2 are collecting the signature, the outputs of TC1 and TC2 remain in their present state. TC2 can be set to enable or disable the OUT buffers during the test.

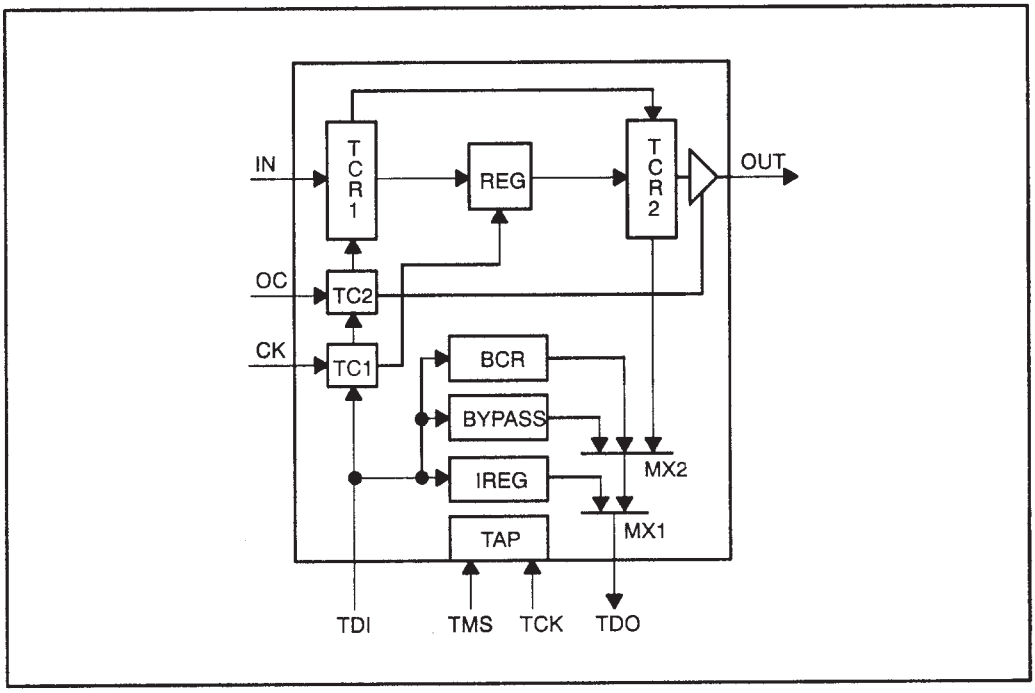

Figure 4. SCOPE Octal Architecture

During the 16-bit PRPG RBTTM instruction, the 8-bit TCR1 and TCR2 boundary sections are linked to form a 16-bit LFSR, as described in the 16-bit PSA test. During the 16-bit PRPG test operation, both parallel inputs to TCR1 and TCR2 are disabled so that both act only as LFSRs. During test, the parallel output from TCR2 drives pseudorandom patterns to the OUT bus on each falling edge of TCK. By linking TCR1 and TCR2, an extended set of pseudorandom pattern sequences is produced. Since the width of the OUT bus is 8 bits, individual patterns will be repeated during every 256-pattern output sequence. However, the test circuit will produce 256 sets of unique 256-pattern output sequences. During this test, TC2 must be set to enable the OUT buffers.

During the simultaneous PSA and PRPG RBTTM instruction, TCR1 and TCR2 operate as two separate 8-bit LFSRs. The parallel inputs to TCR1 are enabled to accept data from the IN bus, and the parallel inputs to TCR2 are disabled. During test, TCR2 outputs pseudorandom patterns to the OUT bus on the falling edge of TCK and TCR1 compresses input data from the IN bus on the rising edge of TCK. Combinational logic residing in the external path between the OUT and IN buses can be tested quickly using this instruction. During this test, TC2 must be set to enable the OUT buffers.

During the simultaneous sample and toggle RBTTM instruction, TCR2 outputs alternating data patterns to the OUT bus on the falling edge of TCK, and TCR1 accepts data input from the IN bus on the rising edge of TCK. By adjusting the frequency of the TCK, this test can be used to measure propagation delays through external logic residing between the OUT and IN buses. During this test, TC2 must be set to enable the OUT buffers.

SCOPE octal ICs will be available in 24-pin DIP and SOIC (Small Outline Integrated Circuit) or 28-pin LCC packages. The parts are designed in bipolar complementary metal-oxide semiconductor (BiCMOS) technology and provide 48/64 mA source/sink output buffers. The functional performance of the SCOPE octals approach 74F speeds, and the maximum scan and BIST clock rate is 20 MHz.

SCOPE Digital Bus Monitor (DBM) IC

To extend board-level testing, a Digital Bus Monitor (DBM) IC is being designed. The DBM can be included in board designs to provide a method of monitoring embedded digital signal paths between ICs. The DBM is capable of monitoring digital signal paths while the board circuitry is either on-line and operating normally or is in an off-line test mode. The benefit of on-line monitoring is that it can be used to reveal timing-sensitive and/or intermittent failures that are otherwise undetectable without the use of external test equipment and mechanical probing fixtures.

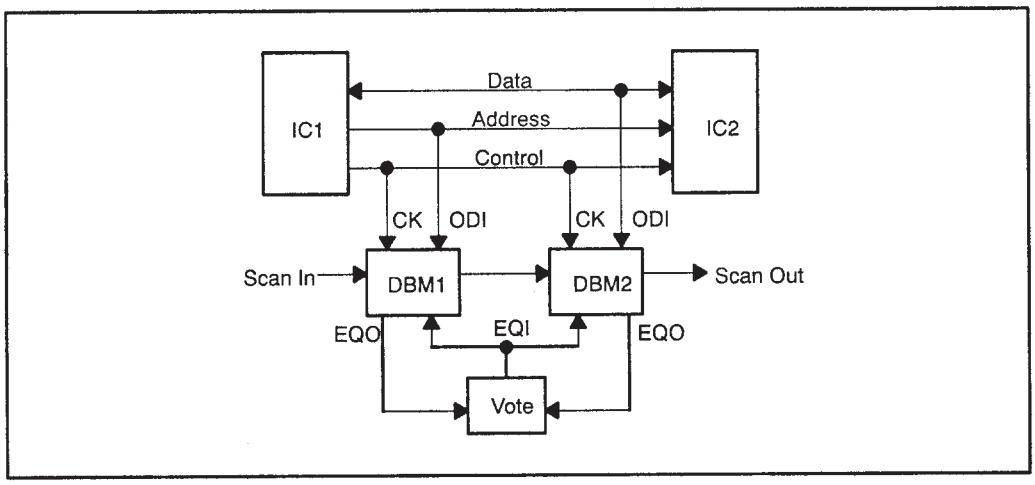

Figure 5. Digital Bus Monitor Example

One of the advantages in using DBMs to construct board-level BIST structures is that the monitoring capability is embedded in the board design and can be used throughout the life cycle of the board production test, system integration, system test, real-time diagnostics, and field support and maintenance. Another advantage in using DBMs is that it does not significantly impact the performance of the board circuitry. Since the signals to be monitored do not pass through the DBM but are only input to the DBM, no significant performance penalty is paid when using these devices.

In the example DBM application shown in Figure 5, two ICs operate together via address, data, and control interface paths to perform a desired function. In normal operation, IC1outputs address and control to IC2 to pass data between the two ICs. DBMs 1 and 2 are included in the circuit for address and data bus monitoring. The DBMs are connected via the 1149.1 four-wire scan bus and the SCOPE two-wire event qualification bus. The address and data bus signals to be monitored are input to the DBMs via observability data inputs (ODIs). The control outputs from IC1 are input to the DBMs via clock inputs (CK) to allow the DBM to operate synchronous with the circuit during on-line monitoring.

The test circuitry residing behind the ODI input pins consists of a Random-Access Memory (RAM) buffer, and a test cell register. The memory buffer provides storage for multiple ODI input patterns. The test cell register operates as either an 1149.1 boundary scan register or PSA register. The memory buffer and test-cell register can be operated together or separately, as required for a particular test operation. The ODI inputs to the test-cell register can be masked individually to allow diagnosing which input or groups of inputs caused a multiple-input PSA operation to fail.

When the circuit in Figure 5 is placed in an off-line test mode, IC1 can be made to output data on its address and data bus. The data and address output from IC1 can be stored into DBM1 and DBM2, respectively, via ODI inputs. After the data have been stored, they can be shifted out for inspection via the 1149.1 scan path. Similarly, IC2 can be made to output data on its data bus, to be stored and shifted out for inspection by DBM2. In the off-line test mode, control to store data and operate the scan path is input via the 1149.1 test bus.

When the circuit shown in Figure 5 is on-line and functioning normally, the DBMs can continue to monitor the data and address bus paths using an internal Event Qualification Module (EQM) resident in each DBM IC. During on-line monitoring, the EQM outputs control to store the data appearing on the DBM's ODI inputs. The EQM operates synchronous to the control signals input to the DBM's CK inputs. To determine when to store data, the EQM includes comparator logic that can match the data appearing on the ODI inputs against a predetermined expected data pattern or set of expected data patterns. The compare operation performed on each ODI input can be masked individually to eliminate input signals not required for event qualification. The EQM has protocols allowing it to perform different types of event-qualified monitoring operations. The type of monitor operation to be performed (RAM storage, PSA, sample) determines the protocol type used.

To expand the event-qualification capability, multiple DBMs or other SCOPE products incorporating EQMs can be connected via the two-wire event-qualification bus to allow qualification of a test operation to be distributed over a range of devices. During expanded event qualification, each DBM operates to output a match condition on its Event-Qualification

Output (EQO) pin. The match signals from multiple DBMs are combined via a voting circuit to produce a global match signal. The global match signal is input to each DBM via an Event-Qualification Input (EQI) signal. When a global match signal is received by the DBMs, the internal EQM initiates a test monitor operation. In some instances, it may be required to qualify a monitor operation further using external signals. In this case, the external signals are input to the voting circuit to allow finer resolution as to when a monitor operation is performed.

The SCOPE DBM ICs will be available in 28-pin PLCC or LCC packages. The devices will have a 16-bit ODI input bus. The internal RAM will have storage capacity for at least 1K patterns. The PSA capabilities of the DBMs will be cascadable to allow constructing PSA registers in multiples of 16 bits (i.e., 16, 32, 48 . . .).

Conclusion

The 1149.1 standard provides the framework for a structured test approach to eliminate the ad hoc techniques used in the past. The products previewed in this paper provide a starting point from which the realization of 1149.1 may begin. TI will continue to support and develop products for IEEE standards such as 1149.1 to provide the industry with improvements over existing techniques.

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