Application Note

DP83825 Troubleshooting Guide

Shane Hauser

ABSTRACT

DP83825 is a low power 10/100Mbps Ethernet physical layer transceiver with an ultra-small form factor. This troubleshooting guide is intended to help designers using DP83825 narrow down system-level implementation issues.

Table of Contents

Trademarks

1 Introduction

The DP83825 is a low power 10/100Mbps Ethernet physical layer transceiver with an ultra-small form factor supporting Wake-on-Lan (WoL) and Energy Efficient Ethernet (EEE). The device includes hardware bootstraps to configure auto negotiation, and a programmable hardware interrupt pin.

Figure 1-1 is a high-level diagram of a typical DP83825 application.

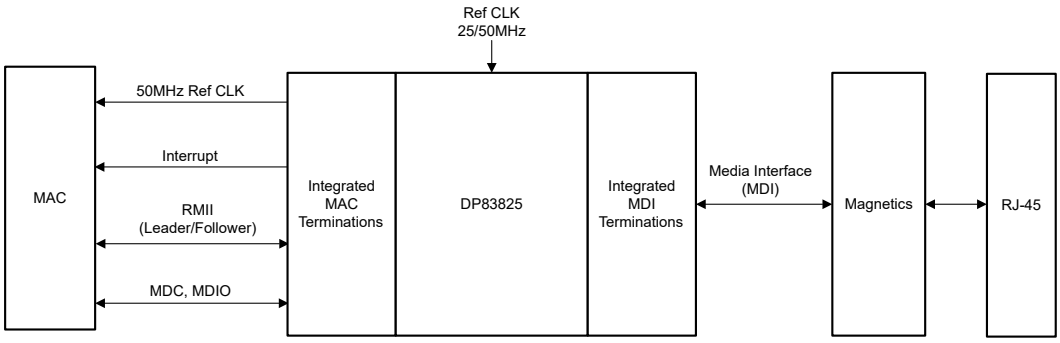

Figure 1-1. DP83825 Application Diagram

The DP83825 connects between an Ethernet MAC and the media through MDI. The connection to the media is typically through magnetics and a connector such as an RJ-45.

2 Troubleshooting the Application

The following sections approach the debug from a high level, basic check approach which isolates subsystems of the PHY design to check if they contribute to an application issue. This document is intended to address common Ethernet issues such as:

- Inability to ping
- Cannot get link OR intermittent linkup
- Linkup but seeing packet errors
- Cannot access registers

The recommendation is to go through the following sections in order unless otherwise specified.

2.1 Schematic Checklist

The DP83825 Schematic Checklist compiles best practices for designing with DP83825 into an easy-to-use document. The recommendation is to go through this document for a detailed description on what connections and components are needed for the PHY to work.

The following sections can present expected behaviors if the PHY is powered and initialized correctly. Any deviations from expected behaviors can point to errors due to incorrect peripheral circuity.

2.2 Device Health Checks

This section dives into device health checks which makes sure the device is powered and initialized correctly. This section can be skipped if DP83825 is:

- Linking up (LED indication or register status) when connected to link partner or showing FLP signals when Ethernet cable is unconnected, and
- Responding to register access (if applicable)

2.2.1 Voltage Checks

DP83825 needs to have sufficient power as well as one 10nF, 100nF, 1uF, and 10uF decoupling per rail:

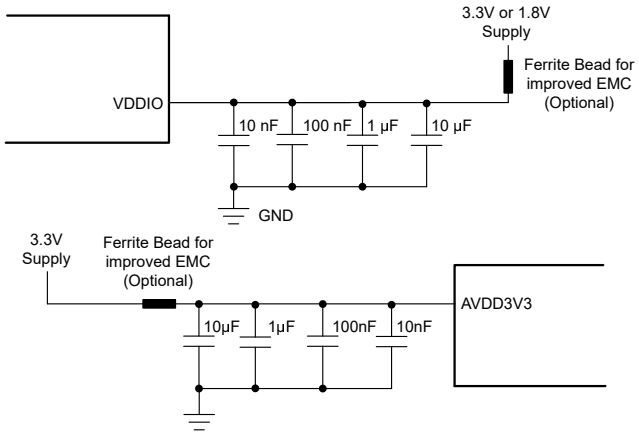

Figure 2-1. Power Supply Decoupling

Power up the device and perform DC measurement of the supplies as close to the pin as possible. Confirm that each measurement is within the limits defined in Table 2-1.

Table 2-1. Recommended Operating Conditions

	Min (V)	Typ (V)	Max (V)
AVDD3V3	3	3.3	3.6
VDDIO (3.3V)	3	3.3	3.6
VDDIO (1.8V)	1.62	1.8	1.98

2.2.2 Probe the RESET_N Signal

The reset functionality on DP83825 is active low. This pin has a weak internal pull-up resistor to provide a default state if left unconnected or not driven externally.

Confirm that the controller is not driving the RESET_N signal low. Otherwise, the device can be held in reset state, and does not respond to register commands nor can link up.

2.2.3 Probe RBIAS

The RBIAS pin is used to set the internal reference current within the DP83825. RBIAS needs to be a 6.49kΩ resistor with a 1% tolerance. The preference is to have a single component over multiple in series as the tolerance range can increase.

If properly powered, a 1V signal appears when probing the RBIAS pin for approximately 60us after power ramp before going back to 0V

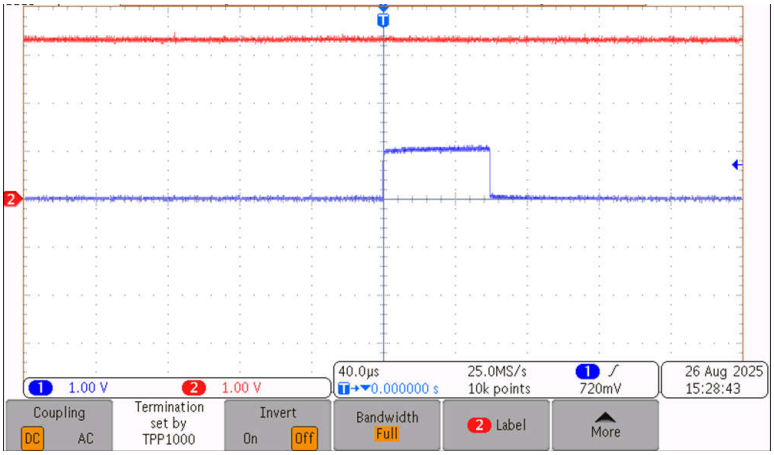

Figure 2-2. RBIAS Voltage (Blue) and VDDA3V3 (Red) on Power up

2.2.4 Probe the XI Clock

The following guidelines are the main specifications to reference for compatible input clocks:

Table 2-2. 25MHz Crystal Specifications

Parameter	Min	Typ	Max	Unit
Frequency		25		MHz
Frequency Tolerance	-50		50	ppm
Load Capacitance		15	40	pF
ESR			50	Ω

Probing on the crystal nodes can change the capacitive loading and therefore change the operational frequency.

Table 2-3. Oscillator Specifications

Parameter	Min	Typ	Max	Unit
Frequency		25 (RMII Leader) 50 (RMII Follower)		MHz
Frequency Tolerance	-50		50	ppm
Rise or Fall Time			5	ns
Duty Cycle	40		60	%

The amplitude of the oscillator must be a nominal voltage of VDDIO.

Note

For more information on designing with a crystal network, please refer to the *Selection and specification of crystals for Texas Instruments Ethernet physical layer transceivers*, application note.

2.2.5 Probe the Strap Pins During Initialization

The DP83825 has strap pins for configuring the device in a predetermined mode. The voltage at these strap pins determines which mode the DP83825 can operate in.

On initialization, the external strap network along with the internal resistor creates a voltage divider that the PHY samples. No other component on the line needs to affect the DC bias set by this network.

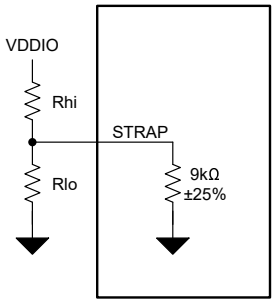

Figure 2-3. DP83825 Strap Circuit

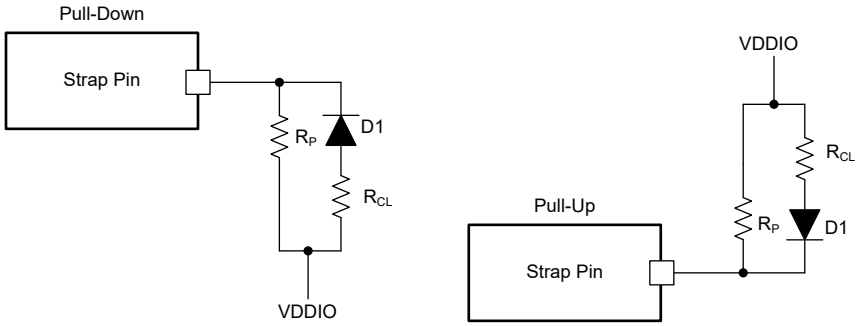

Figure 2-4. DP83825 LED Strap Circuit

In some cases, other devices on the board (for example, the MAC) can drive the strap pins unexpectedly. The strap values can be read from registers 0x0467 (SOR1) and 0x0468 (SOR2). If there is power cycle dependency to an issue, the strapping can be marginal and can be observed cycle to cycle against these registers to determine if the PHY is strapped in an unintended state.

Measurements can be made during power up and after power up when the RESET_N signal is asserted.

2.2.6 Probe the Serial Management Interface (MDC, MDIO)

The Serial Management Interface (SMI) can be useful in providing status fields during a debug. Make sure the MDIO line has a pull up resistor to VDDIO as this pin is an open-drain to the PHY. When idle, the voltage needs to be VDDIO. Make sure the SMI access uses the following sequence:

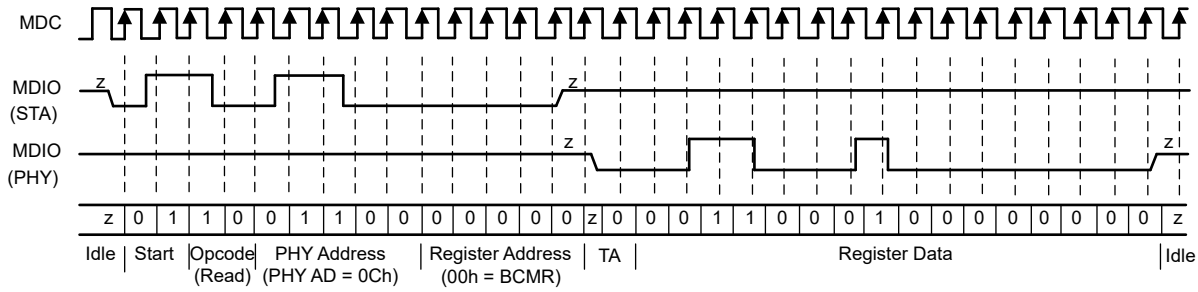

Figure 2-5. SMI Read Operation

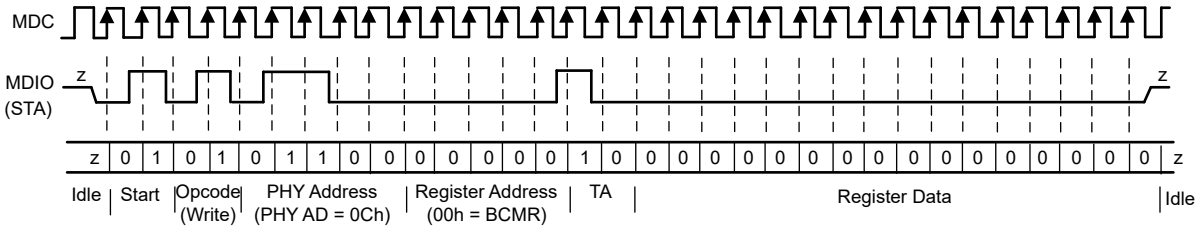

Figure 2-6. SMI Write Operation

2.2.6.1 Read and Check Register Values

Read the registers and verify the default values shown in the data sheet. Note that the initial values of some registers can vary based on strap options. The expected register values for PHY operation and link in 10/100Mbps with auto-negotiation enabled are shown in Table 2-4.

Table 2-4. DP83825 Register Value References

Register Address	Register Value		Comments
	10Mbps	100Mbps	
0x0000	3100	3100	Auto-negotiation enabled
0x0001	786D	786D	Link established
0x0004	0061	01E1	10/100Mbps advertisement
0x0010	4917 or 0917	4715 or 0715	Auto negotiation status

With the PHY linked in a given speed, use these values as a reference to identify any variance from the expected operation. Note that not all registers need to be the same.

Example: After powering and linking the PHY in 10Mbps, Reg 0x10 contains the value 0x0017(Bits 4, 2, 1, 0 are high). This confirms:

- Auto-Negotiation is complete
- Full-Duplex
- 10Mbps Mode
- Link established

Repeating this process for any values distinct from the expected values shown in Table 2-4 help diagnose the exact state of the PHY for any encountered issues.

2.3 MDI Health Checks

This section dives into device health checks which makes sure that the device's MDI section is operating properly. This section can be skipped if DP83825 is linked up and reporting no errors on Reg 0x15 when sending traffic through the device

2.3.1 Magnetics

The following guidelines are the main specifications to reference for compatible magnetics:

Table 2-5. Magnetic Isolation Specifications

Parameter	Test Conditions	TYP	UNIT
Turns Ratio	±2% Tolerance	1:1	-
Insertion Loss	1-100MHz	-1	dB
Return Loss	1-30MHz	-16	dB
	30-60MHz	-10	dB
	60-80MHz	-7.5	dB
Differential to Common Mode Rejection Ratio	1-50MHz	-61	dB
	50MHz	-33	dB
	150MHz	-25	dB
Crosstalk	30MHz	-45	dB
	60MHz	-39	dB
Isolation	HPOT	1500	Vrms

If these exact requirements cannot be met, the following allowances can be made:

- Turns ratio: 3% tolerance is good
- Inductance: High inductance is preferred, typically around 350µH
- Insertion loss: -1dB or closer to 0dB
- Return loss: Meets or exceeds values in Table 2-5. For example -16dB, -17dB, … is good at 1-30MHz

2.3.2 Probe the MDI Signals

In the default configuration, Auto-negotiation and Auto-MDIX can be enabled. A link pulse needs to be visible on the channel transmit (TD_P, TD_M) and can occasionally toggle to the receive pair (RD_P, RD_M). If set to MDI, this pulse is only available on the transmit pair while if set in MDI-X, this will only be available on the receive pair. A short Ethernet cable terminated with 100 Ohm differential needs to be used for measuring the MDI signals. A terminated cable is shown in Figure 2-7. A connection diagram for making measurements with the terminated cable is shown in Figure 2-8.

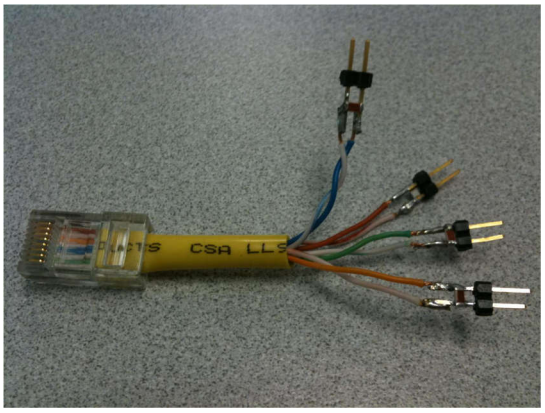

Figure 2-7. 100Ω Terminated Cable

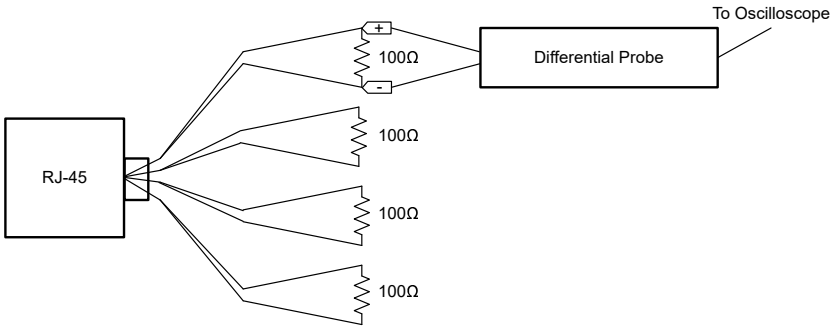

Figure 2-8. 100Ω Terminated Cable Connection Diagram

Auto-negotiation link pulses are nominally 100ns wide. Pulses are spaced by 62µs or 125µs and are transmitted in bursts. The bursts are nominally 2ms in duration and occur every 16ms. Figure 2-9 shows a link pulse.

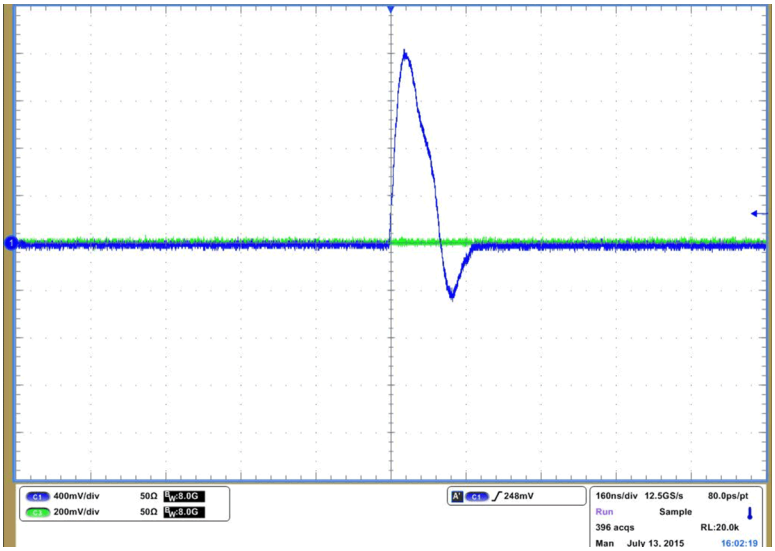

Figure 2-9. Link Pulse Example

2.3.3 Check the Link Quality

After establishing a valid link, confirming the key status register values and visually verifying that the link LED is lit, the next data transfer debug step is to check the MAC Interface. There are several possible sources of link problems:

1. Link partner transmit problem
2. Cable length and quality
3. 25MHz reference clock quality
4. MDI signal quality

With the PHY powered and connected to a link partner, register 0x218 can be used to determine link quality. Read the register value to determine the Mean Square Error (MSE). With the MSE value, refer to Table 2-6 to determine link quality:

Table 2-6. Link Quality Ranges

Link Quality	MSE
Excellent	0x020A > MSE
Good	0x033B > MSE > 0x020A
Poor	MSE > 0x033B

2.3.4 Compliance

IEEE compliance measurements can be made to verify the signaling characteristics. For details on these measurements and how to properly configure the PHY, please refer to *How to Configure DP8382x for Ethernet Compliance Testing*, application note

2.4 RMII Health Check

This section dives into device health checks which makes sure that the device's RMII section is operating properly. The DP83825 offers two modes of RMII operation: RMII Leader and RMII Follower.

In RMII Leader operation, the DP83825 operates from either a 25MHz CMOS-level oscillator connected to XI pin or a 25MHz crystal connected across XI and XO pins. A 50MHz output clock referenced from DP83825 need to be connected to the MAC.

In RMII Follower operation, the DP83825 operates from a 50MHz CMOS-level oscillator connected to the XI pin and shares the same clock as the MAC. Alternatively, the PHY can operate from a 50MHz clock provided by the Host MAC.

The RMII specification has the following characteristics:

- Supports 100BASE-TX and 10BASE-Te
- Single clock reference sourced from the MAC to PHY (or from an external source)
- Provides independent 2-bit wide transmit and receive data paths
- Uses CMOS signal levels

The RMII mode of operation is configured via hardware strapping on RX_D1. Register 0x0017[7] can confirm whether RX_D1 is strapped to RMII leader or follower mode. The RMII signals are summarized in Table 2-7.

Table 2-7. RMII Signals

Function	Pins
Receive Data Lines	TX_D [1:0]
Transmit Data Lines	RX_D [1:0]
Receive Control Signal	TX_EN
Transmit Control Signal	CRS_DV

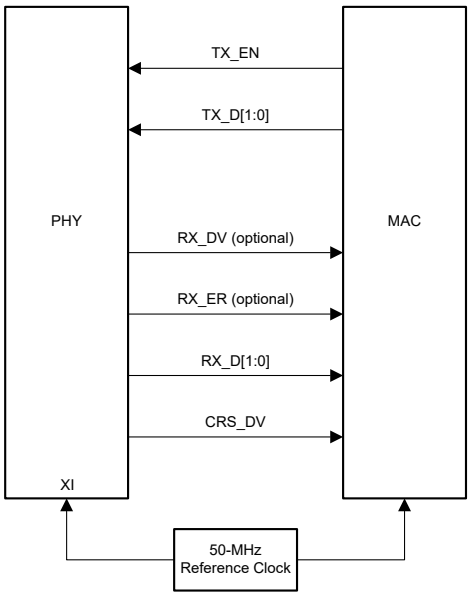

Figure 2-10. RMII Follower Signaling - MAC Follower Configuration

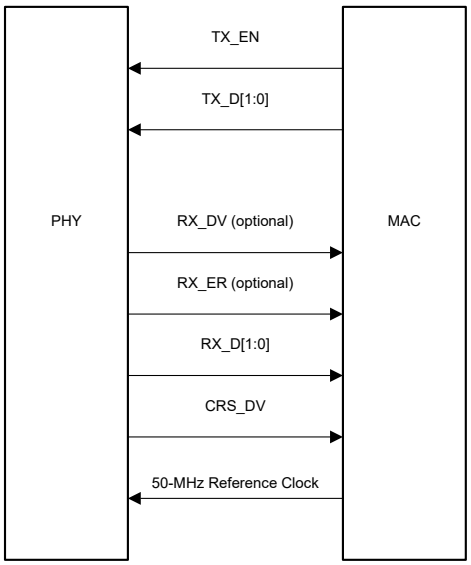

Figure 2-11. RMII Follower Signaling - MAC Leader Configuration

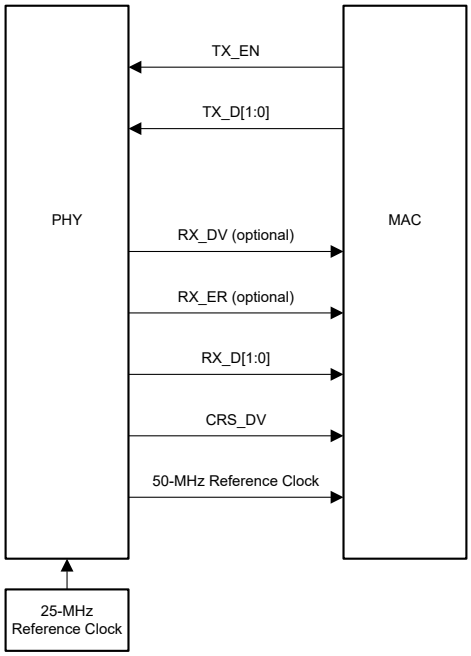

Figure 2-12. RMII Leader Signaling

Data on TX_D [1:0] is latched at the PHY with reference to the 50MHz-clock in RMII Leader and Follower modes. Data on RX_D [1:0] is provided with reference to the 50MHz clock. In addition, CRS_DV can be configured as an RX_DV signal. This allows a simpler method of recovering receive data without the need to separate RX_DV from the CRS_DV indication.

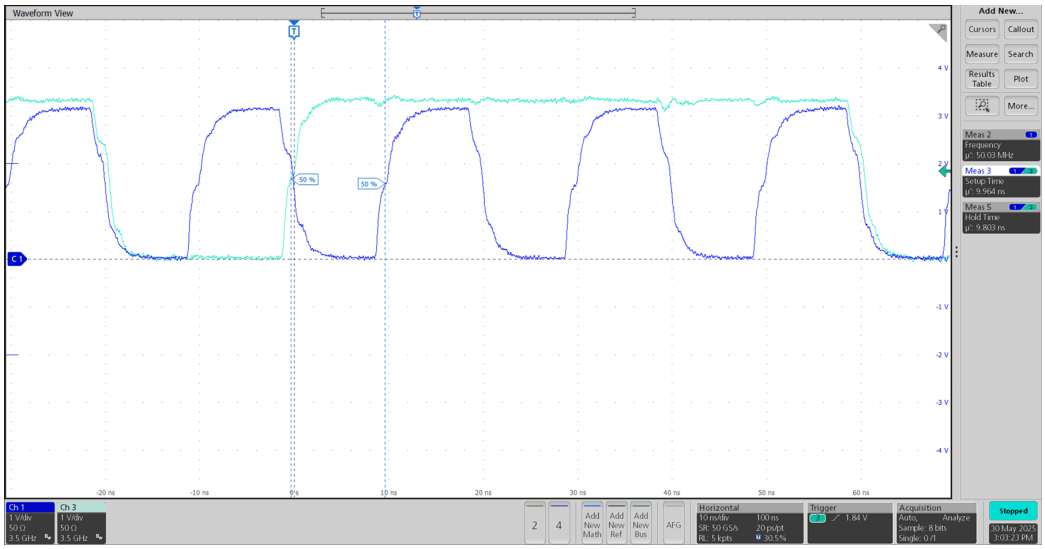

Figure 2-13. RMII 50MHz Clock (Blue) and Data (Green)

2.5 Loopback and PRBS

2.5.1 Loopback Modes

There are several options for loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the RMII and MDI data paths. DP83825 can be configured to one of the near-end (MII) loopback modes or to the reverse (MDI) loopback mode.

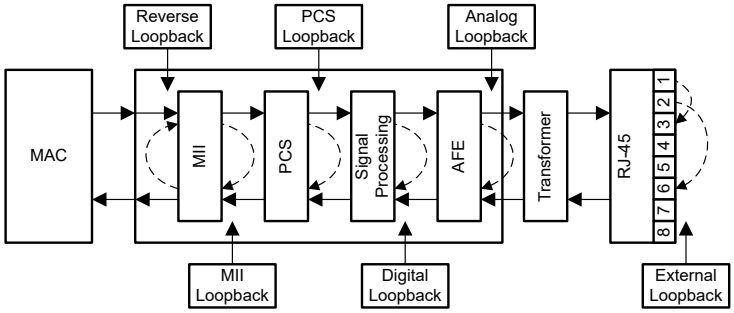

Figure 2-14. Loopback Modes

MII loopback can be used to verify the MAC interface, while reverse loopback is used with a link partner to verify the data path along the MDI.

- MII loopback is enabled by setting registers 0x0000[14] and 0x0016[2]
- Reverse loopback is enabled by setting register 0x0016[4]

2.5.2 Transmitting and Receiving Packets with the MAC

If generating and checking packets with the MAC is possible, and the PHY has a working link partner with reverse loopback capability, verify the full data path as follows:

1. Power and connect the PHY to the MAC and a working link partner.
2. Enable reverse loopback on the link partner.
3. Transmit test packets from the MAC to the PHY.
4. Verify the MAC receives the same test packets.

If the MAC receives the same test packets transmitted without issue, the full MAC → PHY → MDI data path is valid. If this test does not pass, perform MII loopback to isolate the issue along the data path:

1. Power and connect the PHY to the MAC.
2. Enable MII loopback on the PHY.
3. Transmit test packets from the MAC to the PHY.
4. Verify the MAC receives the same test packets.

If the MAC receives the same test packets, the MAC → PHY data path is valid, and the issue has been isolated to the MDI data path. If this test does not pass, the issue is likely on the MAC interface. To verify the MAC interface, refer to the Section 2.4 of this application note. To verify the PHY internal data path, perform the above procedure using analog loopback mode.

2.5.3 Transmitting and Receiving Packets with BIST

The device incorporates an internal PRBS Built-in Self-Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be used to test the integrity of the transmit and receive data paths. BIST can be performed using various loopback modes to isolate any issues to specific parts of the data path. The BIST generates packetized data with variable content and IPG.

If generating and checking packets with the MAC is not possible, use PRBS packet generation and checking functionality to verify the data path. Perform reverse loopback with PRBS and a working link partner as follows:

1. Power and connect the PHY to a link partner.
2. Enable PRBS packet generation on the PHY (write Reg 0x0016 = 0x5000).
3. Enable reverse loopback on the link partner.
4. Wait at least one second, then check PRBS lock status on the PHY by reading register 0x16[11:10].

If register 0x16[11] is high, the data path through PHY → MDI is valid. If this test does not pass, the issue can be on the PHY's internal data path or the MDI. To verify the internal data path, perform PRBS with analog loopback using the following procedure:

1. Write register 0x001F = 0x8000 //PHY reset
2. Write register 0x0000 = 0x2100 //Disable Auto-neg, force 100Mbps
3. Write register 0x0016 = 0x0108 //Enable Analog loopback, use 100Ω MDI terminations
4. Write register 0x0016 = 0x3108 //Enable PRBS generator and checker
5. Read register 0x0016 //Need to read 0x3B08 for PRBS active and locked
6. Read register 0x001B //Need to read 0x007D for no errors

If the internal data path is valid the issue is isolated to the MDI or the link partner.

3 Summary

This application note provides a suggested flow for evaluating a new application and confirming the expected functionality. The step-by-step recommendations can help ease board bring up and initial evaluation of DP83825 designs.

4 References

1. Texas Instruments, *Selection and specification of crystals for Texas Instruments Ethernet physical layer transceivers*, application note.
2. Texas Instruments, *How to Configure DP8382x for Ethernet Compliance Testing*, application note.
3. Texas Instruments, *DP83825I Low Power 10/100 Mbps Ethernet Physical Layer Transceiver*, data sheet.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265