Application Note

Open-Drain Output and Power Consumption Using TI Programmable Logic Devices (TPLD)

ABSTRACT

This application note explores the use of open-drain outputs and mixed-signal voltage circuits in TI programmable logic devices (TPLDs), providing an overview of the design principles and challenges associated with these circuits. This document specifically focuses on the use of these circuits in systems that require interfacing with multiple voltage domains, such as industrial control systems, medical devices, or personal electronic applications, which combine low-voltage digital processing with high-voltage sensing or actuation.

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Trademarks

1 Introduction to Mixed-Voltage Logic in TPLD

The demand for smaller, more power-efficient devices is driving many semiconductor devices and circuit designs to use lower supply voltage levels, such as 1.8V. These advances in technology and manufacturing are challenged by managing integration with existing devices or complying with industry standards that potentially require higher supply voltages, such as 3.3V or 5V. To address these challenges, voltage level translation is a feature in logic devices which serves as a bridge between devices like processors, sensors, and devices of different generations. See Basics of Voltage-Level Translation for a comprehensive explanation of voltage translation.

TI programmable logic devices (TPLDs) can up-translate and down-translate voltages, allowing for the use of several different logic levels. All TPLDs have an optional low-voltage digital input mode for the input pins, allowing for 1.8V logic inputs across all supply voltages. Similarly, the TPLD can facilitate voltage translation with an optional open-drain NMOS output mode. Details about how to use these TPLD features can be found at Up and Down Translation in TI's Programmable Logic Devices (TPLD).

2 Introduction to Output Modes

There are three common output modes for CMOS devices, all of these modes are optional in TPLD. These include push-pull, open-drain, and tri-state.

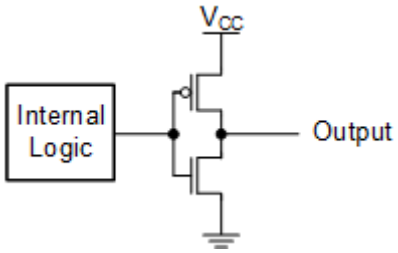

Figure 2-1. Typical Push-Pull Output Configuration

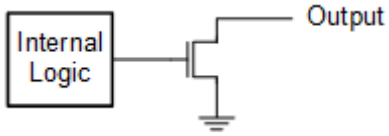

Figure 2-2. Typical Open-Drain Configuration

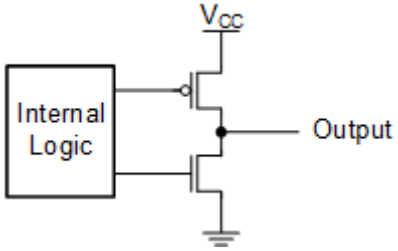

Figure 2-3. Typical Tri-State Output Configuration

The difference between open-drain and push-pull outputs is in the way the outputs drive output signals. A push-pull output uses two transistors to actively drive the line both high and low with one transistor pushing to VCC and the other pulling to ground, providing strong drive in both directions. An open-drain output only has a transistor to pull the line low to ground; the open-drain output relies on an external pullup resistor to bring the line high when the transistor is off. As a result, push-pull outputs actively control both states while open-drain passively releases the line high and actively pulls the line low. As the name suggests, a tri-state output can be in one of three states at any given time:

- Driving high
- Driving low
- Not driving (high impedance)

Tri-state outputs are similar to push-pull devices but with the addition of a high-impedance state.

Choosing between output types depends on how the signal is used and which trade-offs matter most in the design. Push-pull outputs are better when fast edges or frequent switching is required. Open-drain outputs are a better choice when the signal line is shared by multiple devices, when level flexibility is required, or if the signal is idle most of the time. Tri-state outputs are a good choice for when a signal line is shared by multiple devices but the use of external resistors is undesirable. Tri-state outputs often require an additional input to take them in and out of the high impedance state.

Push-pull outputs consume power mainly during switching, actively charging and discharging the load capacitance during switching. Unlike open-drain output devices, push-pull output devices do not need to pull current through a resistor for a low signal, making push-pull more power efficient for signals that toggle often or remain low for long periods.

Aside from a small amount of leakage current, open-drain outputs draw virtually no power when the signal is high. This makes open-drain devices excellent for signals that idle high and do not switch often, such as status lines or interrupts. However, open-drain outputs must draw current through a pullup resistor to achieve a low signal. The current consumption can be reduced by increasing the size of the pullup resistor, but increasing the resistor decreases the switching speed and potentially impacts the ability of the device to drive any loads on the line.

3 Timing of Open-Drain Outputs

Open-drain outputs rely on an external pullup resistor to pull the output voltage high. As a result, the output rise time depends on the value of the pullup resistor and the load capacitance, including pin capacitance and parasitic capacitance. This combination of a pullup resistor and load capacitance has all the characteristic behaviors of a typical resistor-capacitor (RC) circuit.

As an example, this section refers to the setup shown in Figure 3-1 as using a basic buffer configuration, shown in Figure 3-2.

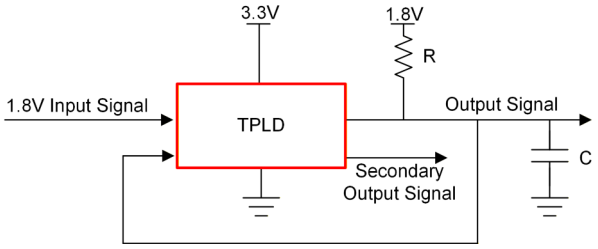

Figure 3-1. TPLD Open-Drain Output Example

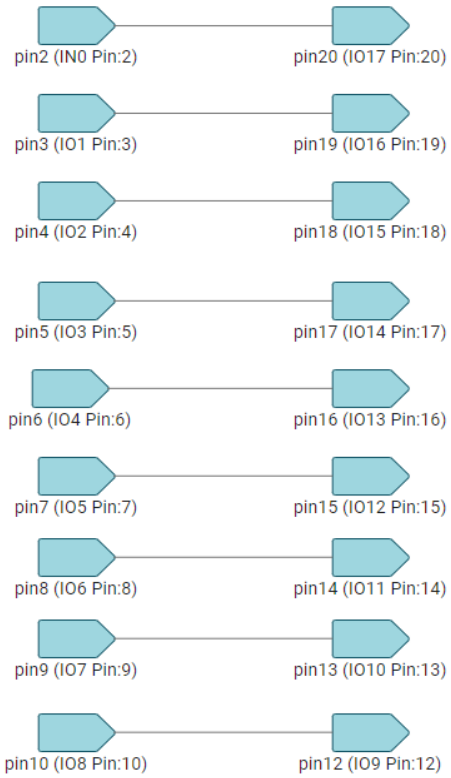

Figure 3-2. TPLD Buffer Configuration

This output signal is part of an RC circuit, and the voltage seen at the output signal when transitioning from a low to high state is governed by the equation:

$$V_C = V_S\left(1 - e^{-t/RC}\right) \quad (1)$$

The 10% to 90% rise time of an RC circuit is:

$$t_{rise} = 2.2\tau = 2.2RC \quad (2)$$

In this case, V_s is 1.8V supply from the pullup resistor and V_C is the voltage across C.

Equation 1 shows that the rise time of an open-drain device is dependent on the pullup resistor because the load capacitance is not easy to change in many applications. This means that choosing the correct resistor value for a specific application becomes very important. By Ohm's law, a larger resistor reduces the current, and therefore, reduces the power consumption. However, a larger resistance also increases the rise time of the output signal.

Ohm's law also dictates the minimum size of the pullup resistor that can be used, and therefore, the maximum rise time. This equation is:

$$R_{pullup,\,min} = \frac{V_{out}}{I_{OL}} \quad (3)$$

Every open-drain device defines a maximum low-level output current, I_{OL}, and this can be used to calculate the smallest allowable resistor before risking damage to the device with high current. Continuing with the TPLD2001 example, there are two options for I_{OL}. In this example, I_{OL} = 20mA is selected, and V_{out} = 1.8V. This selection makes $R_{pullup,min}$ = 90Ω. This resistor produces a fast rise time, but also uses a lot of power. Choosing a

90Ω resistor over a 9kΩ resistor means a 100 times faster rise time but a 10,000 times increase in power consumption. Whether this outcome is considered a fair trade depends on the design requirements.

Although the rise time of an open-drain output is dependent on the pullup resistor size, the fall time is not. An open-drain device passively releases the output high, but the device actively pulls the output low. This outcome produces the asymmetric rise and fall time of open-drain output devices.

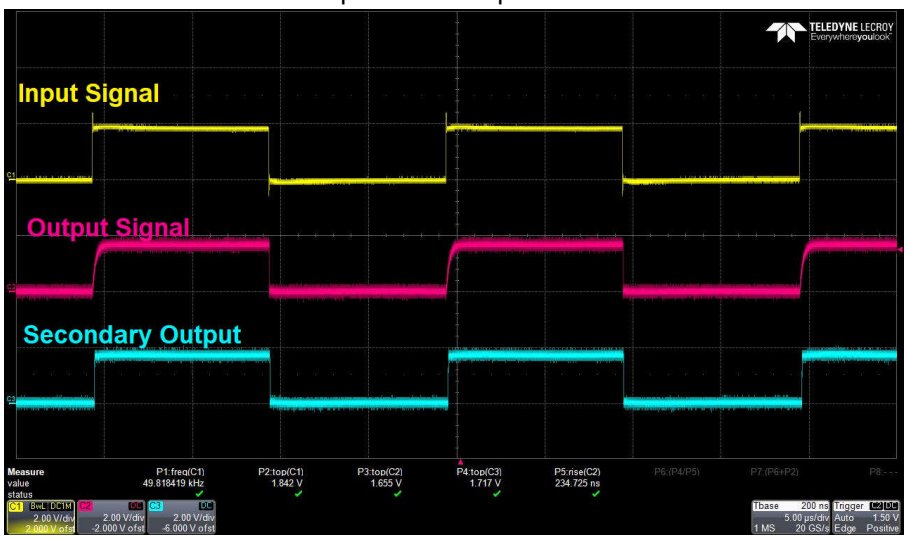

Figure 3-3. Input and Outputs at 50kHz

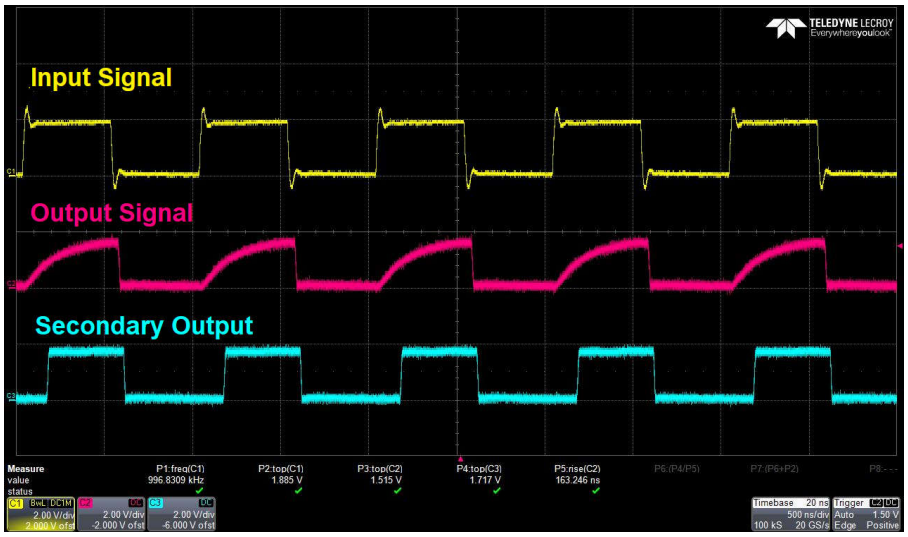

Figure 3-4. Inputs and Outputs at 1MHz

The waveforms in Figure 3-3 and Figure 3-4 show the inputs and outputs of the test setup shown in Figure 3-1. The setup includes a TPLD2001 resistor configured as a simple buffer with low-voltage inputs (as shown in Figure 3-2) to accept 1.8V logic even though the TPLD is powered by a 3.3V rail. Note that the TPLD can also be powered directly by 1.8V. The output labeled *Secondary Output* is configured as a push-pull output. The pullup resistor is 10kΩ. At 50kHz, the effect of this large pullup resistor becomes evident, and at 1MHz, the slow rise time of the output signal starts to affect the duty cycle of the signal of the *Secondary Output*. Although the TPLD2001 resistor can output frequencies up to 8MHz from any output pin in push-pull mode; the output speeds of the open-drain mode outputs of the resistor are still determined by the RC time constant. For this reason, open-drain outputs are rarely appropriate for high-speed applications.

More information about how to choose a pullup resistor can be found at Choosing an Appropriate Pull-Up/ Pull-Down Resistor for Open Drain Outputs.

4 Calculating Power Consumption

In CMOS devices, the static and dynamic power consumption of a device are important. TPLD is no different in this regard.

Static power consumption for CMOS devices is calculated by using the equation:

$$P_{S,\,Device} = V_{Supply} I_{CC} \tag{4}$$

For a push-pull device, this is all the power drawn from the VCC pin of the device when the output does not switch. For an open-drain device, this calculation is still valid, but the system as a whole includes the current that is drawn through the external pullup resistors. To use the example in Figure 3-1, this is the 1.8V source. If the output is low, the power consumption of the system includes both the power drawn from the 3.3V source of the device, in addition to the power dissipated in the device by the pullup resistor. The total power consumption of the system for an open-drain device must include:

$$P_{S,\,Total} = P_{S,\,Device} + N_{Low} \frac{V^2}{R} \tag{5}$$

Equation 5 illustrates that a larger pullup resistor is advantageous when power consumption is a concern; particularly, when many outputs are in a low state at the same time. However, a larger pullup resistor is detrimental to the switching speed, as shown in the previous section. Timing and power consumption are the major trade-offs to consider for open-drain devices.

Dynamic power consumption is a bit more complicated. This type of consumption includes transient power consumption and capacitive-load power consumption, and only occurs when a device switches from one state to another. Dynamic power consumption includes the power consumed in charging external load capacitance, the power necessary to charge the internal nodes, and the power consumed by the shoot-through current that flows from Vcc to GND when both the p-channel and n-channel transistors turn on briefly at the same time. When used in open-drain NMOS mode, a TPLD in open-drain output mode avoids shoot-through current, as do similar open-drain devices.

Additional information on this topic can be found in CMOS Power Consumption and Cpd Calculation.

5 Summary

TPLDs can up-translate and down-translate voltages, allowing for the use of several different logic levels, and the outputs facilitate voltage translation with an optional open-drain NMOS output mode. Open-drain outputs are appropriate for signals that idle high and do not switch often, such as status lines or interrupts; as these signals consume virtually no power when the signal is high, and the signals can be tied together at the outputs without danger of bus contention. When considering power consumption of a system that uses open-drain outputs, selection of an appropriate pullup resistor is critical, as this value affects the rise time and power consumption of the output signal; a larger resistor can reduce power consumption but increase the rise time. Understanding these trade-offs is essential for excellent system design.

6 References

- Texas Instruments, Basics of Voltage-Level Translation, Application Report
- Texas Instruments, Up and Down Translation in TI's Programmable Logic Devices (TPLD), Application Brief
- Texas Instruments, Choosing an Appropriate Pull-Up/Pull-Down Resistor for Open Drain Outputs, Application Report
- Texas Instruments, CMOS Power Consumption and Cpd Calculation, Application Report

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