Application Note

Design Considerations for Large Y-Capacitor Resistive-Bridge DC Insulation Monitoring Device

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ABSTRACT

The two most common methods to measure insulation are AC current injection and resistive bridge. In general, the AC current injection method is flexible for various operating conditions and is widely used in DC charging but has higher complexity and cost compared to the resistive bridge method. Regardless of the method, the approach has to meet the standard requirements such as accuracy, response time, and operating voltage limits. One of the key challenges associated with the resistive bridge method is dealing with a large RC time constant. Some systems such as megawatt chargers require very large Y-capacitances (for example, 4µF). This application note discusses the design considerations for a resistive-bridge approach that is specially designed to deal with large Y-capacitances by employing a novel predictive algorithm to shorten the measurement time without requiring heavy computation such as floating-point operations.

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Trademarks

1 Introduction

High-voltage (HV) DC systems show accelerated adoption across multiple end equipment applications including energy storage systems, data centers, solar inverters, and DC fast chargers. The typical DC voltage for these applications ranges from 150V to 1000V. Larger energy storage systems operate at voltages up to 1500V. User protection represents an important design consideration in these HV DC systems. All HV parts of the system receive electrical isolation from PE through high-ohmic paths (typically in the high MΩ range). The insulation limits the maximum leakage current. International standards (for example, UL 2231-2, IEC 61851-23 for EV charging) require that leakage current remain limited to 10mA (that is, 100Ω/V) to avoid personal injury from contact with the system. IEC 61851-23 specifies a safe isolation rating when the leakage measures less than 2mA (500Ω/V). Table 1-1 shows the insulation monitoring device (IMD) key thresholds. Figure 1-1 shows that the IMD monitors insulation resistance and reports faults to the main controller when the insulation resistance becomes insufficient. The main system controller initiates a safe shutdown sequence following a fault. These IMDs operate continuously at a low frequency of 1Hz to 2Hz because insulation changes occur slowly.

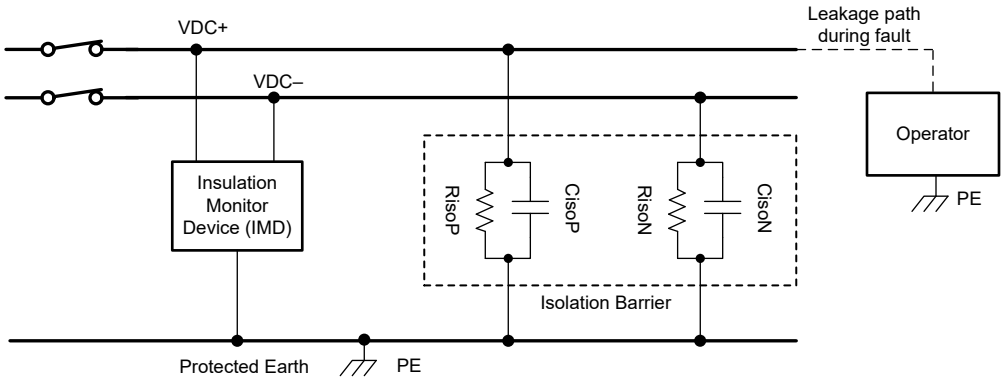

Figure 1-1. Insulation Monitoring Device in DC Unearthed Distribution Systems

Table 1-1. IMD Key Thresholds from IEC and UL Standards

STATUS	Ω/V	LEAKAGE CURRENT	800V VBus	1000V VBus
Warning	500	2mA	400kΩ	500kΩ
Fault	100	10mA	80kΩ	100kΩ

1.1 Insulation Monitor

There are a number of methods for measuring insulation. However, the two most common methods are AC current injection and resistive bridge. In general, the AC current injection method is flexible for various operation conditions and is widely used in DC charging but has higher complexity and cost compared to the resistive bridge method. Regardless of the method, the approach has to meet the standard requirements such as accuracy, response time, and operating voltage limits. One of the key challenges associated with the resistive bridge method is dealing with a large RC time constant. Some systems such as megawatt chargers require very large Y-capacitances (for example, 4µF). In TIDA-010985, which implements the resistive-bridge approach, the reference design was specially designed to deal with large Y-capacitances by employing a novel predictive algorithm to shorten the measurement time without requiring heavy computation such as floating-point operations. In addition, this new design topology limits the voltage variation on the Y caps. Table 1-2 shows a comparison overview of the various methods.

Table 1-2. Comparison of Various IMD Methods

METHOD	ADVANTAGES	DISADVANTAGES
AC Current Injection • Typically sold as a standalone module	• Can measure energized and non-energized lines • No reduction in insulation resistance during measurement • Supports UL 2231-2 including large Y caps	• High hardware complexity and cost • High software complexity (AC signal processing, floating point math)
Resistive Bridge • TIDA-01513, BQ79731 EVM • TIDA-010232 (MCU on isolated GND)	• Simple implementation – both hardware and software • Low cost • Low calculation effort	• Does not support UL 2231-2 for large Y caps (>100nF) • Does not support IEC 61851-23 due to high voltage swings relative to PE during measurement. Limits applications to < 500 Vbus • Only capable of measuring energized lines • Slightly reduces insulation resistance during measurement
Balanced Resistive Bridge + Prediction Algorithm • TIDA-010985 (MCU on Earth GND)	• Simple implementation – both hardware and software • Low cost and computationally light • Limited voltage swings relative to PE during measurement, supporting IEC 61851-23 • Supports UL 2231-2 including large Y caps	• Only capable of measuring energized lines • Slightly reduces insulation resistance during measurement

Table 1-3 **s**ummarizes the key specifications for TIDA-010985 compared to UL 2231-2 and IEC 61851-23.

Table 1-3. Key UL 2231-2 , IEC 61851-23 Specifications

PARAMETER	UL 2231-2 / IEC 61851-23 SPECIFICATION	TIDA-010985
Trip Accuracy (symmetrical and asymmetrical faults)	15%	5%
Response time	<10 seconds	<2 seconds (Ciso = 4µF, Riso = 1MΩ)
Line to PE Voltage Variation % of VDC	10%	10% (i.e. 50V for 1kV bus)

2 Detailed Description

The design considerations for this application note is based on the TIDA-010985 reference design hardware. For convenience, the TIDA-010985 system block diagram is shown in Figure 2-1.

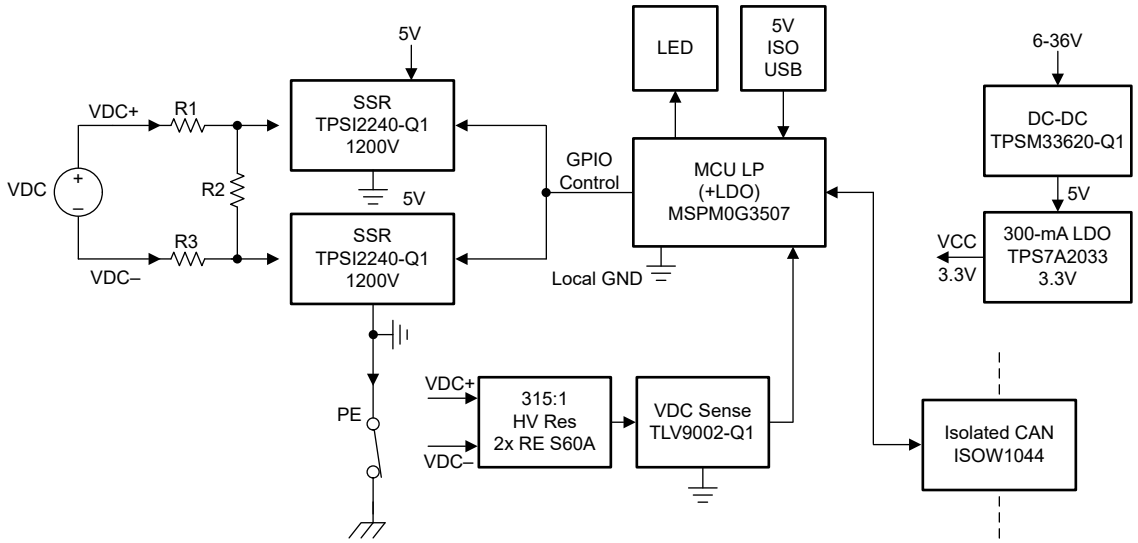

Figure 2-1. TIDA-01985 System Block Diagram

As shown in Figure 2-2, the TIDA-010985 analog front end (AFE) key system components are:

1. Mechanical connectors to DC+, DC- and Protected Earth (PE)
2. The quasi-balanced resistive network providing multiple test resistance combinations (Rsn, R1, Rsp).
3. TPSI2240 bidirectional solid-state switches (SW1, SW2) to alternate the resistive network
4. Single-supply inverting amplifier for voltage sensing of VDC- relative to PE. Voltage is scaled down to ADC level (Vn). Required to calculate RisoN and RisoP.
5. Single-supply voltage buffer for voltage sensing of VDC+ relative to PE. Voltage is scaled down to ADC level (Vp). Required to calculate RisoN and RisoP.
6. A microcontroller is used to control these switches, sample the analog outputs (simultaneously), and calculate the insulation resistances.

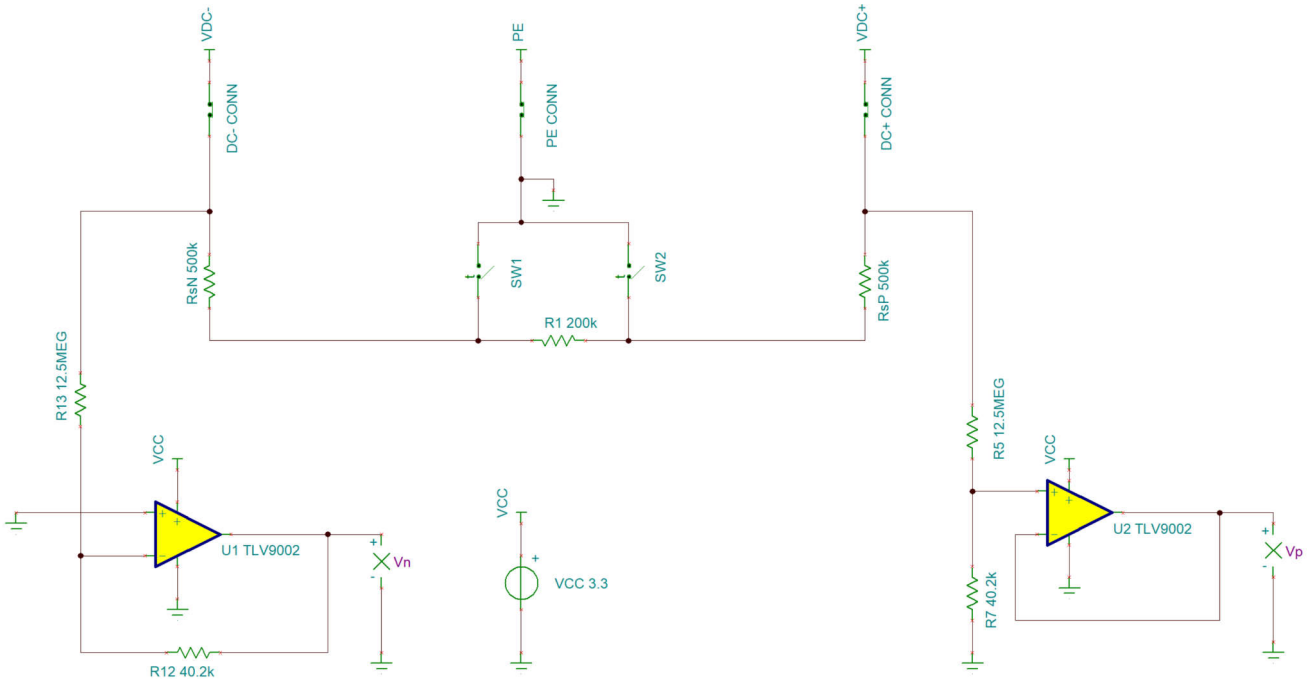

Figure 2-2. Simplified Schematic of TIDA-010985 without Target System Connected

Figure 2-3 shows the simplified schematic with the target system connected. All Riso and Ciso passives are unknowns the IMD needs to solve for.

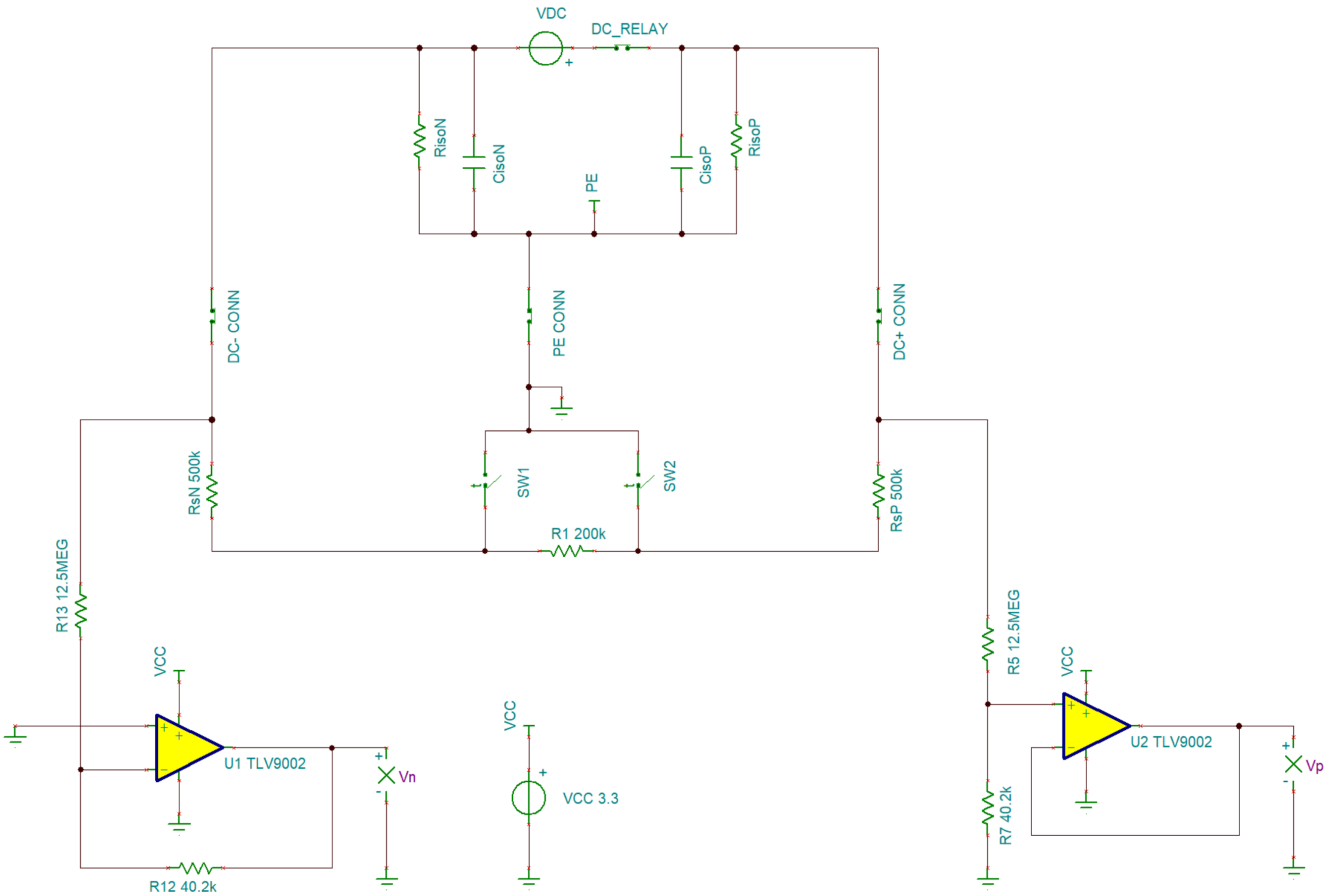

Figure 2-3. Simplified Design Schematic with Target System Connected.

The resistive network is made from a combination of parallel and series resistors as shown in Figure 2-4. The key considerations here are

- Power rating - must consider a worst-case condition such as during an asymmetric fault where the entire Vbus is applied to one side. For 1kV with 500kΩ per side, that is each ladder step (for example, R8 and R20) needs to support 0.4W (worst-case). Each resistor is rated for 0.25W and effectively 0.5W for each ladder step. During normal condition, each ladder step dissipates approximately 0.1W.
- Component tolerance for accuracy – to minimize the error from the resistor tolerance, 0.1% resistor tolerance was selected. This contributes to approximately 0.03% voltage ratio measurement error. If 0.5% resistors are used, the error rises to approximately 0.167%. If 1% resistors are used, the error rises to approximately 0.33%.
- Resistance value affecting measurement time – since the resistance affects the time constant, it is important to size the value appropriately. The settling time is the longest when the insulation is normal (MΩ levels). When the resistive bridge is active, the effective resistance is lowered.
- Leakage current to earth – the resistive bridge cannot be too low in resistance such that the leakage current is too high. For a 1 kV bus, assuming the 500kΩ per side when the switch is ON, the leakage is 2mA if a person touches one of the HV rails while standing on earth ground.

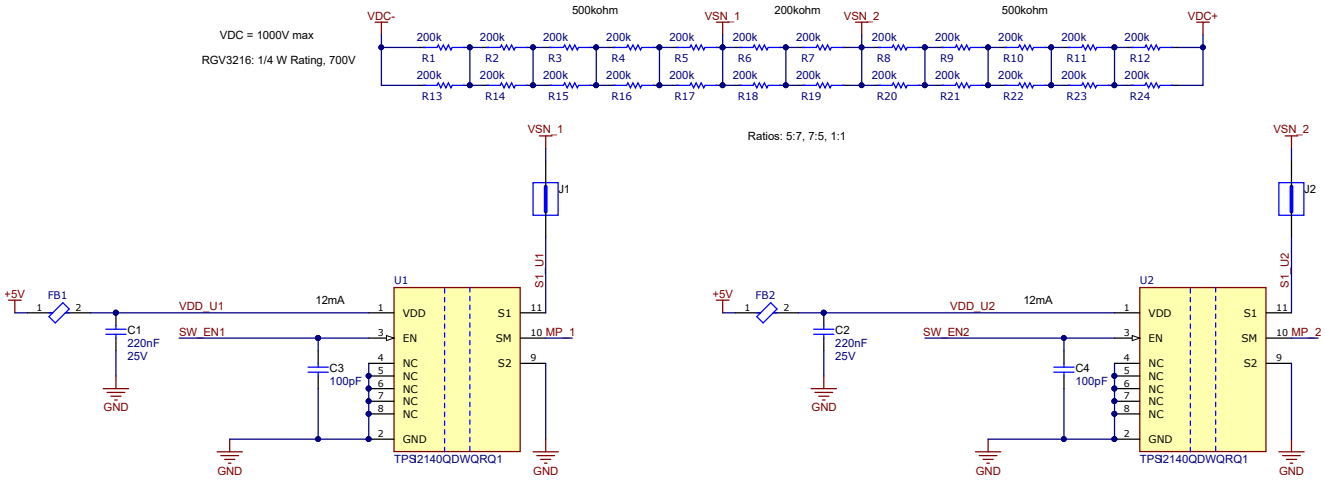

Figure 2-4. TIDA-010985 Schematic Showing the Implementation of the Resistive Bridge Network and the Solid-State Switches

The exact TIDA-010985 voltage sensing circuit implementation is shown in Figure 2-5 and Figure 2-6. RC filter can be modified as needed to meet the system requirements. The default RC values shown in Figure 2-6 (R33 C19) are really meant for a charge bucket function. The help reducing noise, limiting the BW further is recommended (for example, 500Hz). Another option is to add a small capacitor in the feedback loop of U3A (pin 2 and pin 1) and at the positive input of U3B (pin 5 and GND).

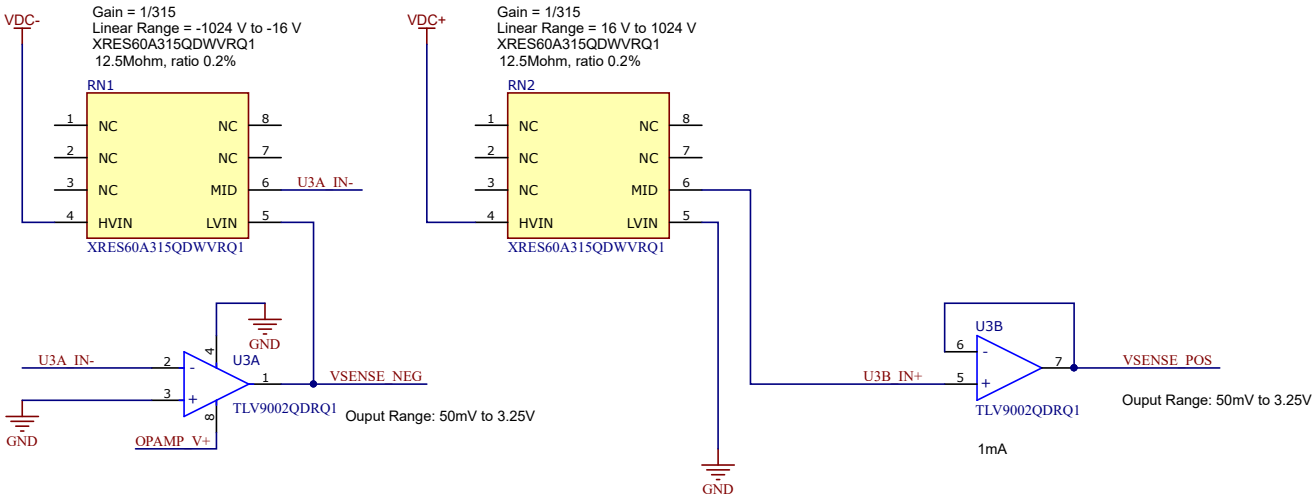

Figure 2-5. TIDA-010985 Schematic Showing the Implementation of the Voltage Sensing Circuits

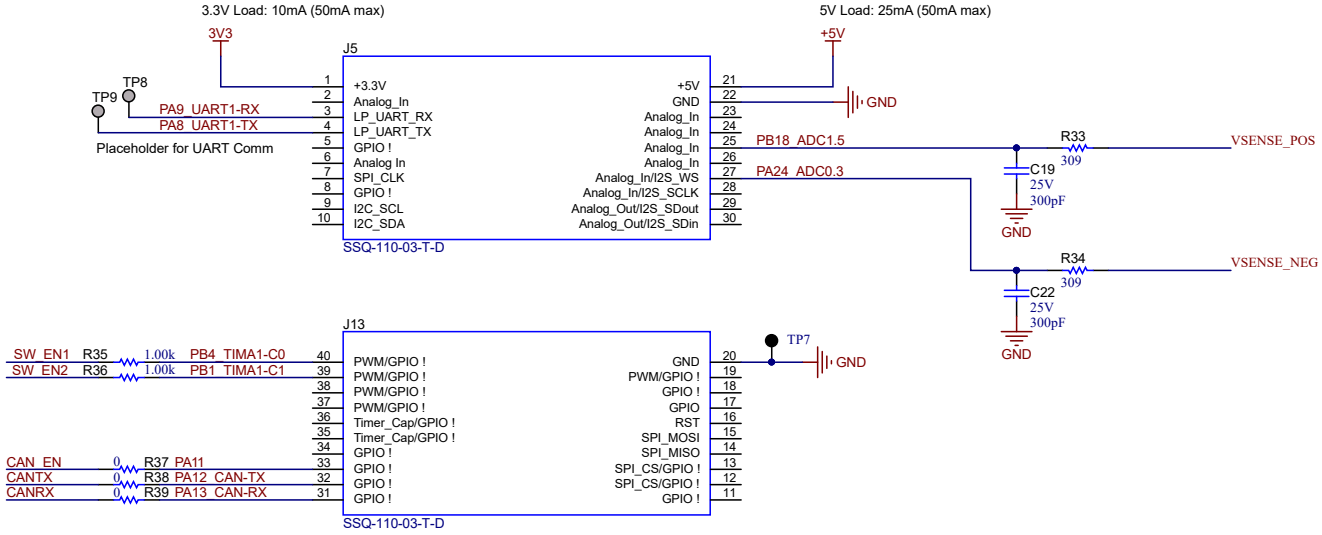

Figure 2-6. TIDA-010985 Schematic Showing the Implementation of the RC Filters

2.1 Solving for the Unknown Isolation Resistances

Two switches enable multiple resistive bridge test ratios using RsP, RsN, and R1. This configuration provides detection capability for any given RisoP to RisoN ratio. The system detects both asymmetric and symmetric faults. Table 2-1 shows the possible switching states for TIDA-010985 and corresponding equations. Only two switching states (except D) are required to solve for RisoP and RisoN. Two equations solve for two unknowns.

Table 2-1. All possible switching states for TIDA-010985

State	SW1	SW2	RsP:RsN Ratio	Steady State Equation
A	ON	OFF	7:5	$\frac{Vp}{Vn} = \frac{-RisoP \mid\mid (7R)}{RisoN \mid\mid (5R)}$
B	OFF	ON	5:7	$\frac{Vp}{Vn} = \frac{-RisoP \mid\mid (5R)}{RisoN \mid\mid (7R)}$
C	ON	ON	5:5	$\frac{Vp}{Vn} = \frac{-RisoP \mid\mid (5R)}{RisoN \mid\mid (5R)}$
D	OFF	OFF	N/A	N/A

In theory, designers can choose any two combinations of A, B, and C switching states. This reference design uses switching states A and B to solve for the isolation resistances. This AB combination maximizes the signal to noise ratio (SNR) by generating the greatest voltage difference between the switching states while limiting voltage variation under IEC requirements. With this selection, the two relevant equations are:

$$\frac{Vp1}{Vn1} = \frac{-RisoP||(7R)}{RisoN||(5R)} \quad (1)$$

$$\frac{Vp2}{Vn2} = \frac{-RisoP||(5R)}{RisoN||(7R)} \quad (2)$$

where

- Vp1 is the voltage of first DC+ measurement (Switch state A)
- Vn1 is the voltage of first DC- measurement (Switch state A)
- Vp2 is the voltage of second DC+ measurement (Switch state B)
- Vn2 is the voltage of second DC- measurement (Switch state B)

Using two equations solves for the two unknowns (RisoP and RisoN). MATLAB® helped solve the equations.

```
% solve for two equations with two unkowns assuming settled voltages
clc
syms rp rn vp1 vp2 vn1 vn2 rs
% change the sign if we're using inverting op amp for the vn sense
eq1 = vp1/vn1 == (rp*7*rs/(rp+7*rs)) / (rn*5*rs/(rn+5*rs));
eq2 = vp2/vn2 == (rp*5*rs/(rp+5*rs)) / (rn*7*rs/(rn+7*rs));
eq3 = rs > 0 & vp1 > 0 & vn1 > 0;
eqns = [eq1, eq2, eq3];
%
[srna, srpa, parametersa, conditionsa] = solve(eqns,[rn, rp],ReturnConditions=true)
%
```

The calculation for this yields:

$$RisoN = \frac{-(35*Vn1*Vp2 - 35*Vn2*Vp1)*RS}{(7*Vn1*Vp2 - 5*Vn2*Vp1 + 2*Vp1*Vp2)} \quad (3)$$

$$RisoP = \frac{-(35*Vn1*Vp2 - 35*Vn2*Vp1)*RS}{(2*Vn1*Vn2 + 7*Vn1*Vp2 - 5*Vn2*Vp1)} \quad (4)$$

Note the RS constant is defined as100 kΩ. If the user uses a different ratio, the MATLAB script can be modified to solve for the new chosen ratio.

Figure 2-7 shows an example voltage waveform with the AB combination. In this example, each switching state lasts for one second. One IMD measurement cycle takes two seconds since measurement for the two states is required. Vp1 and Vn1 are measured simultaneously within the first second, and Vp2 and Vn2 are measured simultaneously in the following second. Note that simultaneous ADC measurement of Vp and Vn rejects noise disturbances on the HV bus. The Riso answer depends on the difference in ratios of Vp to Vn (not the individual absolute Vp and Vn).

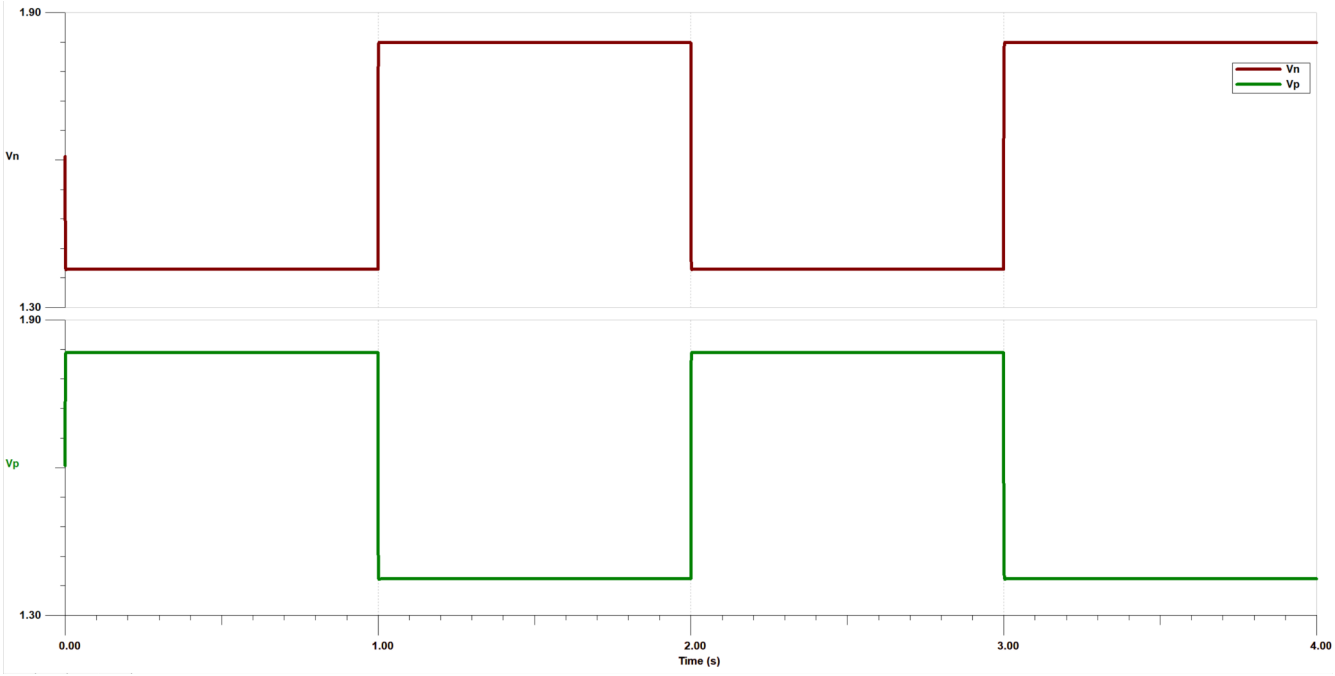

Figure 2-7. Example AB switch toggling mode waveform

2.2 Addressing Large Time Constant Cases

In the previous example, no significant RC settling time before the ADC measures Vp and Vn is assumed. In some conditions, such as the example in Figure 2-8, the time constant can be quite long. Without a workaround, the system can need to wait for a significant amount of time for the voltage to settle and thus fail to meet the standard response time requirements (for example, UL 2231-2 is 10s).

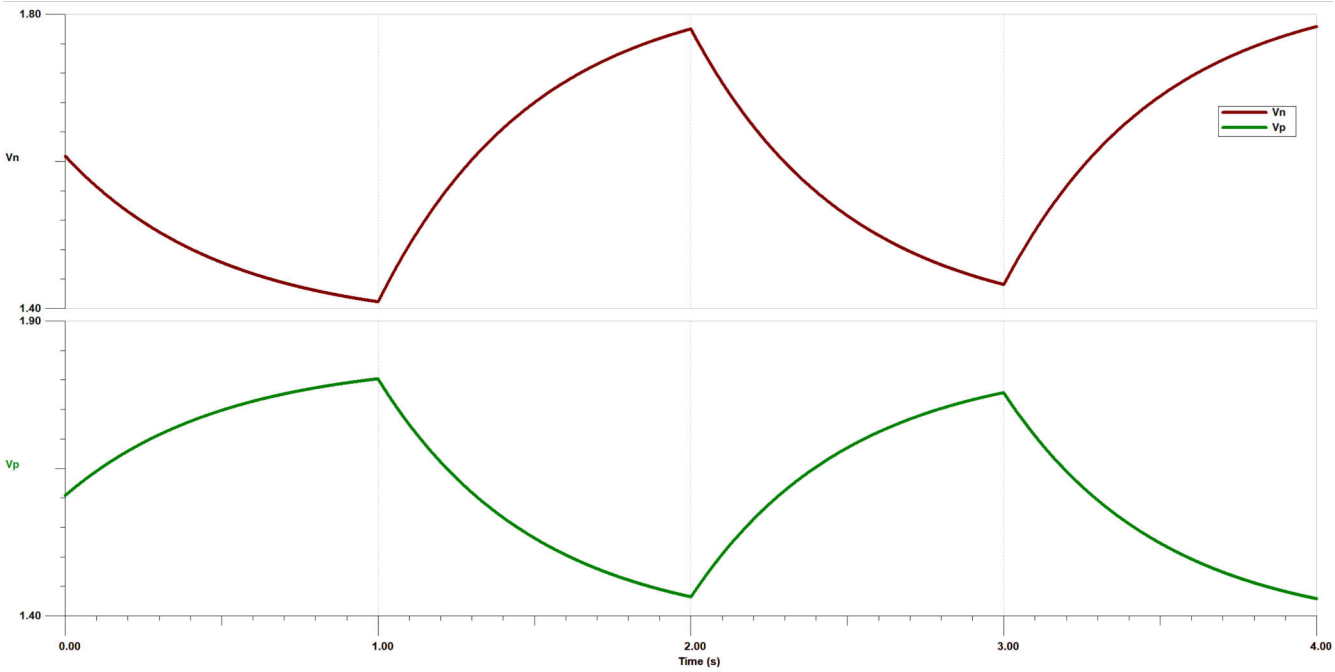

Figure 2-8. Example Waveforms With Large Time Constant

The time constant τ when SW1 is ON and SW2 is OFF:

$$\tau = (\mathrm{RisoP}\,||\,\mathrm{RisoN}\,||\,\mathrm{RsP} + \mathrm{R1}\,||\,\mathrm{RsN}) * (\mathrm{CisoP} + \mathrm{CisoN}) \quad (5)$$

There are a number of ways to address the larger time constant cases (i.e. large Y caps in the µF range)

- Use lower Rsp and Rsn values at the expense of increased power dissipation and leakage current. This is often not practical, since this leads to higher leakage currents, which violates standard requirements.
- Increase the cycle time (for example, from 2s to 3s) to account for the added settling time. This is often not practical with the UL response time limit.
- Use multiple measurements and an algorithm to predict the final settling voltage. When done correctly, this can help extend the IMD operating range without increasing power and time. This topic is discussed in the next section.

2.3 Prediction Algorithms

When SW2 is ON, the response follows the exponential decay equation:

$$V(t) = V_{inf} + V_o e^{\frac{-t}{\tau}} \quad (6)$$

where V_{inf} is the final settled voltage (t = infinity) and V_o is the difference between the initial voltage at time zero, $V(t_0)$, and V_{inf}. Refer to Figure 2-9 to help understand the concept.

The settling voltage, V_{inf}, is of specific interest. The three unknowns in this equation are V_{inf}, τ, and V_o. If the ADC measures three sample voltages at three different times, a system of three equations is created:

$$V(t_0) = V_{inf} + V_o \quad (7)$$

$$V(t_1) = V_{inf} + V_o e^{\frac{-t_1}{\tau}} \quad (8)$$

$$V(t_2) = V_{inf} + V_o e^{\frac{-t_2}{\tau}} \quad (9)$$

By using $t_2 = 2*t_1$, the equations become:

$$V(t_0) = V_{inf} + V_o \quad (10)$$

$$V(t_1) = V_{inf} + V_o e^{\frac{-t_1}{\tau}} \quad (11)$$

$$V(t_2) = V_{inf} + V_o e^{\frac{-2t_1}{\tau}} \quad (12)$$

Now, let $x = e^{\frac{-t_1}{\tau}}$ and the equations become:

$$V(t_0) = V_{inf} + V_o \quad (13)$$

$$V(t_1) = V_{inf} + V_o x \quad (14)$$

$$V(t_2) = V_{inf} + V_o x^2 \quad (15)$$

The calculation for V_{inf} is heavily simplified:

$$V_{inf} = \frac{V(t_0)*V(t_2) - V(t_1)^2}{V(t_0) - 2V(t_1) + V(t_2)} \quad (16)$$

- Note that only four-function arithmetic is needed to compute the V_{inf}. Once V_{inf} is calculated, V_o can be calculated by subtracting V_{inf} from $V(t_0)$.
- In theory, the location of t_0 on the decay curve does not matter as long as t_1 and t_2 are spaced appropriately relative to each other. Specifically, users must keep the same time difference between the three samples. For longer time constants, the voltage settling curve can be relatively flat for the same cycle time. In noisy

conditions, increasing the time spacing between the three samples increases SNR and thus improves the prediction algorithm performance.

The MATLAB script used to solve for the system of equations is:

```
%% solution for exponential decay
clc
syms vt0 vt1 vt2 vinf v0 x
eq1 = vt0 == vinf+v0;
eq2 = vt1 == vinf+v0*x;
eq3 = vt2 == vinf+v0*x*x;
eq4 = vt0 ~= vt1;
eqns = [eq1, eq2, eq3, eq4];
[vinf, v0, x, para, conditions] = solve(eqns,[vinf, v0, x],ReturnConditions=true)
```

In the TIDA-010985 default code, the time spacing between the three samples is 330ms. This verifies the total IMD measurement cycle time is under 2s while making the fixed-point computation straightforward. To change the default cycle time, the user can do one of the following:

- Change the E1 #define in IMD.c. For example, changing E1 #define from 990 to 600 (ms) decreases the IMD cycle time from approximately 2s to approximately 1.2s. The exact time depends on a few milliseconds (ms) of computation (approximately 2ms) after the data acquisition period. If the user wants to increase the cycle time for some reason, the data buffer "SamplesSize" must be changed accordingly in addition to E1 #define. Without changing the default ADC sampling period, increasing the data buffer may be limited due to available SRAM (32 kB total):

```
#define SamplesSize 2000 // ADC buffer size
#define E1 990 // total time for Riso measurement is 2xE1 in ms
```

- Change the ADC sampling interval by changing the TIMER_0 period in syscfg (e.g. from 1 ms to 0.5 ms). This requires some changes to the rest of the code since the code assumes the default 1-ms ADC sampling period.

The time constant is calculated with the following equation:

$$\tau = \frac{-V_o}{V'(t_0)} \tag{17}$$

For isolation resistance, only V_{inf} is necessary. For the total system Y-cap (CisoP + CisoN), approximate V'(t) at t_0 with two adjacent ADC measurements. Then Ciso is:

$$\text{Ciso} = \frac{\tau}{\text{RisoP}\,||\,\text{RisoN}\,||\,\text{RsP} + \text{R1}\,||\,\text{RsN}} \tag{18}$$

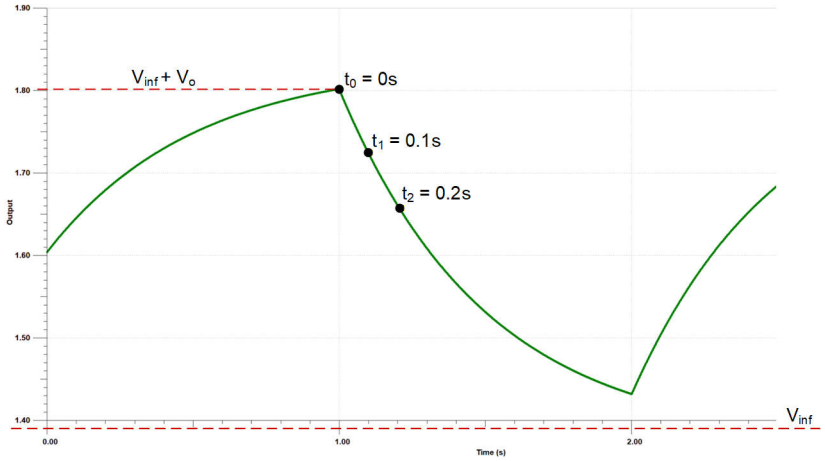

Figure 2-9. Example Voltage Decay Curve with ADC Samples Used for Prediction Algorithm

A similar analysis can be done for the charging curve. If the ADC measures three sample voltages at three different times, a system of three equations is created for the charging curve:

$$V(t_0) = V_i \tag{19}$$

$$V(t_1) = V_i + V_o\left(1 - e^{\frac{-t_1}{\tau}}\right) \tag{20}$$

$$V(t_2) = V_i + V_o\left(1 - e^{\frac{-t_2}{\tau}}\right) \tag{21}$$

Note that V_i is the initial voltage at t_0 time. By using $t_2 = 2*t_1$, the equations become:

$$V(t_0) = V_i \tag{22}$$

$$V(t_1) = V_i + V_o\left(1 - e^{\frac{-t_1}{\tau}}\right) \tag{23}$$

$$V(t_2) = V_i + V_o\left(1 - e^{\frac{-2t_1}{\tau}}\right) \tag{24}$$

Now, let $x = e^{\frac{-t_1}{\tau}}$ and the equations become:

$$V(t_0) = V_i \tag{25}$$

$$V(t_1) = V_i + V_o(1 - x) \tag{26}$$

$$V(t_2) = V_i + V_o\left(1 - x^2\right) \tag{27}$$

Note, the steady state voltage, V_{inf}, is:

$$V(t = \infty) = V_{inf} = V_i + V_o \tag{28}$$

The calculation for the system of equations is heavily simplified (given $t_2 = 2*t_1$) and thus V_{inf} is:

$$V_{inf} = V(t_0) + \frac{V(t_0)^2 - 2*V(t_0)*V(t_1) + V(t_1)^2}{-V(t_0) + 2*V(t_1) - V(t_2)} \tag{29}$$

The MATLAB script used to solve for the system of equations is:

```
%% charging solution
clc
syms vt0 vt1 vt2 vi v0 x
eq1 = vt0 == vi;
eq2 = vt1 == vi+ v0*(1-x);
eq3 = vt2 == vi+ v0*(1-x*x);
eq4 = vt0 ~= vt1;
eqns = [eq1, eq2, eq3, eq4];
%
[svi, sv0, sx, para, conditions] = solve(eqns,[vi, v0, x],ReturnConditions=true)
```

One important consideration is knowing when to apply the prediction algorithm. If the voltage has a fast settling time, the prediction algorithm is not needed. It is more practical to just wait a little longer in time before solving for Riso or Ciso. Currently, the SW does some basic checks based on the voltage time derivative (normalized

by the Vbus voltage) to set a threshold for prediction mode. This method does require some tuning with known loads to verify reliable operation. These are the possible operating modes in the code:

```
#define SETTLED_MODE
#define DECAY_MODE
#define CHARGE_MODE
#define OUT_OF_RANGE_MODE
```

2.4 Understanding Error Sources

The MSPM0G3507 only supports fixed-point math, and thus some consideration of number overflow is required to minimize error and/or loss of precision. The current code is optimized to maintain precision and accuracy where it matters most, which is near the fault and warning thresholds. The user can avoid this challenge by switching to an MCU with floating-point math support.

Component tolerances are specifically chosen to meet the design target accuracy. Some passives such as the RES60A resistors have a maximum absolute tolerance of 15%, affecting measurement accuracy when the Riso is in the MΩ range. However, this is not important since the highest accuracy closer to the fault trip point of 100Ω/V is desired. For a 1kV bus, that is 100kΩ. At this level, the RES60A tolerance is not significant for a 5% accuracy target. However, the equivalent resistance reading must be compensated for the paralleling of RES60A and other resistances.

So far, the IMD is assumed to work under exceptional conditions without noise, providing a good place to start understanding the fundamental concepts. In practice, TIDA-010985 performance is heavily dependent on how well noise is controlled. These are the steps to help mitigate noise for this design:

- HW filtering to limit input noise
- Follow PCB layout guidelines to optimize SNR
- ADC HW averaging (default is set to 128)
- SW averaging of multiple ADC readings or predictions to estimate the steady-state voltage. For non-prediction-based IMD calculations, the SW averages 50 adjacent ADC samples to estimate the settled voltage.
- For prediction-based IMD calculations, the SW averages 330 predictions to estimate the settled voltage (i.e. Vp1, Vn1, Vp2, Vn2). Longer time constants create flatter voltage settling curves and decrease prediction accuracy under noisy conditions. As mentioned previously, increasing the time spacing between the three samples can help improve prediction performance.

2.5 Test Results

The key test results of TIDA-010985 are shown in Figure 2-10 and Figure 2-11. Each test condition includes ten IMD measurements for statistical analysis (mean and standard deviation). Fixed-point math error is significant in some cases. Overall, the measurement errors and response time were well below the UL 2231-2 requirements (±15%, 10 seconds). For Figure 2-10 below, for asymmetric faults, the error displayed is the Riso in the fault condition. The 1MΩ-1MΩ case requires a 3-s cycle to resolve due to a very large time constant.

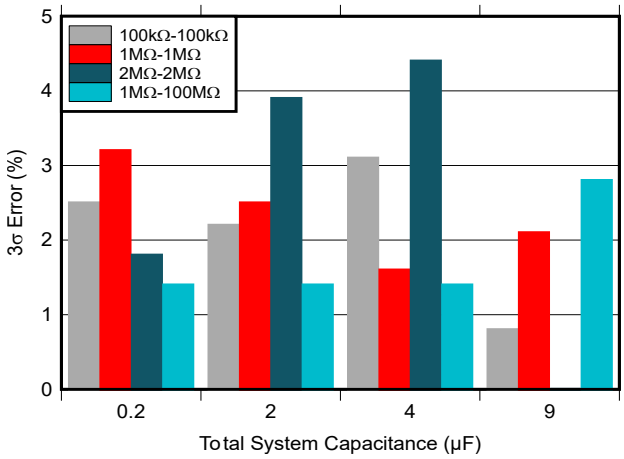

Figure 2-10. IMD Riso Measurement Error, 1000VDC, 2s Cycle

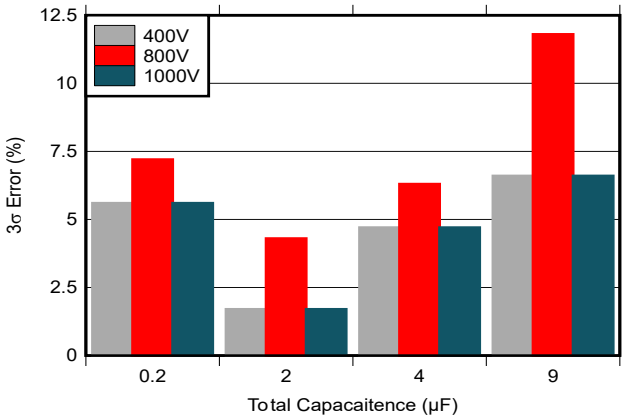

Figure 2-11. IMD Ciso Error, 1MΩ-100kΩ, 2s Cycle

3 Summary

This application note discusses the key design considerations for a resistive-bridge insulation monitor based on TIDA-010985. The key design challenge discussed here is how to address large Y-cap applications while considering the trade-offs. The current design is able to support up to 9µF with the help of a novel predictive algorithm software. For more information on the TIDA-010985 IMD reference design and design resources, please visit ti.com.

4 References

1. Texas Instruments, *Resistive-Bridge Insulation Monitoring Device for 800V DC Systems With Large Y Cap Reference Design*, design guide.
2. Texas Instruments, *AFE for Insulation Monitoring in High-Voltage EV Charging & Solar Energy RefDes*, design guide.

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Last updated 10/2025