Application Note

Debugging Methodology for DisplayPort/embedded DisplayPort Link Training Utilizing the Auxiliary Channel

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ABSTRACT

This application note provides a comprehensive guide to DisplayPort and embedded DisplayPort (DP/eDP) link training by emphasizing debugging methodologies that use DisplayPort Configuration Data (DPCD) registers and Auxiliary (AUX) channel signal analysis. The document begins by explaining the fundamental architecture of the DP/eDP link and the operational principles of the AUX channel. Subsequently, this document details the complete DP/eDP link training procedure, highlighting potential failure points at clock recovery, channel equalization, symbol lock, and inter-lane alignment stages, and presents targeted debugging strategies. Lastly, the document provides instructions for implementing a differential-to-single-ended conversion circuit using the DS90LV011-12AEVM evaluation module, along with guidance on protocol analyzer configuration, AUX signal acquisition procedures, and AUX data format interpretation. Note that all information in this application note is based on DP v1.4a and eDP v.1.4b standards.

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Trademarks

1 Introduction

The DP/eDP interface, developed by the Video Electronics Standards Association (VESA), is a mainstream high-definition video transmission standard widely used in computers, monitors, and other displays. The DP/eDP interface consists of multiple functional channels, including an Auxiliary (AUX) channel, Hot Plug Detect (HPD), and main link. Notably, the AUX channel plays an indispensable role in verifying stable and efficient communication between the DP/eDP source and sink devices.

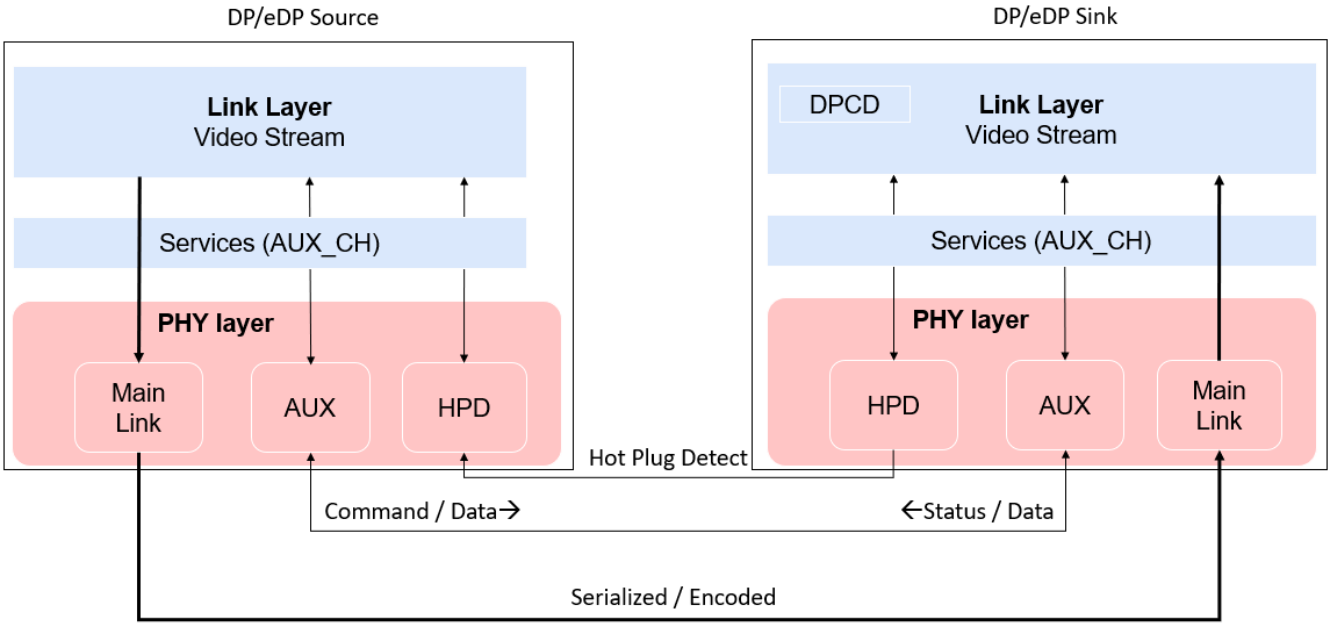


Figure 1-1. DP/eDP Architecture

2 DP/eDP Link Training Procedure and Debugging Methodology

2.1 Link Training Procedure

DP/eDP link training is the initialization process to verify stable video transmission through the interface. Link training is triggered by the HPD signal from the sink, which indicates the presence of the sink. As shown in Figure 2-1, this process cycles through device capability reading, clock recovery, channel equalization, symbol lock and inter-lane alignment, and realizes video stream transmission upon completion.

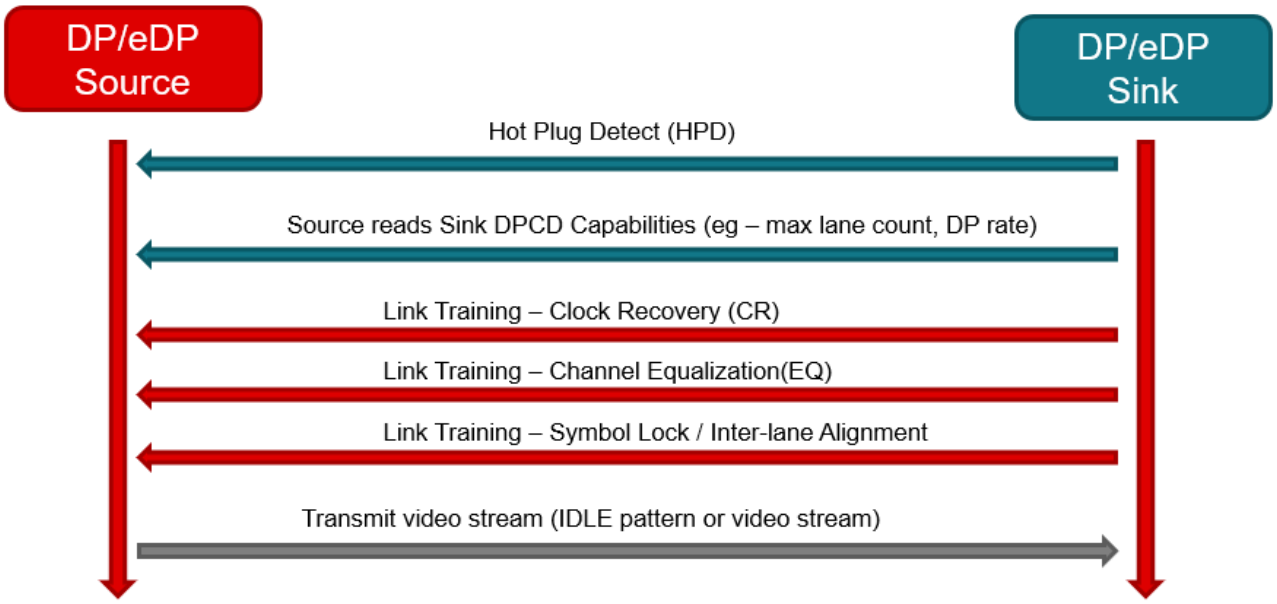
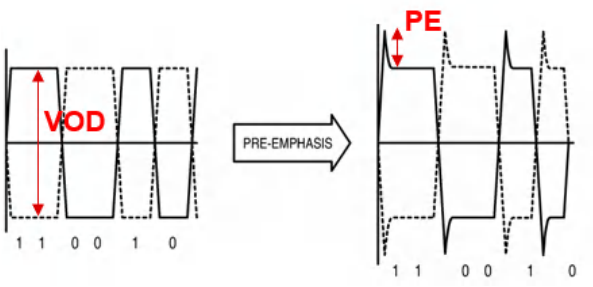


Figure 2-1. DP/eDP Link Training Procedure

1. **HPD Trigger and DPCD Capability Reading:** After the physical connection between the sink and source is established, the sink pulls up the HPD signal to notify the source to establish communication. Upon detecting the HPD signal is pulled high, the source reads the DPCD registers of the sink through the AUX channel to obtain core capability parameters, including maximum lane count, supported lane speed, voltage swing, and pre-emphasis levels.
2. **Clock Recovery:** This is the first step of link training. Since the DP/eDP interface does not include an independent clock line, clock recovery is when the sink attempts to recover a synchronous clock from the data stream of the source. The source transmits TPS1 at the highest supported DP/eDP lane speed by the sink, lowest voltage swing (VOD), and lowest pre-emphasis (PE). VOD adjusts the differential voltage swing and amplitude, and pre-emphasis modifies the overshoot to the signal as the overshoot leaves the transmitter. The source then checks the DPCD Registers 00202h and 00203h bits 4 and 0 LANEx_CR_DONE through the AUX channel. This process lasts 100µs for all interval settings defined in DPCD Register 0000Eh TRAINING_AUX_RD_INTERVAL. If all LANEx_CR_DONE bits report back 1, then clock recovery is successful. If any LANEx_CR_DONE bits report back 0, then the VOD/PE combination increments upwards and the training pattern is re-transmitted for another 100µs. If the clock is not recovered after five times with the same lane speed, the source then reduces the lane speed, restarts from the lowest VOD/PE combination, and cycles until the clocks are successfully synchronized, or until it fails with the maximum VOD/PE combination at the lowest speed. Valid VOD/PE combinations are shown in Figure 2-2. VOD and PE cannot add to be greater than three.



Valid VOD/PE combinations:

	PRE0	PRE1	PRE2	PRE3
VOD0	**OK**	**OK**	**OK**	**OK**
VOD1	**OK**	**OK**	**OK**	*NOK*
VOD2	**OK**	**OK**	*NOK*	*NOK*
VOD3	**OK**	*NOK*	*NOK*	*NOK*

Figure 2-2. VOD Swing and Pre-Emphasis

3. **Channel Equalization:** Once clock recovery is successful, channel equalization begins with the lane speed and VOD/PE settings defined at clock recovery and the source transmits one of the three pre-defined training patterns – TPS2, TPS3, or TPS4. The sink parses the patterns to detect signal distortion, dynamically adjusting equalizer parameters and feeding back the status through the DPCD Registers 00202h and 00203h bits 5 and 1 LANEx_CHANNEL_EQ_DONE to verify signal integrity on the DP/eDP lanes.
4. **Symbol Lock and Inter-Lane Alignment:** Symbol lock requires the sink to accurately identify 8b/10b encoding symbol boundaries with a Bit Error Rate (BER) less than 10^{-9} and sets DPCD Registers 00202h and 00203h bits 6 and 2 LANEx_SYMBOL_LOCKED upon meeting the standard. Inter-lane alignment adjusts the delay of each lane to achieve data synchronization, indicating proper alignment of all lanes through DPCD Register 00204h bit 0 INTERLANE_ALIGN_DONE.
5. **Video Stream Transmission:** After all training steps are successful, the source notifies the sink of training completion via the DPCD Registers 00202h LANE0_1_STATUS, 00203h LANE2_3_STATUS, and 00204h LANE_ALIGN_STATUS_UPDATED. The source stops transmitting training patterns and starts transmitting either IDLE patterns or video streams.

2.2 Debug Guide for Link Training Failure

2.2.1 Debugging Points when Clock Recovery is Not Successful

Correct transmission of the test pattern TPS1 is key to clock recovery. The following issues can impact the transmission of the TPS1 pattern:

1. Improper PCB layout, causing signal integrity issues
   - DP/eDP trace layout considerations are listed here:
     - Make sure that DP traces are routed with 100Ω ± 10% differential impedance. When using eDP, if direct trace connection is used instead of an eDP connector, then route with 100Ω ± 10% trace impedance. If an eDP connector is used, then route with 85Ω ± 15% trace impedance.
     - Length match to avoid intra and inter-pair skew.
     - Route traces on layers adjacent to ground. Avoid routing traces adjacent to power planes. TI recommends burying traces in an inner layer to reduce EMI impact.
     - Prevent via stubs to reduce signal reflections.
     - Provide enough space between traces to reduce crosstalk.
     - Do not add test points to the traces.
   - A useful diagnostic is checking the eye diagram of the DP/eDP signals. To improve the eye, make sure jitter is within specifications and follow layout considerations as listed above.
2. Voltage swing and pre-emphasis minimum voltage levels are not met
   - Make sure voltage swing and pre-emphasis voltages meet the specifications for TPS1 pattern transmission.

2.2.2 Debugging Points when Channel Equalization is Not Successful

Similar to the clock recovery stage, make sure proper layout and voltage swing/pre-emphasis minimum voltage levels meet the DP/eDP standard for the predefined pattern (TPS2, TPS3, or TPS4).

2.2.3 Debugging Points when Symbol Lock and Inter-Lane Alignment is Not Successful:

If the symbol lock stage is unsuccessful, the digital PHY layer has not successfully aligned the symbol boundaries.

1. Check symbol errors for each lane through DPCD Registers (DPCD 00210h – 00211h for lane 0, 00212h – 00213h for lane 1, and so on) to determine if there are transmission errors on specific lanes.
2. Meet DP/eDP specifications for inter-lane skew (for example, between lane 0 and lane 1) and intra-lane skew (between P and N traces on each lane).

3 DP/eDP AUX Channel Signal Overview

The AUX channel is a half-duplex bidirectional channel which operates at approximately 1Mbps transfer rate. This is the communication method between source and sink and carries management and device control data.

3.1 AUX Transaction Types

The AUX channel supports native AUX operations and I2C-over-AUX operations.

Native AUX operations include AUX writes and reads to DPCD registers shared between the source and sink. DPCD registers contain device capability information, status information, and various configuration parameters.

I2C-over-AUX operations is a type of AUX channel command intended to carry standard I2C communication over the AUX lines. I2C-over-AUX operations can be used for efficiently accessing and transporting EDID information, bypassing the external I2C controller and target interface.

3.2 DPTX and DPRX AUX Design Guidance

3.2.1 DP/eDP Implementation

Figure 3-1 shows a typical AUX hardware implementation for DP. The discrete components are required to verify proper AUX operation. Note that the typical value of C_AUX is 0.1µF.

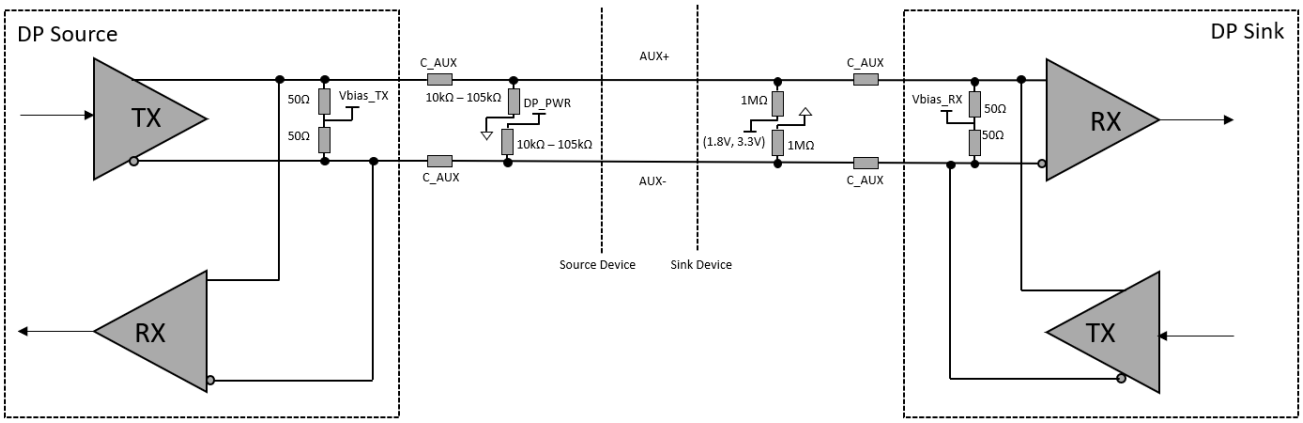


Figure 3-1. DP AUX CH Differential Pair

Figure 3-2 shows the eDP AUX hardware implementation.

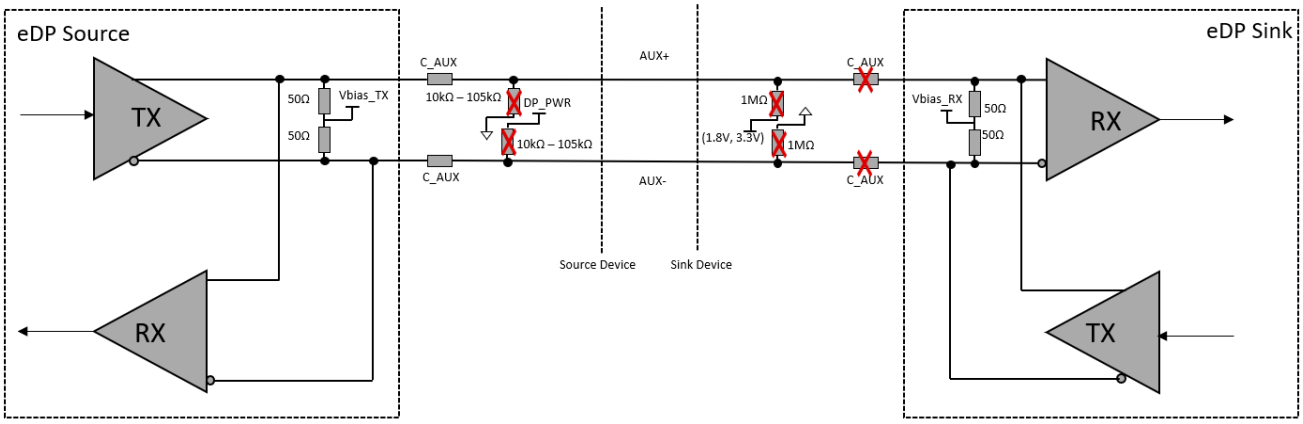


Figure 3-2. eDP AUX CH Differential Pair

Red marked components are not required. eDP stuffing options are listed:

Stuffing Option 1:

1. Source side pull-up/pull-down = 100kΩ
2. Sink side pullup/pulldown = 1MΩ
3. Sink side C_AUX = 100nF

Stuffing Option 2:

1. Source side pull-up/pull-down = DNP
2. Sink side pull-up/pull-down = DNP
3. Sink side C_AUX replaced with 0Ω resistor

3.2.2 Electrical Specifications

Table 3-1 lists AUX Channel electrical specifications at typical condition (T=25ºC, nominal VDD). See DP v1.4a and eDP v1.4b specifications for a complete table.

Table 3-1. AUX_CH Electrical Specifications

Symbol	Parameter	Min	Nom	Max	Units
UI_{MAN}	Manchester transaction unit interval	0.4	0.5	0.6	us
Pre-charge pulse	Number of pre-charge pulses	10		16	
	Number of Pulses before SYNC end symbol (DP mode)		16		pulses
	Number of Pulses before SYNC end symbol (eDP mode)		8		pulses
$T_{AUX-BUS-PARK}$	AUX_CH bus park time	10			ns
$T_{cycle-to-cycle\ jitter}$	Maximum allowable UI variation within a single transaction at connector pins of a transmitting device			0.08	UI
	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a transmitting device			0.04	UI
	Maximum allowable UI variation within a single transaction at connector pins of a receiving device			0.1	UI
	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a receiving device			0.05	UI
$V_{AUX-DIFFP-P\_TX}$ (eDP)	AUX Peak-to-peak voltage at TX package pins (TP1)	0.18	0.20	1.38	V
	AUX peak-to-peak voltage at TP3	0.14		1.36	V
$V_{AUX-DIFFP-P\_TX}$ (DP)	AUX peak-to-peak voltage from Main-Link Source/Sink when transmitting	0.29	0.40	1.38	V
$V_{AUX-DIFFP-P\_RX}$ (DP)	AUX peak-to-peak voltage received by Main-Link Source, TP2	0.27		1.36	V
	AUX peak-to-peak voltage received by Main-Link Sink, TP3	0.27		1.36	V
$V_{AUX-DC-CM}$ (eDP)	AUX DC common mode voltage	0		1.2	V
$V_{AUX-DC-CM}$ (DP)	AUX DC common mode voltage	0		2.0	V
$V_{AUX-TURN-CM}$	AUX turnaround common mode voltage	0		0.3	V
I_{AUX_SHORT}	AUX short circuit current limit			90	mA
C_{AUX}	AUX AC-coupling capacitor	75		200	nF

3.2.3 AUX EYE Diagram

Figure 3-3 and Figure 3-4 show the eye diagram test criteria for DP and eDP AUX channels, respectively. See DP v1.4a and eDP v1.4b specifications for a complete design guide.

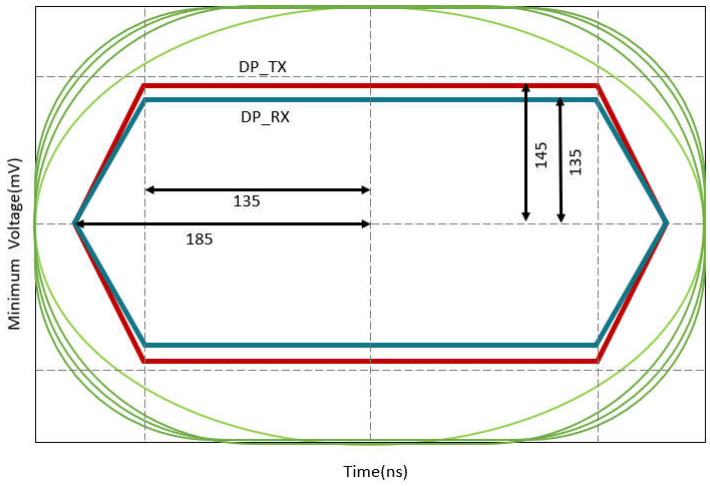


Figure 3-3. DP AUX_CH EYE Mask

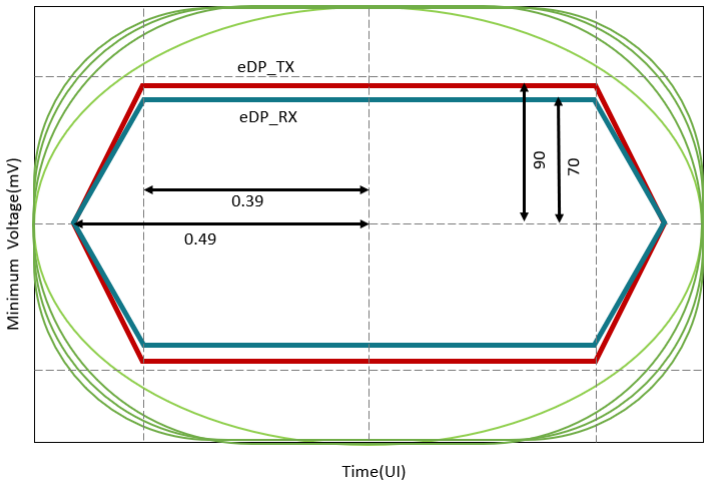


Figure 3-4. eDP AUX_CH EYE Mask

4 Decoding AUX Channel Signal

Since the AUX channel is responsible for key functions such as link training, device enumeration, and real-time control signal transmission between the DP/eDP source and sink, monitoring the channel is useful.

4.1 AUX Transaction Syntax

As previously mentioned, the AUX channel uses a half-duplex communication mode, and the data transmission strictly complies with the Manchester-II transaction format.

The SYNC Pattern serves as the start identifier of a data frame. This pattern consists of 16 to 32 consecutive logical 0s encoded in Manchester-II and the purpose is to achieve receiver synchronization and accurate identification of data frames.

Then, a SYNC END/START signal is transmitted, defined as two HIGH clock cycles and two LOW clock cycles.

Then, the 4-bit Manchester-II encoded Command (CMD) field is transmitted. This field is used to specify the operation type, such as DP/eDP write operation (80h) and DP/eDP read operation (90h). Following the CMD field are the Address (ADDR) field and Data (DATA) field in sequence.

The ADDR field is used to designate the target register or memory location for the operation, while the DATA field carries the specific information to be transmitted.

The end of the frame structure is the STOP signal, which has the same format as SYNC END/START and is used to mark the termination of the data transmission of the frame. More information regarding specific AUX transaction formats can be found in the DP v1.4a specification.

4.2 How To Use DS90LV011-12AEVM to Capture DP/eDP AUX Channel Signal

Since DP/eDP uses a differential signaling scheme, it is difficult to capture the AUX channel using conventional test tools that only support single-ended signals. To address this technical challenge, this design utilizes the dedicated differential-to-single-ended conversion evaluation module DS90LV011-12AEVM.

Note that the DS90LV011-12AEVM includes both the DS90LV011A and DS90LV012A modules, but the differential-to-single-ended conversion function is implemented by using the DS90LV012A module only. The core technical features are as follows:

- Input differential signal rate: Supports all DP/eDP AUX channel rates
- Supply voltage: Supports 3.3V single power supply operation
- Output level: Compatible with 3.3V CMOS/TTL level standards

For more information on the DS90LV011-12AEVM, see the *DS90LV011-12AEVM User's Guide*.

The implementation block diagram is shown in Figure 4-1. To connect to the AUX lines, solder wires onto the EVM on the side of the capacitor where there are pull-up / pull-down resistors (solid red circles). In circumstances where the common mode voltage exceeds the VDD (3.3V) of the DS90LV012A, solder the wires on the other side of the capacitors (dotted red circles) to avoid negatively impacting the LVDS receiver.

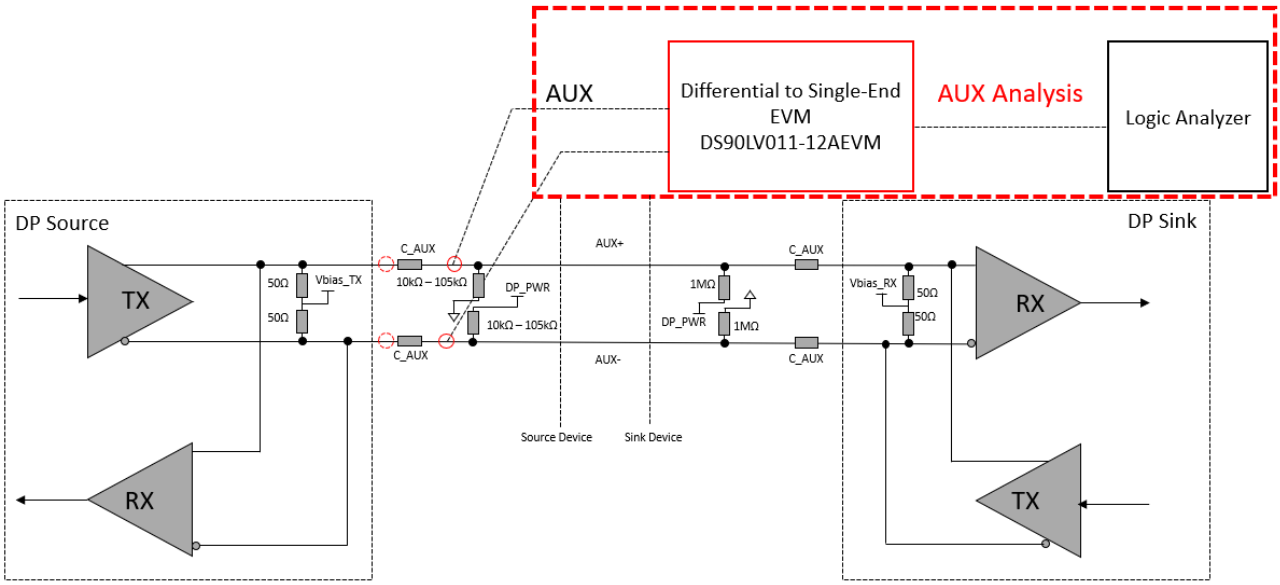
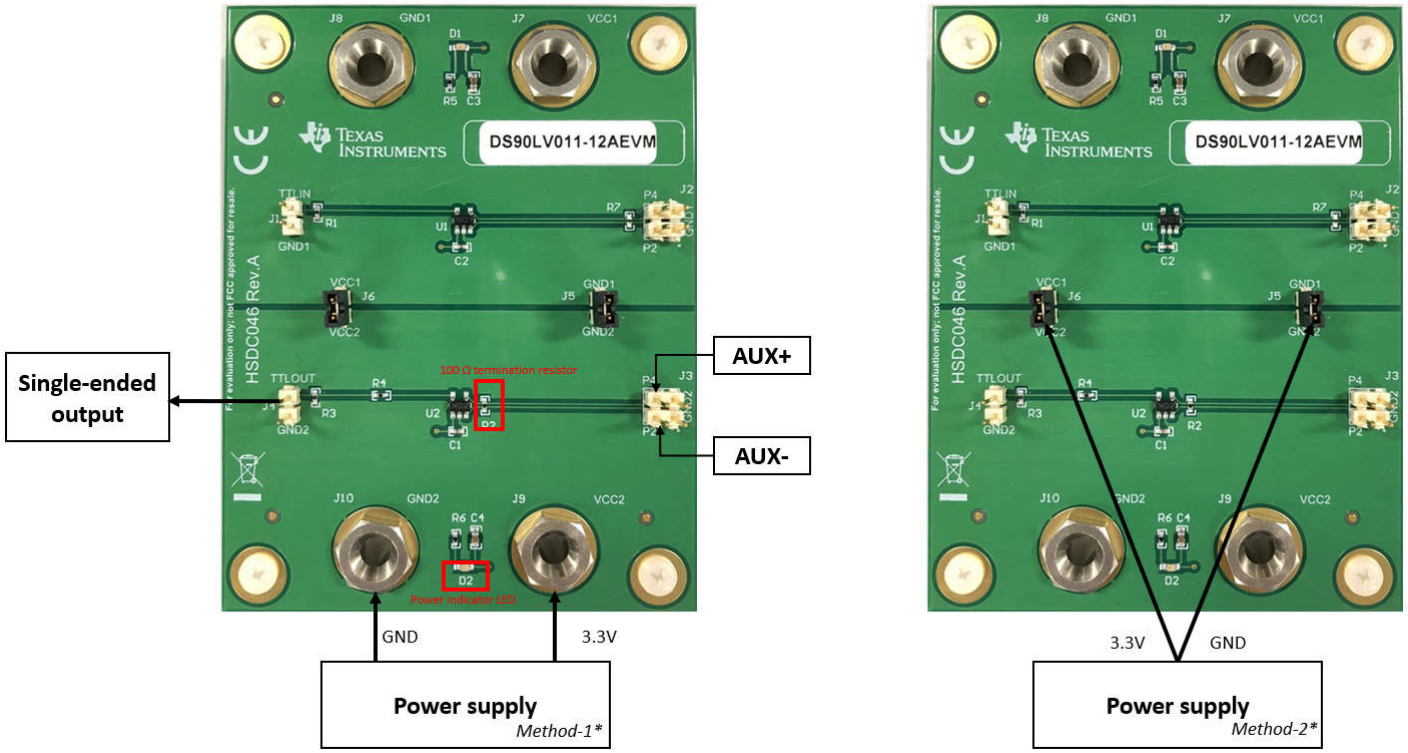


Figure 4-1. Block Diagram Integrating DS90LV011-12AEVM

The hardware connection for capturing the AUX signal using the DS90LV011-12AEVM is shown in Figure 4-2.

There are two ways to power on the DS90LV011-12AEVM – using banana jacks J9 and J10 or using jumper hook wires on J5 and J6. If properly powered, D2 lights up.

Connect the AUX differential signal to J3 (AUX+ to P4 and AUX- to P2) and connect the J4 TTLOUT signal to the single-ended logic analyzer. Verify the logic analyzer is set to parse at 3.3V to match the EVM output voltage. To measure the LVDS signals properly, the EVM features a 100Ω termination resistor R2 across the differential pairs at the point of measurement.



*Note that VCC1 and GND1 can also be used to power the EVM if J5 and J6 are populated.

Figure 4-2. DS90LV011-12AEVM Configuration to Capture AUX Channel

4.3 AUX Channel Decoding Methodology

To properly decode AUX channel signals, the hardware must be implemented correctly. More specifically, AUX polarities must be matched between EVM and the AUX channels. With properly matched AUX polarities, each AUX transaction includes both a SYNC END/START and STOP sequence as depicted in Figure 4-3. Conversely, a hardware implementation with swapped AUX polarities does not have a SYNC END/START or STOP sequence as shown in Figure 4-4.

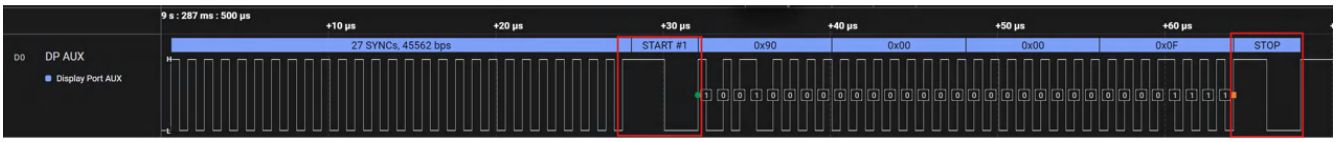


Figure 4-3. Proper Polarities AUX Transaction

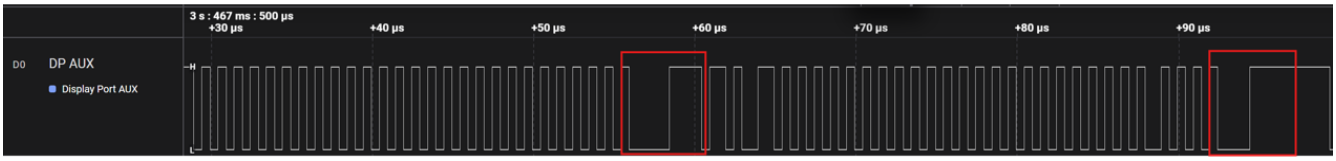


Figure 4-4. Swapped Polarities AUX Transaction

If AUX polarities are found to be incorrect, swap the AUX+ and AUX- wires on the DS90LV011-12AEVM.

Upon capturing the AUX channel, using a dedicated AUX analyzer extension enables efficient parsing of captured signals. Figure 4-5 shows the AUX waveform decoded by utilizing this AUX analyzer extension, which can be applied to the Logic 2 analyzer.

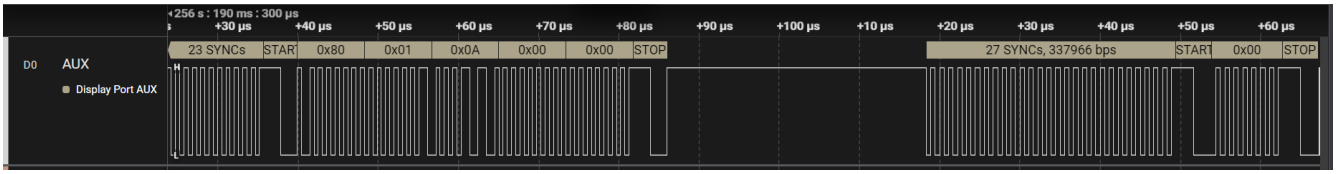


Figure 4-5. Logic 2 AUX Waveform Utilizing AUX Analyzer Extension

When using Logic 2 software, place the AUX analyzer extension in the Logic\resources\windows-x64\Analyzers folder, as shown in Figure 4-6.

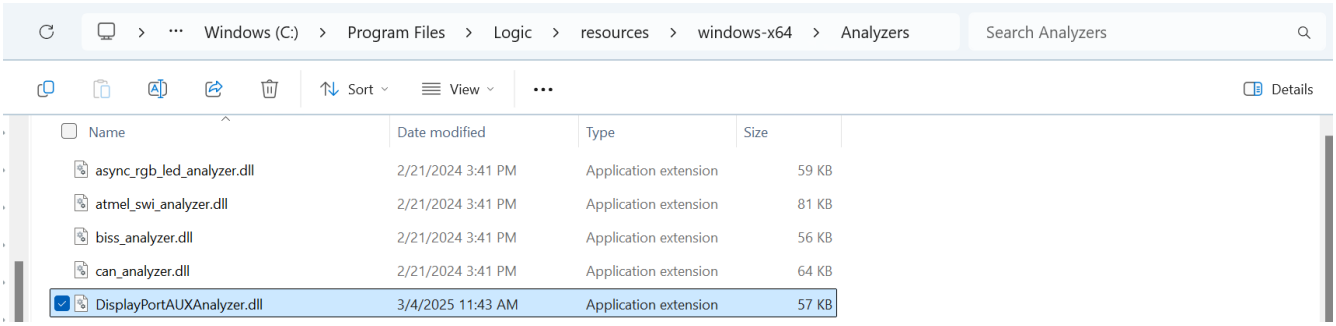


Figure 4-6. AUX Analyzer Extension in Logic 2 Software

To apply the extension on Logic 2, follow these steps:

1. Click on *Analyzers* tab.
2. Add an analyzer.
3. Select Display Port AUX.
4. Set the proper channel to analyze (for example, Channel 00 in Figure 4-7).
5. Click *Save*.

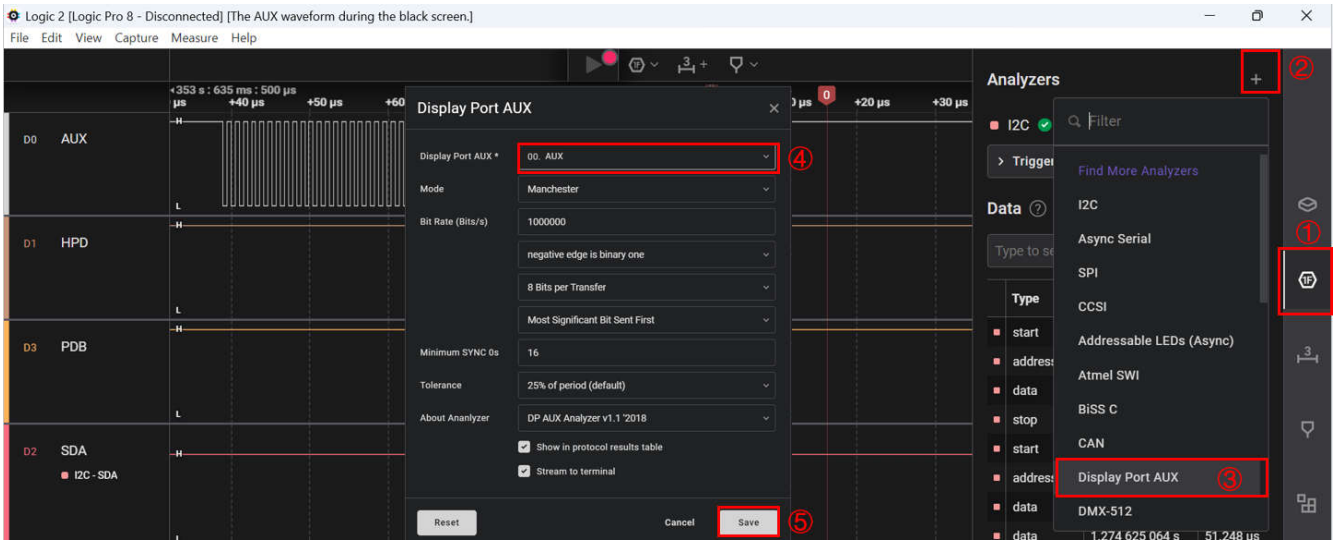


Figure 4-7. Steps to Apply AUX Extension on Logic 2

When using the AUX Analyzer extension, make sure the sampling rate is at least 250MS/s.

4.4 AUX Channel Decoding Example

Figure 4-8 shows native AUX read transactions reporting back DPCD Register 00202h – 00207h. In this capture, 00202h and 00203h report back 0x77 and 00204h report back 0x81, indicating a successful 4-lane link training sequence.

Similarly, Figure 4-9 shows a native AUX write transaction. As per DP/eDP specifications, DPCD Register 00101h is used to determine the number of DP/eDP lanes. This example demonstrates the source writing 84h to this register through the AUX channel, specifying that link training is performed in 4-lane mode.

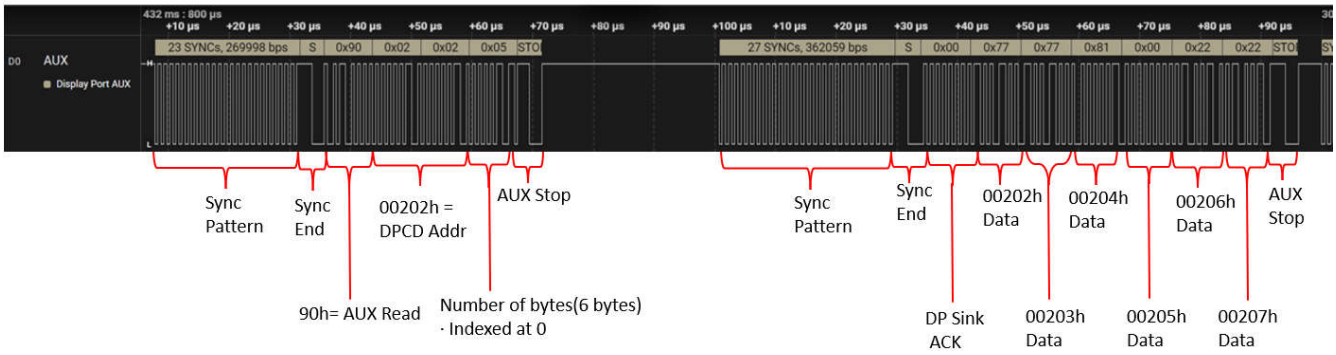


Figure 4-8. Native AUX Read Transaction

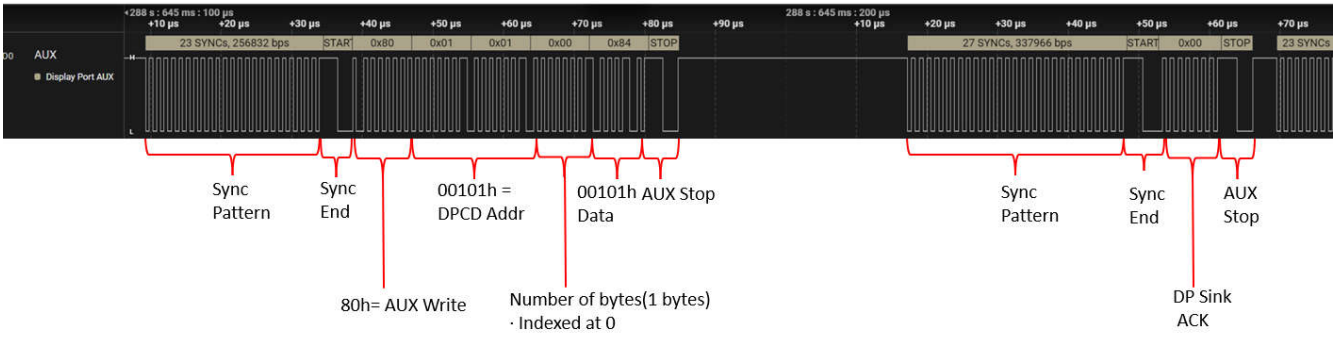


Figure 4-9. Native AUX Write Transaction

5 Summary

Overall, this application note presents a practical engineering guide for DP/eDP link training technology with emphasis on systematic debugging approaches and AUX channel signal analysis techniques. Most notably, this document presents a complete implementation methodology using the DS90LV011-12AEVM differential receiver evaluation module for signal conversion, enabling engineers to diagnose and resolve link training issues efficiently through validated measurement techniques.

6 References

1. Texas Instruments, *DS90UB983-Q1 4K DisplayPort/eDP to FPD-Link IV Bridge Serializer*, datasheet.
2. Texas Instruments, *DS90UB984-Q1 4K FPD-Link IV to DisplayPort/eDP Bridge Serializer*, datasheet.
3. VESA, DisplayPort Standard v1.4a
4. Texas Instruments, *DS90LV012A / DS90LT012A 3-V LVDS Single CMOS Differential Line Receiver*, datasheet.
5. Texas Instruments, *DS90LV011-12AEVM User Guide*, user's guide.
6. Github (Alex-the-Smart), *AUX Analyzer*, webpage.
7. Saleae, *Logic 2 Software*, software.

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