

Application Note

OSFP Applications for TPLD



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ABSTRACT

This application note explores how Texas Instruments' Programmable Logic Devices (TPLD) can be configured to support Octal Small Form-factor Pluggable (OSFP) applications in high-performance computing environments such as data centers and AI computing clusters. TPLD supports single and multiple host controllers within a single device, provides I²C integration to reduce system signal line count, provides module controller options, and offers additional features that extend functionality of the system. These options enable OSFP system designers to meet OSFP MSA standards across both host and module controllers with flexibility and efficiency.

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1 Introduction

OSFP (Octal Small Form-factor Pluggable) is a high-performance pluggable form factor featuring eight high-speed electrical lanes designed to meet the demanding thermal and signal integrity requirements of data centers, AI computing centers, and similar high-performance computing clusters. OSFP specifications are governed by a Multi-Source Agreement (MSA) that defines both mechanical and electrical requirements for compliant implementations.

As OSFP adoption grows, system designers need flexible and reliable tools for managing the low-speed signals required by the MSA. Demand for OSFP host-side systems that can support an increasingly large number of modules in smaller footprints add additional challenges. Texas Instruments' Programmable Logic Devices (TPLD) offer several configurations to address these needs for both host and module controllers. This application note describes how TPLD can be configured to support OSFP applications, including: supporting low-speed signals for single or multiple host controllers within a single TPLD2001; utilizing I²C within TPLD to reduce the number of signal lines required by the system; options for module controllers; and additional features that extend system functionality in OSFP applications.

2 Basic Configurations for Host and Module Controllers

The low speed signals for OSFP include the I²C SCL and SDA signals at 3.3V and the multi-level signals LPWn/PRSn and INT/RSTn. These signals are used by the host to configure and control the module. The INT/RSTn signal has three voltage zones defined by the MSA that represent reset mode, normal mode, and interrupts. The LPWn/PRSn signal has three voltage modes that represent low or high power states and whether the module is present or not present. To achieve three distinct voltage levels with devices that typically only have high or low states, the system requires 1% external resistors and a combination of push-pull, open drain, and open collector outputs. The typical setup, showing both module and host, are shown below.

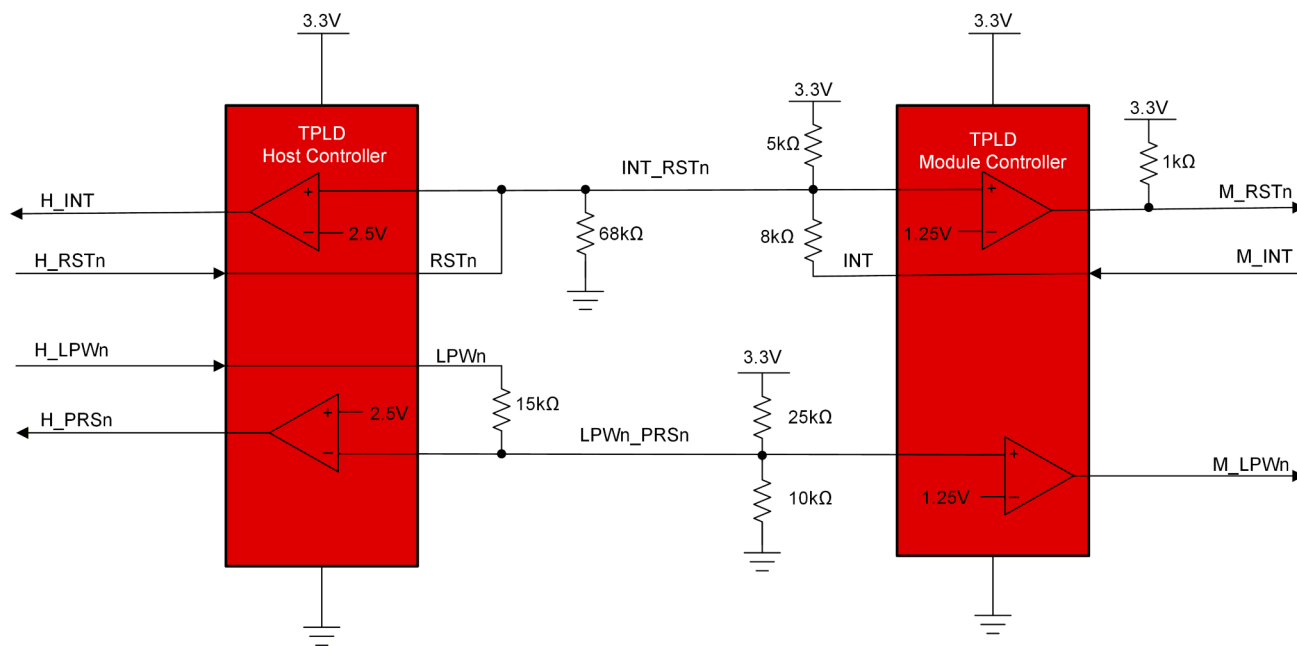


Figure 2-1. TPLD1202 OSFP Host and Module Setup

TPLD that have eight or more GPIOs and two or more analog comparators can be used as a single-channel host controller. TPLDs that have six or more GPIOs and two or more analog comparators can be used as module controllers. For example, TPLD1202 and TPLD2001 are both good options for these basic host and module controller designs.

Table 2-1. Output Types for Host Controller

Output Name	Output Type
RSTn	Open drain NMOS
H_INT	Push-pull
H_PRSn	Push-pull
LPWn	Open Collector

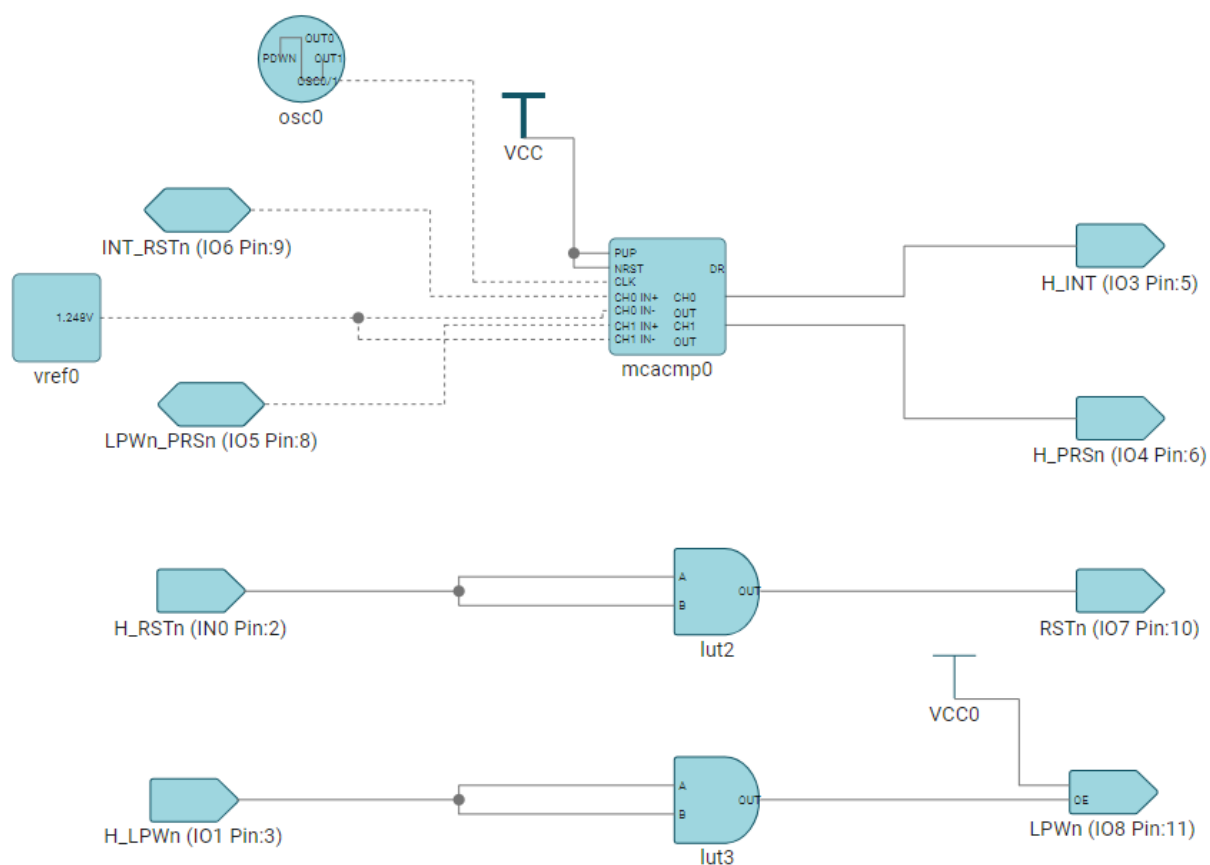


Figure 2-2. TPLD1202 Host Controller InterConnect Studio Implementation

MULTI-CHANNEL ANALOG COMPARATOR ⓘ

Name mcacmp0

Label

Temperature Sensor Input Enable ☐

VCC Input Enable ☐

McACMP Output Synchronicity Staggered

McACMP Trigger Mode Level sensitive EN mode

McACMP Clock Select OSC0/1

Synchronous Edge Select Falling Edge

Channel Amount Sampled 2 Channels

ACMP 0 Settings Settings Specific to ACMP 0

Hysteresis Select Disabled (0mv)

Positive Input Gain 0.50X

IN+ : Positive Input Source AIO1

Reset Enable ☐

Amount of Voltage References 1 VREF

IN- : Voltage Select 1.248V

ACMP 1 Settings Settings Specific to ACMP 1

Hysteresis Select Disabled (0mv)

Positive Input Gain 0.50X

IN+ : Positive Input Source AIO0

Reset Enable ☐

Amount of Voltage References 1 VREF

IN- : Voltage Select 1.248V

Device MacroCell Allocated MCACMP

Figure 2-3. TPLD1202 Host Controller InterConnect Studio Settings

Table 2-2. Output Types for Module Controller

Output Name	Output Type
M_RSTn	Open drain NMOS
INT	Open drain NMOS
M_LPWn	Open drain NMOS

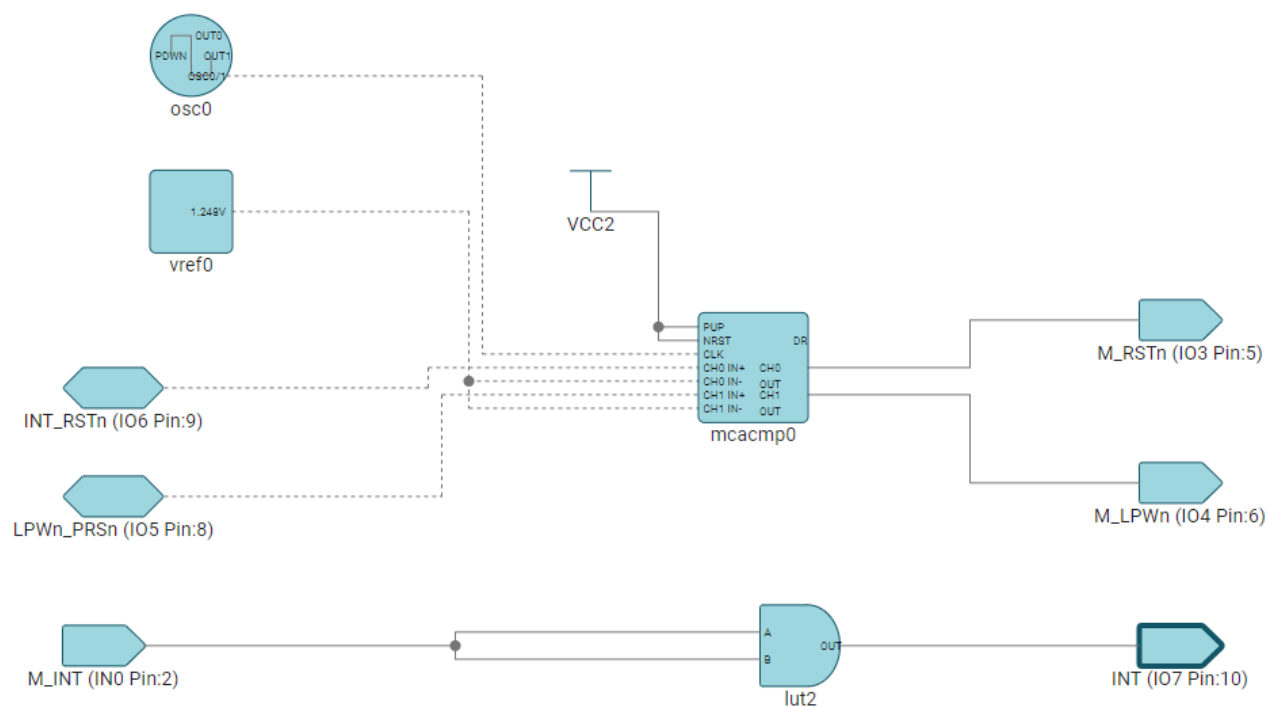


Figure 2-4. TPLD1202 Module Controller InterConnect Studio Implementation

MULTI-CHANNEL ANALOG COMPARATOR ⓘ

Name

mcacmp0

Label

Temperature Sensor Input Enable ⓘ

☐

VCC Input Enable

☐

McACMP Output Synchronicity

Staggered

▼

McACMP Trigger Mode

Level sensitive EN mode

▼

McACMP Clock Select

OSC0/1

▼

Synchronous Edge Select

Falling Edge

▼

Channel Amount Sampled

2 Channels

▼

ACMP 0 Settings

Settings Specific to ACMP 0

^

Hysteresis Select

Disabled (0mv)

▼

Positive Input Gain

1.00X

▼

IN+ : Positive Input Source

AI01

▼

Reset Enable

☐

Amount of Voltage References

1 VREF

▼

IN- : Voltage Select

1.248V

▼

ACMP 1 Settings

Settings Specific to ACMP 1

^

Hysteresis Select

Disabled (0mv)

▼

Positive Input Gain

1.00X

▼

IN+ : Positive Input Source

AI00

▼

Reset Enable

☐

Amount of Voltage References

1 VREF

▼

IN- : Voltage Select

1.248V

▼

Device MacroCell Allocated

MCACMP

▼

🔒

Figure 2-5. TPLD1202 Module Controller InterConnect Studio Settings

Interfacing with a host controller via I²C is another option. Many TPLDs have the ability to act as an I²C peripheral with a user-defined address. TPLD2001 can fit up to three OSFP host controllers in a single device, freeing up a lot of space and GPIO pins in the system. TPLD's I²C address is defined by the user but cannot be changed after the TPLD is permanently configured. If the designer is ordering pre-configured devices from TI, a single pre-configured orderable part number can only have one I²C address. Designs requiring more than three OSFP host controllers can use an I²C multiplexer or, more efficiently, TPLD's GPIO-addressable I²C.

Although TPLD can be ordered pre-configured with no additional charge, the devices can also be configured by the user. All TPLDs that have I²C interfaces also allow the user to program the TPLDs on their own factory line by ordering unconfigured blank devices from TI. In this case, every TPLD can easily be configured with different addresses with only one orderable part number. More information about ordering pre-configured TPLD can be found in the Application Brief [TPLD Ordering Process](#) and information about in-system programming TPLD can be found in the Application Note [Programming in Production with TPLD](#).

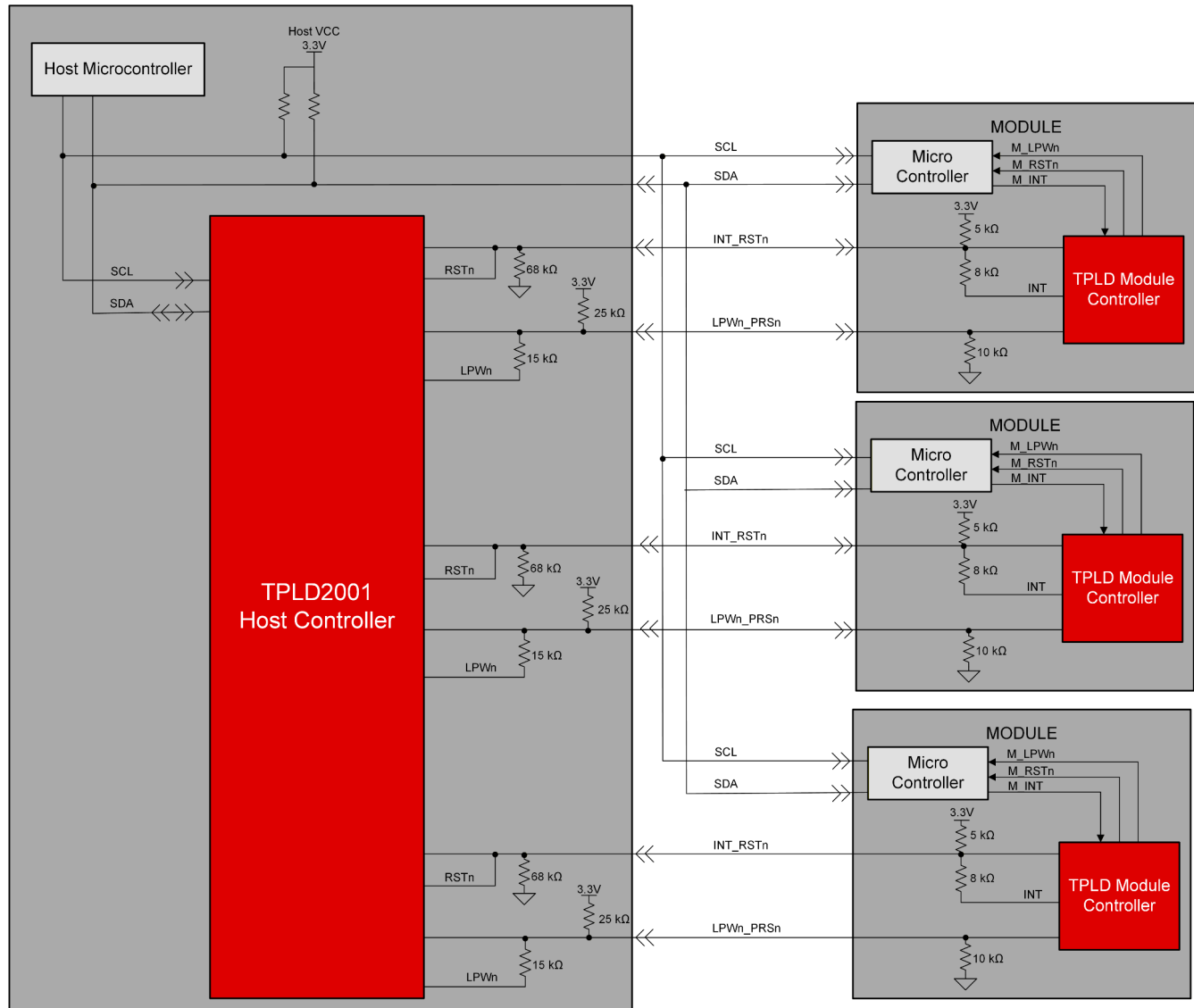


Figure 3-2. TPLD as a Three-Channel Host Controller

To provide each TPLD with a different I²C address, up to four bits of the I²C address are GPIO-selectable. The other three bits are defined by the user within the internal configuration. As a result, each TPLD orderable part number can have up to sixteen unique addresses. If more than sixteen unique addresses are required, adding additional TPLD configurations with a different address can allow up to a total of up to 126 unique addresses with eight orderable part numbers. Using GPIOs as address bits allows the designer to operate all the TPLD devices on the same I²C bus.

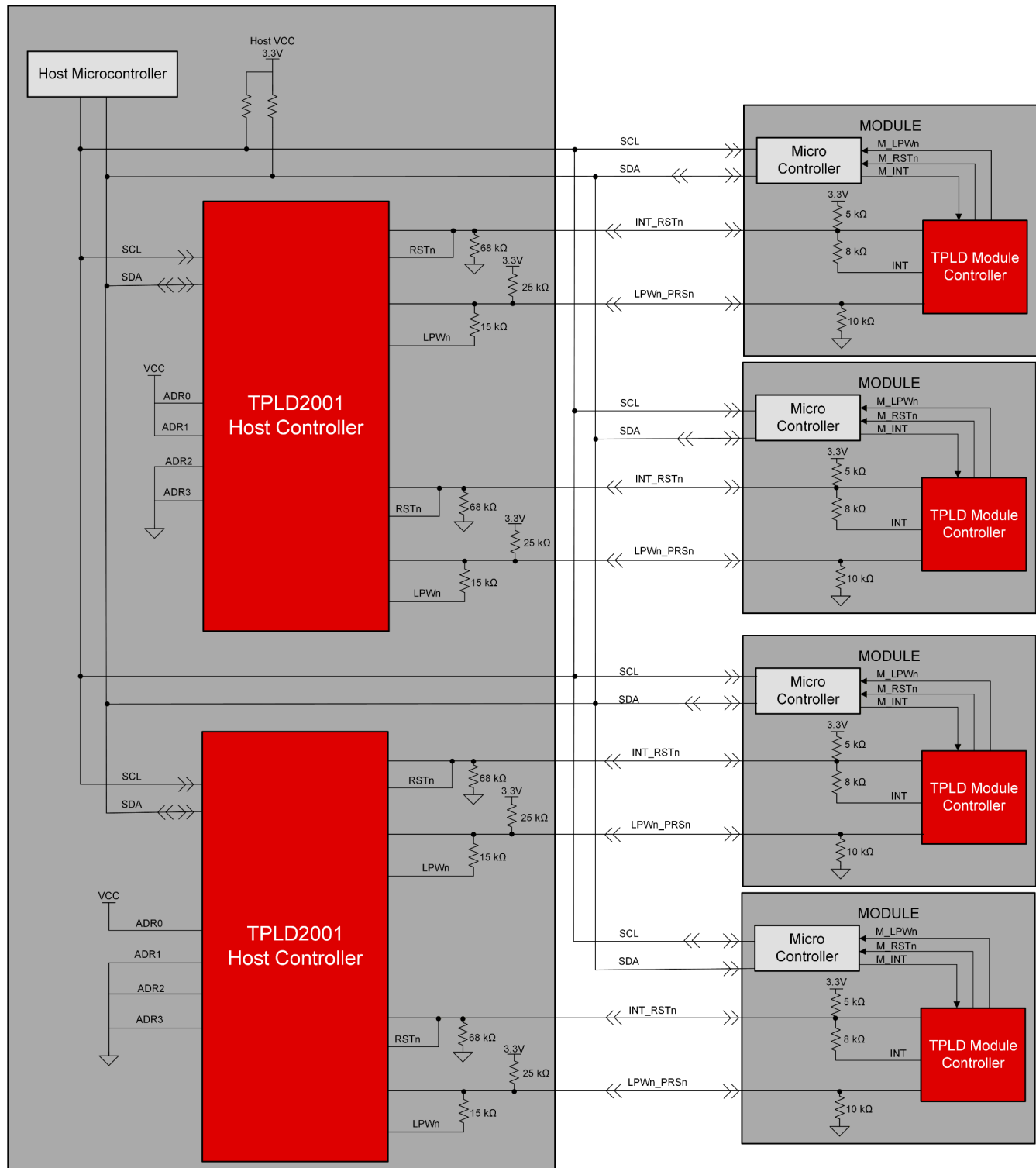


Figure 3-3. TPLD as a GPIO-addressable Dual-Channel Host Controller

4 Utilizing Optional TPLD Features for OSFP Systems

One of TPLD's most valuable features is its adaptability and customizability. This allows the integration of additional features that can be beneficial to the system even when it may not be directly relevant to OSFP low-speed signal requirements. For example, TPLD2001's analog multiplexer can be used to test other aspects of the system during the prototype or quality control phase, or TPLD's internal oscillator and logic gates can be used in power sequencing or signal delay.

5 Summary

This application note explores how TPLD can be configured to manage the low-speed signaling requirements of OSFP applications. TPLD can serve as both host and module controllers, providing the ability to integrate multiple host controllers into a single device to save space, the use of I²C integration to reduce signal line counts, and the utilization of GPIO-addressable I²C to eliminate the need for external multiplexers when communicating with host and module controllers.

TPLD allows designers to design-in and integrate logic and various functions into a single device, simplifying the BOM and reducing design size. For more information on TPLD, visit the TPLD product pages or ask our engineers a question on the TI E2E™ Support Forum.

6 References

- Texas Instruments, [TI Programmable Logic Devices](#), product page.
- Texas Instruments, [TPLD Ordering Process](#), application brief.
- Texas Instruments, [Programming in Production with TPLD](#), application note.

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