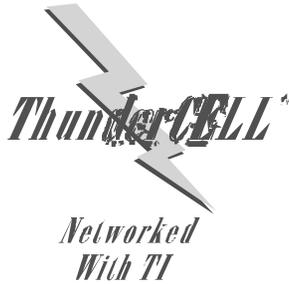


# TNETA1500 (SABRE™) Architecture

SONET/SDH/ATM  
BICMOS  
Receiver  
Transmitter

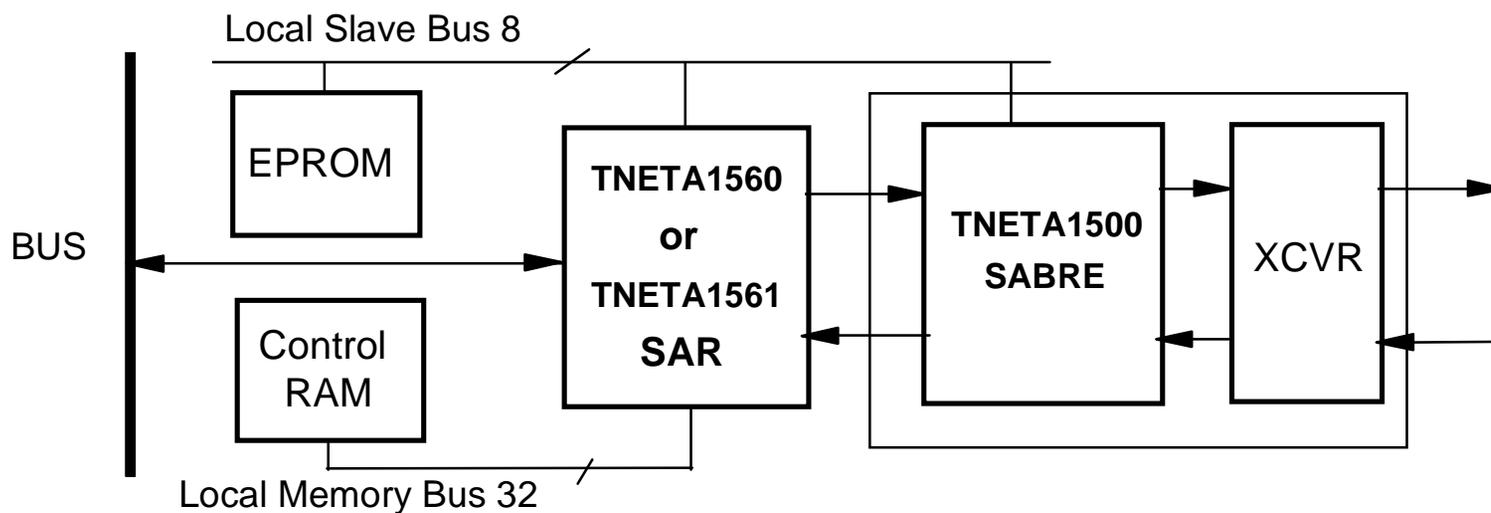
4ATM@timsg.csc.ti.com



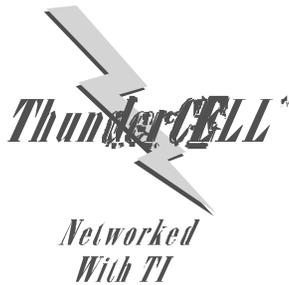
# AGENDA

- Main features
- Interfaces
- Architecture
- Transmit operation
- Receive operation
- Controller interface operation
- Registers
- SABRE™ and SAR interconnect

# SABRE Main Features

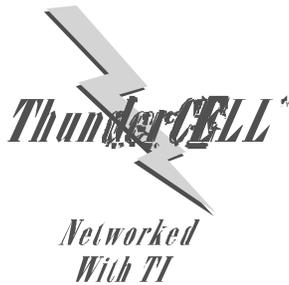


- Single chip receiver/transmitter for transporting 53-byte ATM cells via SONET STS-3c/STM-1 frames (155.52 Mbit/s)
- On-chip phased locked loops



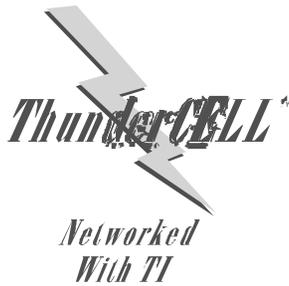
# Main Features

- Recovery of receive clock from incoming serial data stream
- Transmit clock generation from external 19.44-MHz source
- Inserts/extracts ATM cells into/from SONET (STS-3c)/SDH (STM-1) synchronous payload envelope (SPE)
- Idle (SONET mode)/unassigned (SDH mode) cells inserted when no cells are received from SAR
- Implements self-synchronizing scrambler polynomial
- Optional calculation of header error check (HEC) byte
- Meets ATM Forum user network interface (UNI) specification
- SAR (segmentation and reassembly) interface is full-duplex and compliant to UTOPIA specification
- Terminal loopback feature: cells received from the SAR device can be looped back

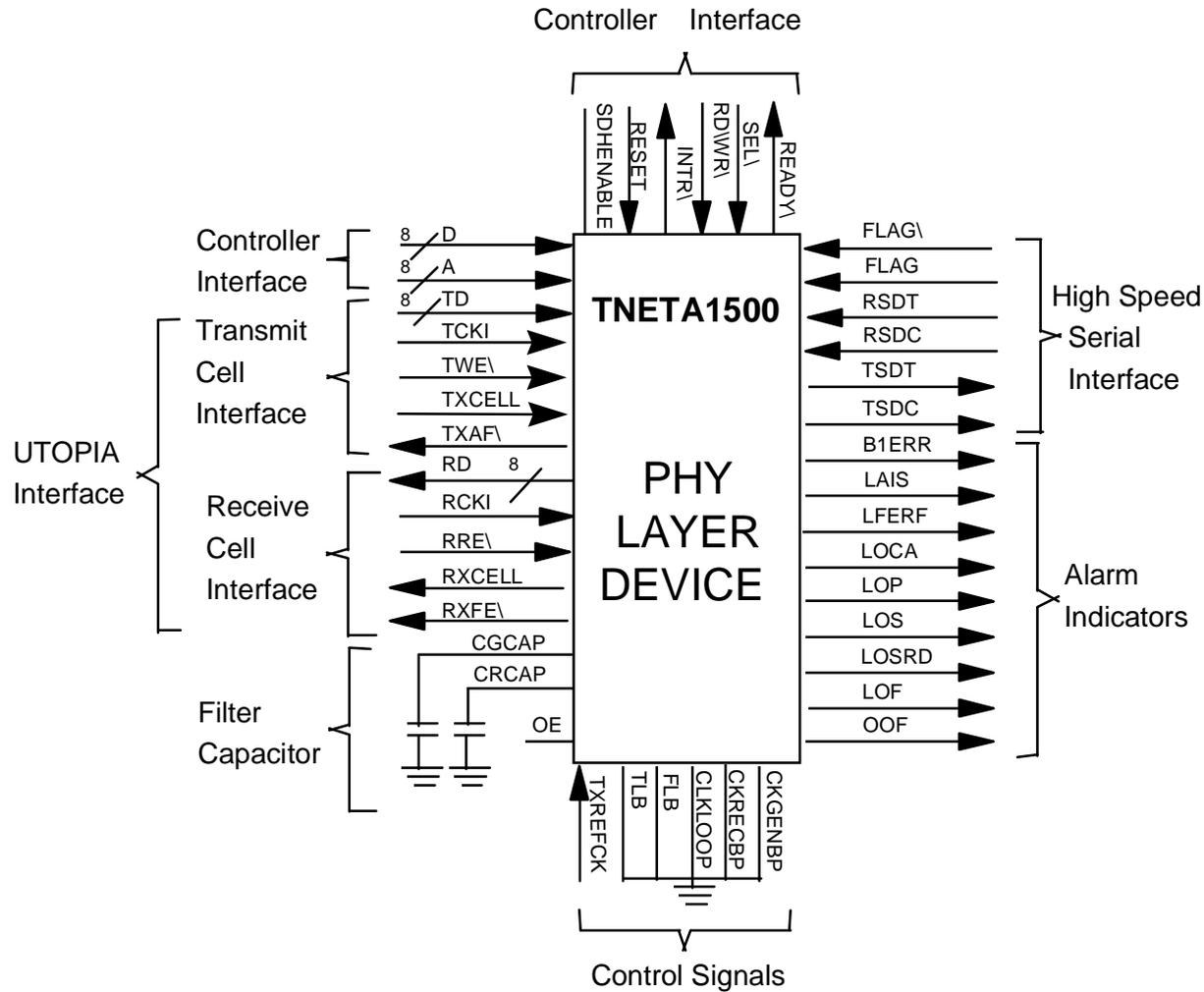


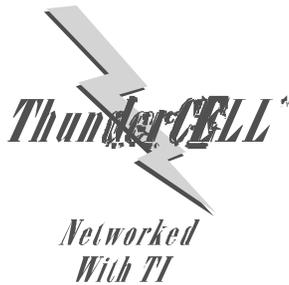
## Main Features (continued)

- Detects multiple bit errors in ATM header of incoming cells
- Corrects single bit errors in ATM header of incoming cells
- Counts the number of corrupted ATM cells (8-bit counter)
- B1, B2, and B3 coding violation and block error counters
- Path RDI soak counter
- Generates alarms for nine conditions, via pins
- Generates interrupts for eleven error conditions
- Packaged in a 144-pin plastic quad flatpack package (PQFP)



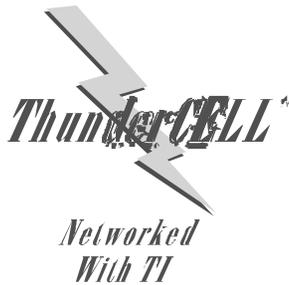
# SABRE Interfaces





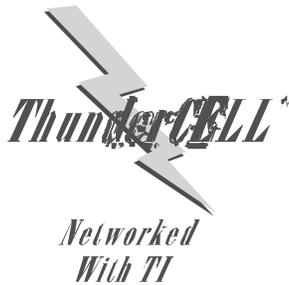
# High-Speed Serial Interface

- All signals on this interface are pseudo ECL
- Loss of optical carrier alarm (input): can be used to generate an interrupt, whenever the incoming optical signal is lost
- Receive serial clock (input): used when the clock recovery PLL is bypassed (CKRECBP input set high)
- Receive serial data (input)
- Transmit serial clock (output)
- Transmit serial data (output)
- Transmit high-speed clock (input); optional external high-speed clock source 155.52 MHz



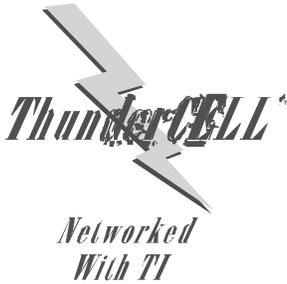
# Receive-Cell Interface

- Receive byte data (8-bit output)
- Receive clock (input)
- Receive start of cell (input): identifies the first byte of an outgoing ATM cell to SAR
- Receive FIFO empty (output): goes low when the receive FIFO is empty, indicates that RD is not valid
- Receive read enable (input)



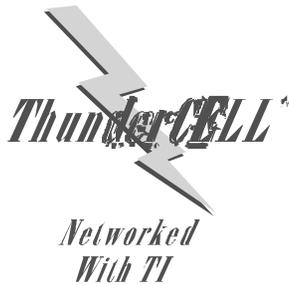
# Transmit-Cell Interface

- Transmit byte data (8-bit input)
- Transmit clock (input)
- Transmit start of cell (input): identifies the first byte of an incoming ATM cell
- Transmit FIFO almost full (output): goes low when there is room for only five more bytes
- Transmit write enable (input)



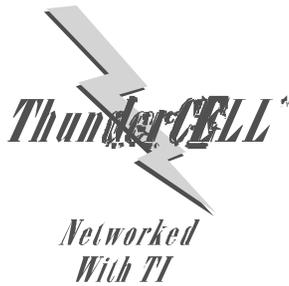
# Alarms Interface

- B1 error: B1 parity error on incoming frame
- Line alarm indication signal: from K2 byte
- Line far end receive failure: from K2 byte
- Loss of cell alignment: ATM cell alignment lost
- Loss of incoming pointer: invalid H1, H2 pointer bytes
- Loss of signal: no signal transitions
- Loss of frame: SONET/SDH frame loss (two frames)
- Out of frame: SONET/SDH frame loss (four frames)
- Loss of receive data: receive FIFO overflow

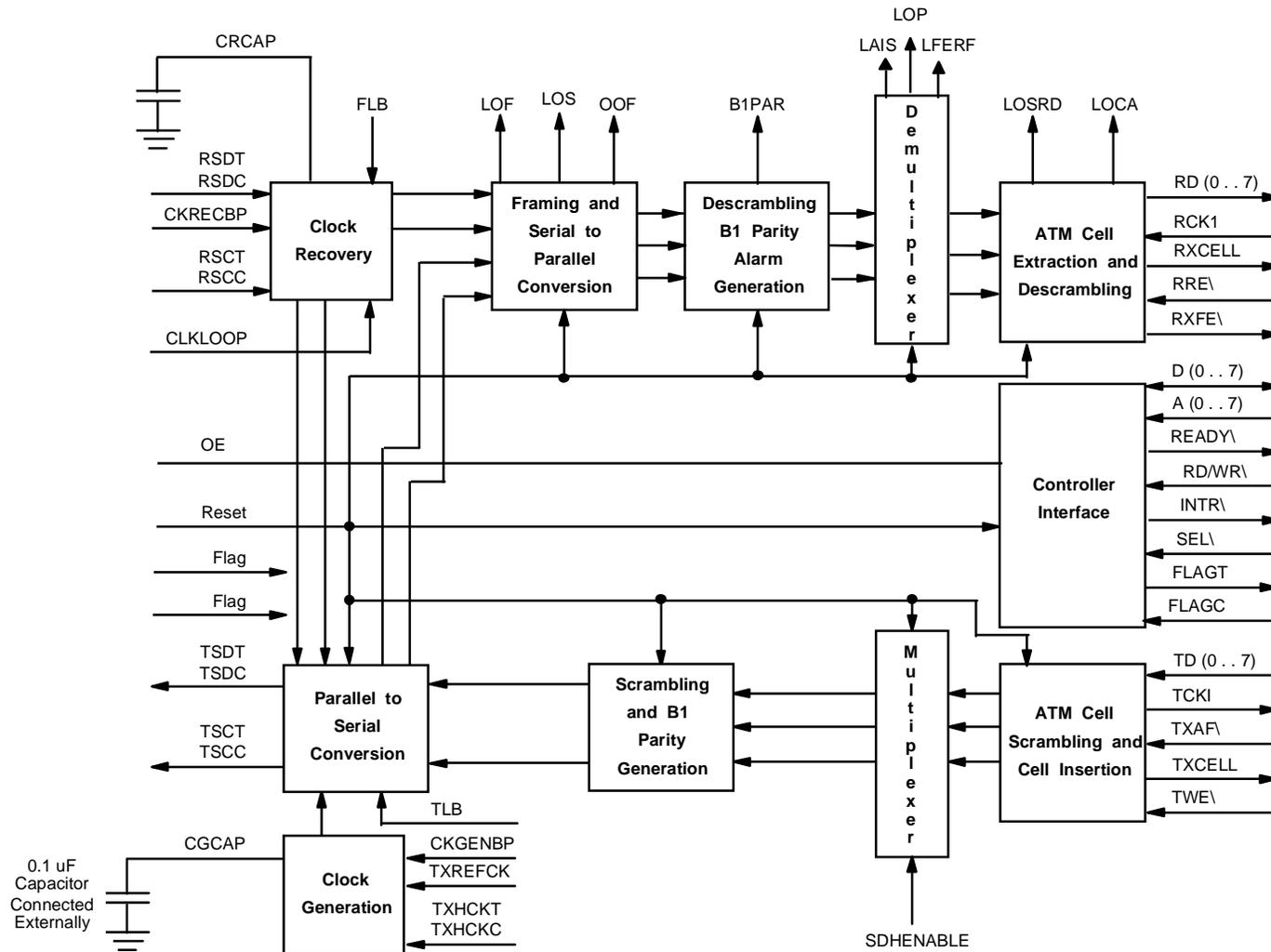


# Controller Interface

- Address lines (8-bit input)
- Data lines (8-bit input/output)
- Interrupt (output)
- Read/write (input)
- Ready (output)
- Device select (input)
- SDH enable (SONET mode if left open or tied to ground)

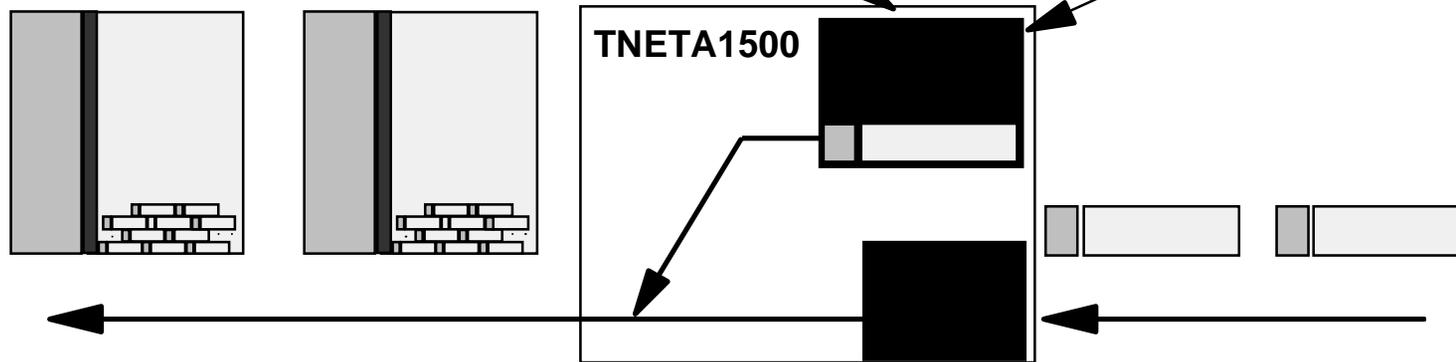
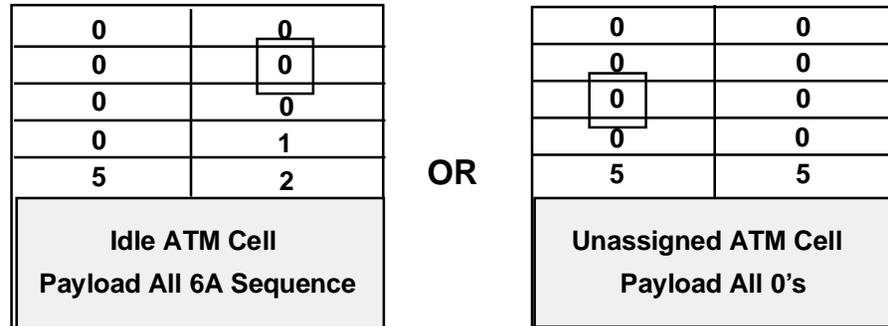


# TNETA1500 Architecture



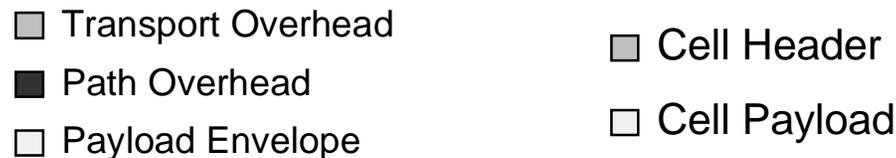
# Transmit Operation

- If a cell is incomplete in the FIFO, idle/unassigned cells are placed into the SONET/SDH payload.

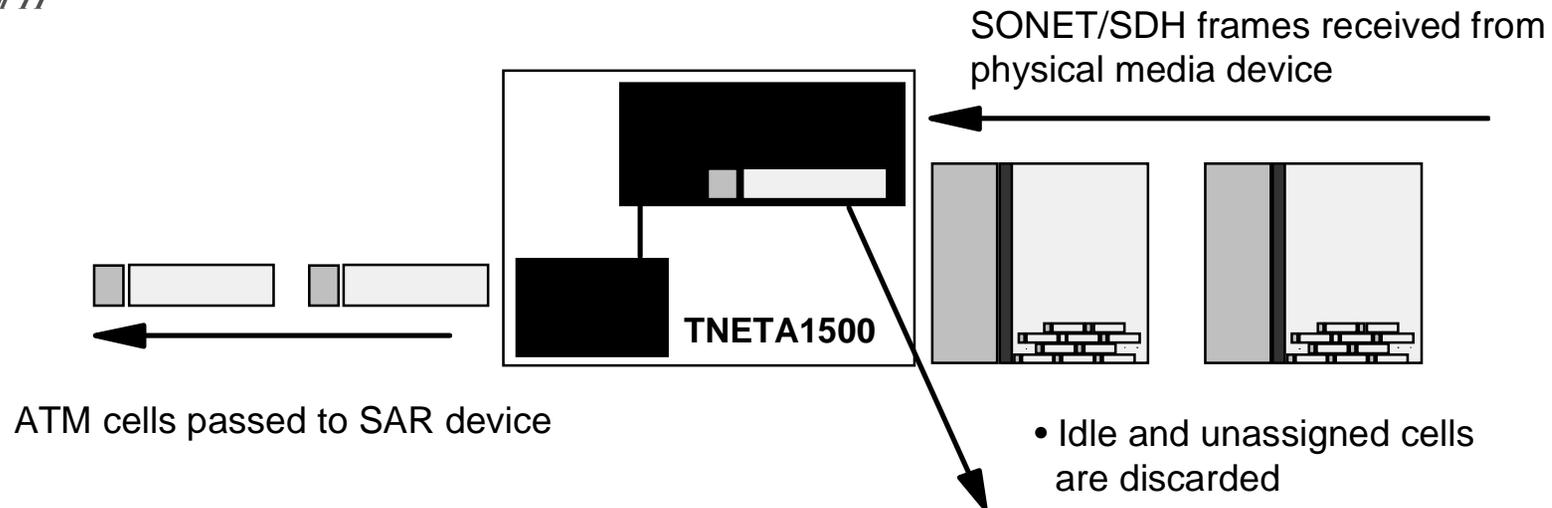


- SONET/SDH frames transmitted to physical media device

- ATM cells received from SAR device



# Receive Operation



- After descrambling, the idle and unassigned cells are dropped, and the ATM cells are passed to the output FIFO.

0	0
0	0
0	0
0	1
5	2

Idle ATM Cell  
 Payload All 6A Sequence

OR

0	0
0	0
0	0
0	0
5	5

Unassigned ATM Cell  
 Payload All 0's

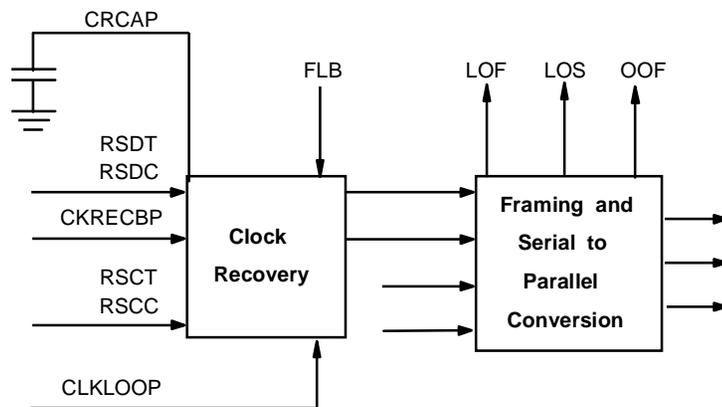
- Cell Header
- Cell Payload

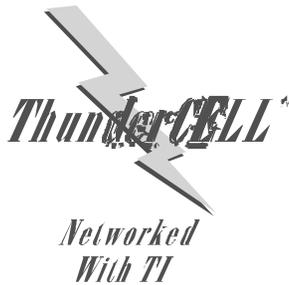
- Transport Overhead
- Path Overhead
- Payload Envelope



# SONET/SDH Frame Processing

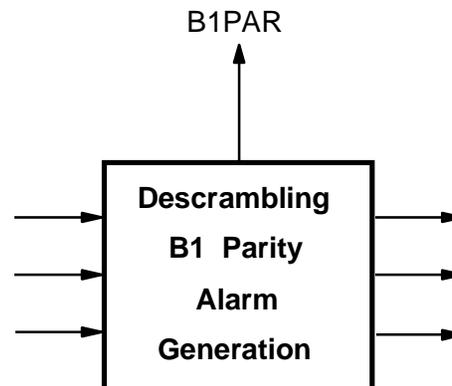
- Analog PLL locks onto incoming serial data to produce an accurate clock within five milliseconds
- Facility loopback feature loops receive data directly to transmit serial data output
- Loss of signal (LOS) output provided
- Loss of frame indicates framing circuit is unable to find two consecutive frames
- Out of frame goes active when four consecutive unacceptable (errored) frames are received
- Framing circuit searches for SONET/SDH framing pattern.
- For STS-3c/STM-1: A1A1A1A2A2A2 = F6F6F6282828 (hex)





# SONET/SDH Frame Processing

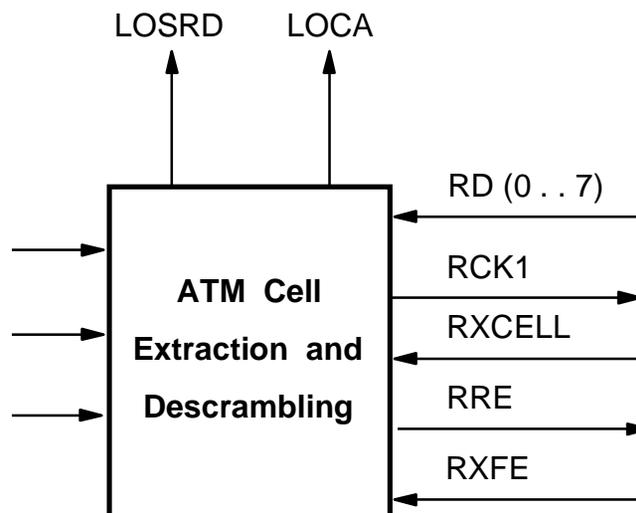
- Serial data converted to byte-wide data
- B1 parity calculated over scrambled SONET/SDH frame
- This is compared with the B1 byte in the next frame
- Failure indicated by signal and interrupt
- SONET/SDH frame is then unscrambled

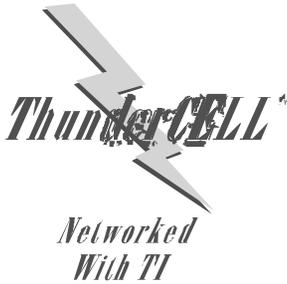




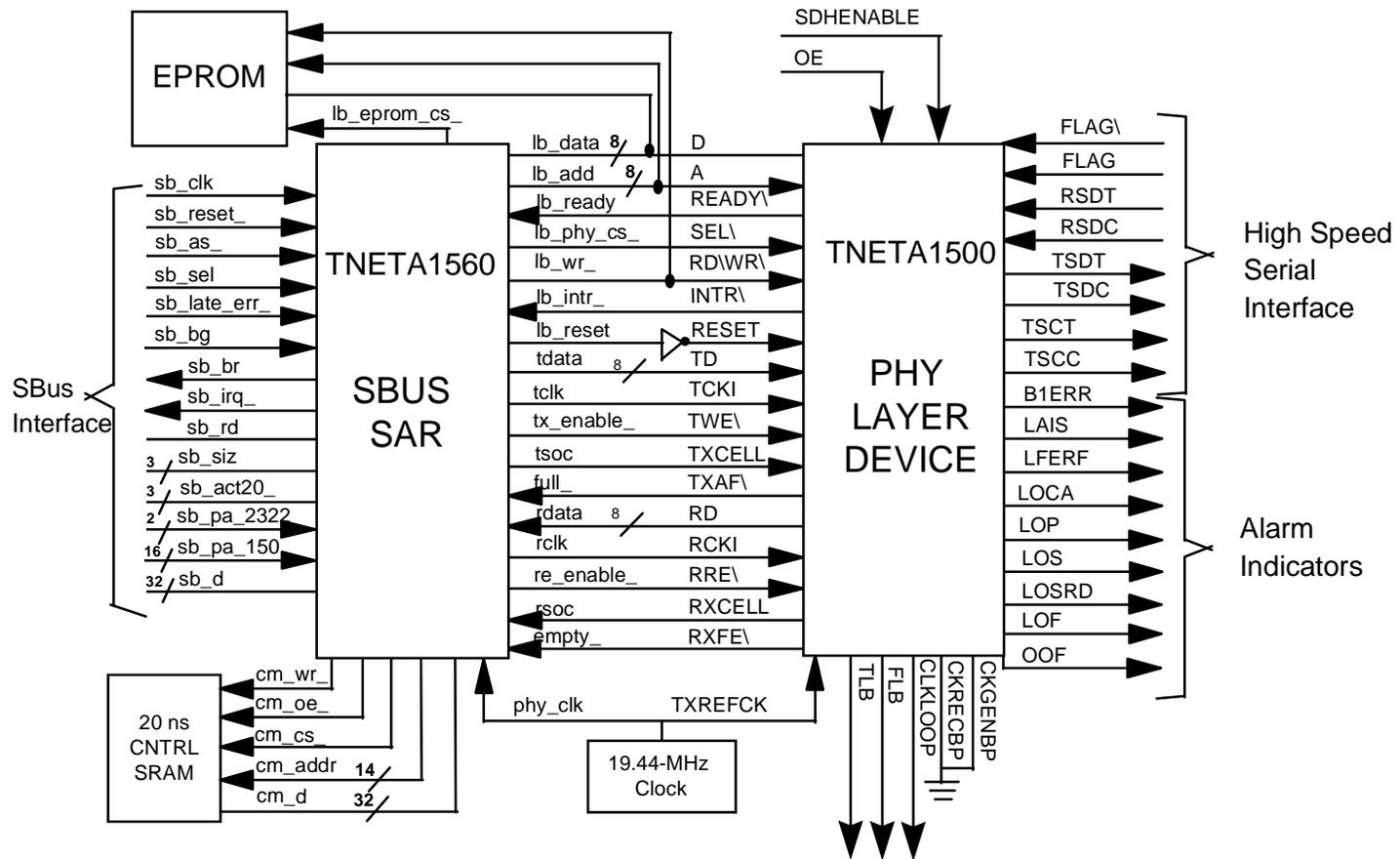
# ATM Cell Processing

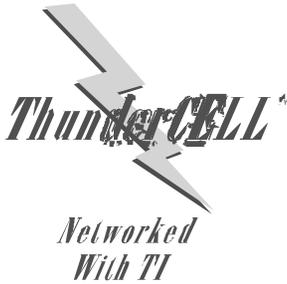
- Detects multiple bit errors and corrects single-bit errors in the 5-byte header of incoming ATM cells
- Cells with multiple-bit errors are dropped if so configured
- Cell payloads are descrambled and placed in output FIFO
- Loss-of-receive data signal is asserted when the output FIFO overflows



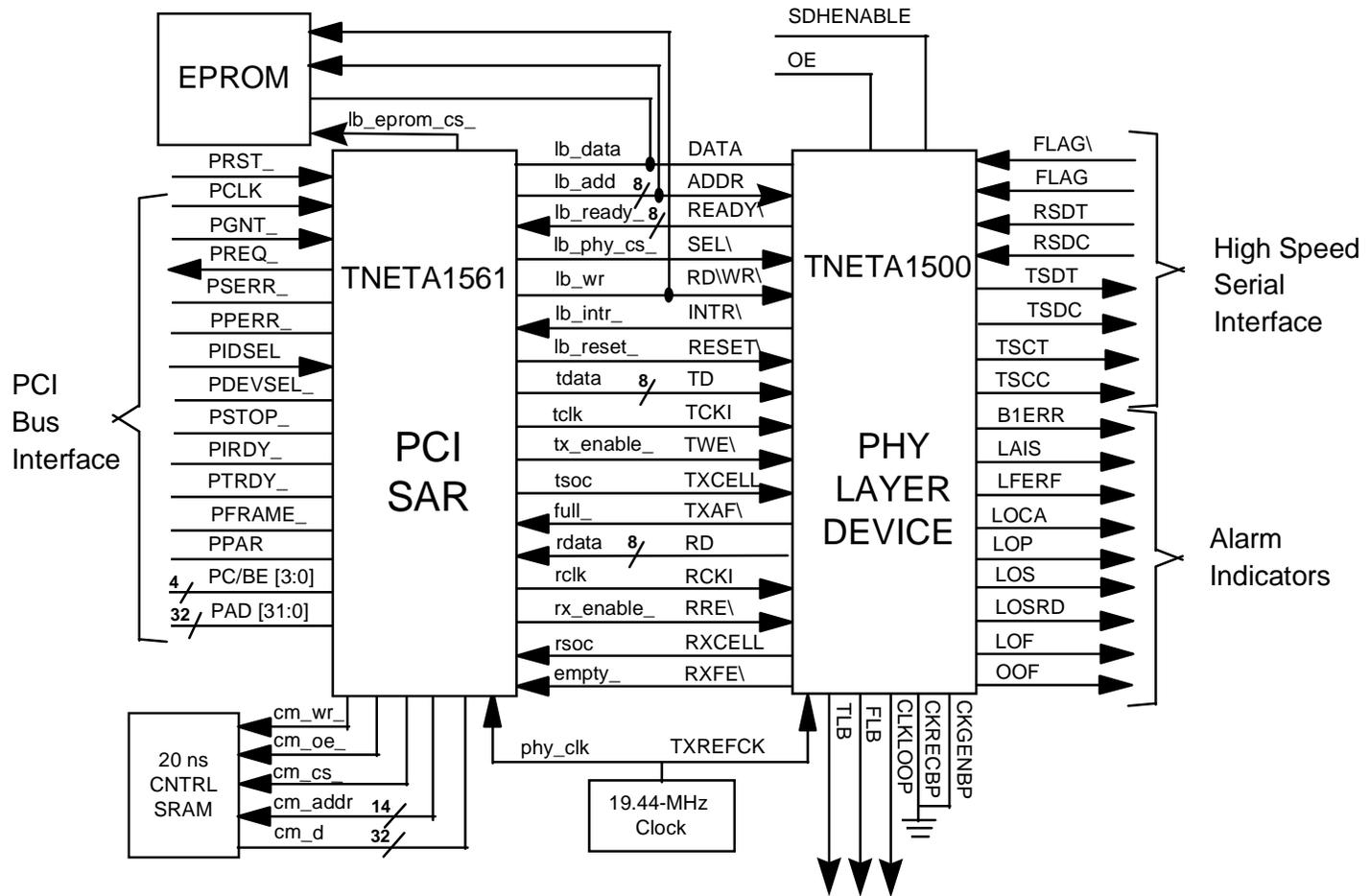


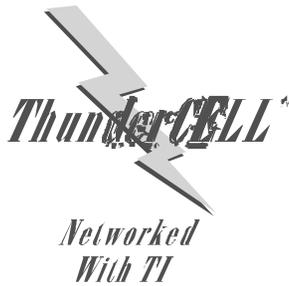
# SBus SAR, SABRE Interconnect



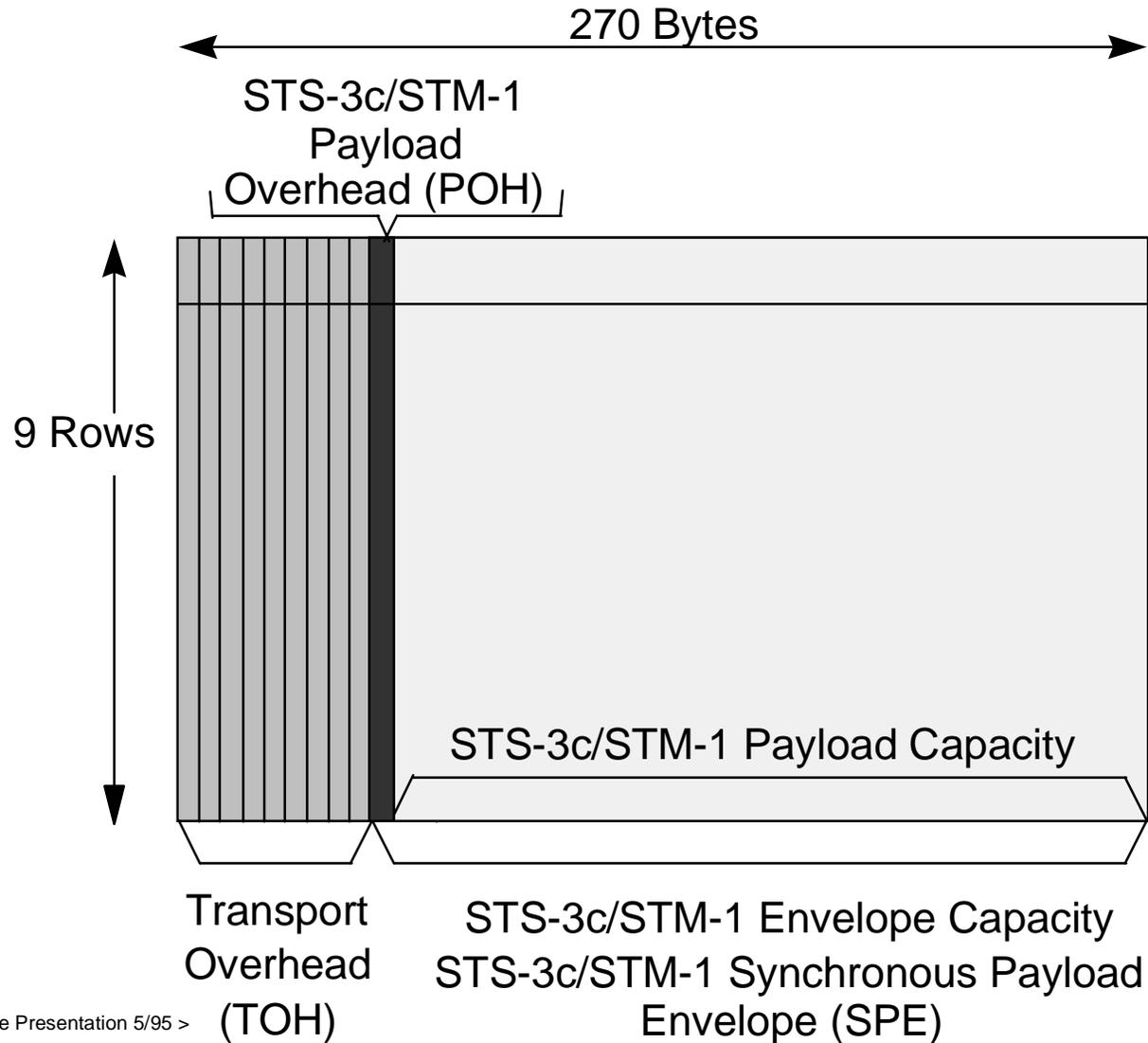


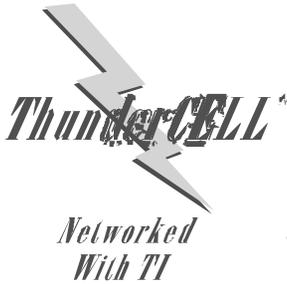
# PCI Bus ATM Adapter





# SONET/SDH Frame Structure





# SONET/SDH Frame Structure

