Functional Safety Information

TMP112-Q1 and TMP112D-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TMP112-Q1 and TMP112D-Q1 (SOT563-6 and X2SON-5 packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

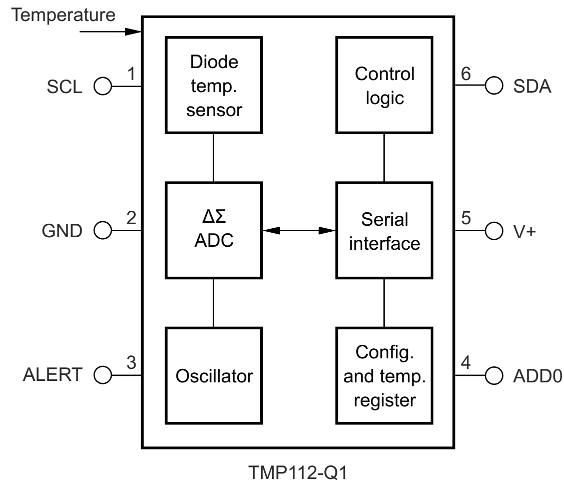

Figure 1-1. Functional Block Diagram

TMP112-Q1 and TMP112D-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT563-6 Package

This section provides functional safety failure in time (FIT) rates for TMP112-Q1 and TMP112D-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1.0mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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2.2 X2SON-5 Package

This section provides functional safety failure in time (FIT) rates for the X2SON-5 package of the TMP112D-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	3
Die FIT rate	2
Package FIT rate	1

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1.0mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TMP112-Q1 and TMP112D-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Temperature results are out of specification	50
Serial communication error	25
Register bank data bit error	20
Alert false trip, fails to trip	5

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TMP112-Q1 and TMP112D-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is the only target on the I2C bus.
- There is an external pullup resistor on the SCL and SDA pins.

4.1 SOT563-6 Package

Figure 4-1 shows the TMP112-Q1 and TMP112D-Q1 pin diagram for the SOT563-6 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMP112-Q1 and TMP112D-Q1 datasheet.

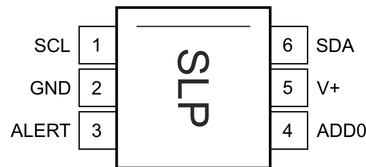

Figure 4-1. Pin Diagram (SOT563-6) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SCL	1	The SCL pin is stuck low. I2C communication is not possible.	B
GND	2	There is no effect on the device. The device operates as normal.	D
ALERT	3	The ALERT pin is stuck low. The device is not functional, a false thermal limit triggers.	B
ADD0	4	The I2C address selection is limited. I2C communication is potentially corrupted.	B
V+	5	The device is not powered. The device is not functional. The device is potentially damaged.	A
SDA	6	The SDA pin is stuck low. I2C communication is not possible.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SCL	1	The state of the SCL pin is undetermined. I2C communication is not possible.	B
GND	2	The functionality of the device is undetermined. The device is potentially not powered or connects to GND internally through the ESD diode of the alternate pin and powers on.	B
ALERT	3	The ALERT pin is stuck low. The device is not functional, a false thermal limit potentially triggers.	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ADD0	4	The I2C address selection is limited. I2C communication is potentially corrupted.	B
V+	5	The device is not powered if all other pins are held low; the device is not functional. The device potentially powers up through ESD diodes to the V+ pin if voltages above the power-on reset threshold for the device are present on any of the pins of the device.	B
SDA	6	The state of the SDA pin is undetermined. I2C communication is not possible.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
SCL	1	GND	The SCL pin is stuck low. I2C communication is not possible.	B
GND	2	ALERT	The ALERT pin is stuck low. The device is not functional, a false thermal limit potentially triggers.	B
ALERT	3	ADD0	If the ADD0 pin is connected to GND, the ALERT pin is stuck low and not functional and a thermal limit triggers. If the ADD0 pin is connected to the SCL or SDA pin, the ALERT pin toggles between high and low as communication occurs, potentially triggering thermal limits. If the ADD0 pin is connected to the V+ pin, the ALERT pin is stuck high and a thermal limit does not trigger.	B
ADD0	4	V+	The I2C address selection is limited. I2C communication is potentially corrupted.	B
V+	5	SDA	The SDA pin is stuck high. I2C communication is not possible.	B
SDA	6	SCL	I2C communication cannot occur, data corruption occurs.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SCL	1	The SCL pin is stuck high. I2C communication is not possible.	B
GND	2	The functionality of the device is undetermined. The device is potentially damaged.	A
ALERT	3	The ALERT pin is stuck high. The device is not functional. Thermal limit does not trigger.	B
ADD0	4	The I2C address selection is limited. I2C communication is potentially corrupted.	B
V+	5	There is no effect on the device. The device operates as normal.	D
SDA	6	The SDA pin is stuck high. I2C communication is not possible.	B

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4.2 X2SON-5 Package

Figure 4-2 shows the TMP112D-Q1 pin diagram for the X2SON-5 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMP112D-Q1 datasheet.

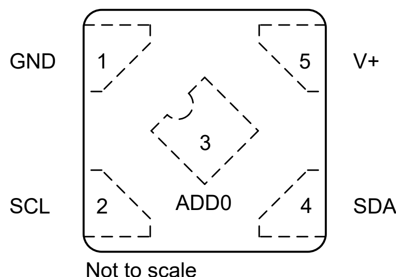

Figure 4-2. Pin Diagram (X2SON-5 Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	There is no effect on the device. The device operates as normal.	D
SCL	2	The SCL pin is stuck low. I2C communication is not possible.	B
ADD0	3	The I2C address selection is limited. I2C communication is potentially corrupted.	B
SDA	4	The SDA pin is stuck low. I2C communication is not possible.	B
V+	5	The device is not powered. The device is not functional. The device is potentially damaged.	A

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	The functionality of the device is undetermined. The device is potentially not powered or connects to GND internally through the ESD diode of the alternate pin and powers on.	B
SCL	2	State of SCL undetermined, no I2C communication possible.	B
ADD0	3	The address selection function is limited. Communication is potentially corrupted.	B
SDA	4	The state of the SDA pin is undetermined. I2C communication is not possible.	B
V+	5	The device is not powered if all other pins are held low; the device is not functional. The device potentially powers up through ESD diodes to the V+ pin if voltages above the power-on reset threshold for the device are present on any of the pins of the device.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	SCL	The SCL pin is stuck low. I2C communication is not possible.	B
SCL	2	SDA	I2C communication cannot occur, data corruption occurs.	B
SDA	4	V+	The SDA pin is stuck high. I2C communication is not possible.	B
V+	5	GND	The functionality of the device is undetermined. The device is potentially damaged.	A
ADD0	3	GND	The I2C address selection is limited. I2C communication is potentially corrupted.	B
ADD0	3	SCL	The I2C address selection is limited. I2C communication is potentially corrupted.	B
ADD0	3	SDA	The I2C address selection is limited. I2C communication is potentially corrupted.	B
ADD0	3	V+	The I2C address selection is limited. I2C communication is potentially corrupted.	B

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Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	The functionality of the device is undetermined. The device is potentially damaged.	A
SCL	2	The SCL pin is stuck high. I2C communication is not possible.	B
ADD0	3	The address selection function is limited. Communication is potentially corrupted.	B
SDA	4	The SDA pin is stuck high. I2C communication is not possible.	B
V+	5	There is no effect on the device. The device operates as normal.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 13, 2022 to November 7, 2025 (from Revision * (June 2022) to Revision A (November 2025)) **Page**

- Added the TMP112D-Q1 part number throughout the document....2
- Added the X2SON-5 package information....2
- Added *SOT563-6 Package* section....3
- Added *X2SON-5 Package* section....4
- Updated the *Die Failure Modes and Distribution* table....5
- Updated links in the *Pin Failure Mode Analysis (Pin FMA)* section....6
- Added independent section for the tables in the *Pin Failure Mode Analysis (Pin FMA)* section....6
- Added the *SOT563-6 Package* section....6
- Added *X2SON-5 Package* section....8

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