Functional Safety Information

LMR436x0 and LMR436x0-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Marshall Beck, SR-WVB

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Trademarks

1 Overview

This document contains information for LMR436x0 and LMR436x0-Q1 (VQFN-HR package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

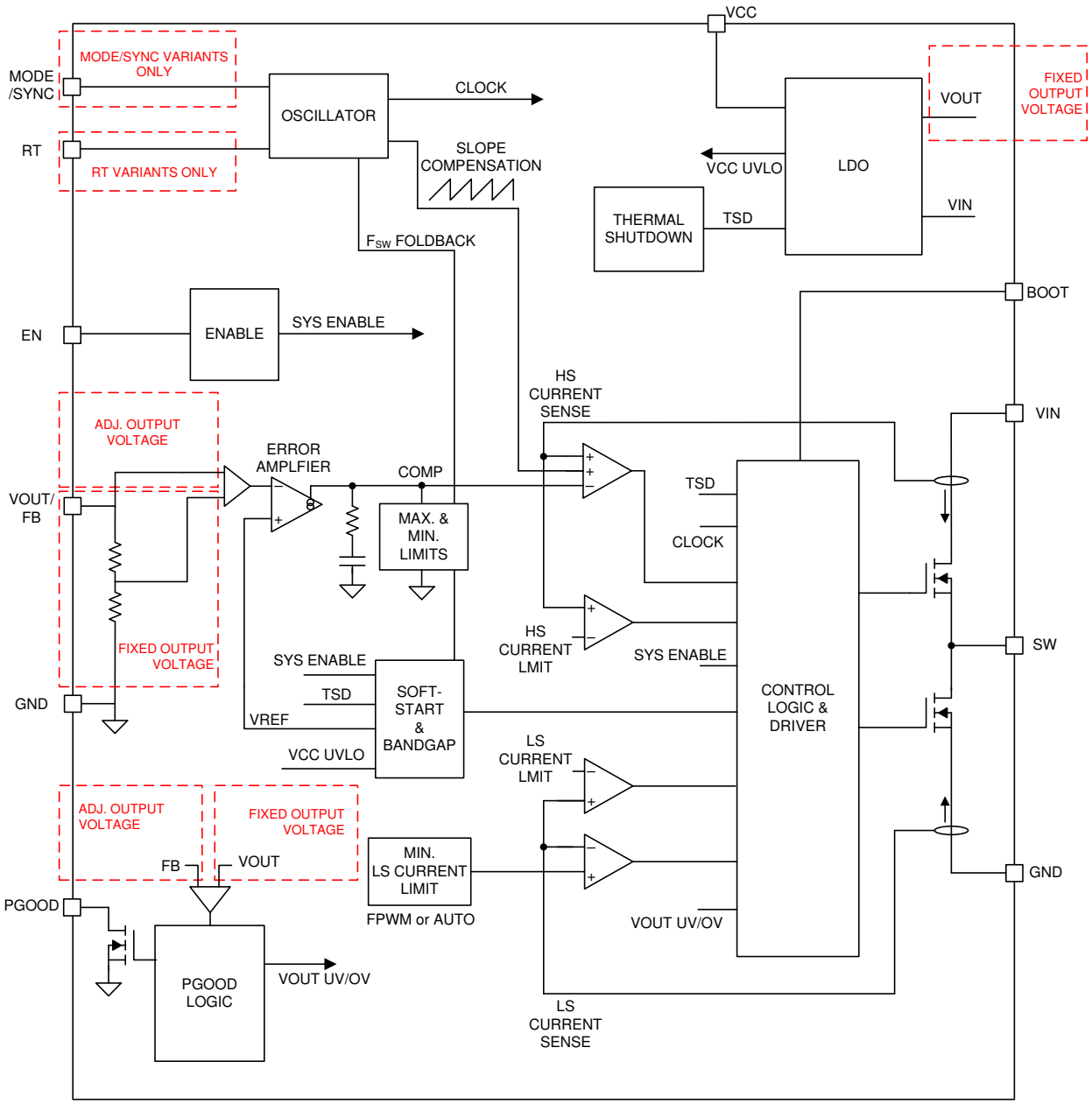

Figure 1-1. Functional Block Diagram

LMR436x0 and LMR436x0-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LMR436x0 and LMR436x0-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	11
Die FIT rate	4
Package FIT rate	7

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 230mW
- Climate type: World-wide from table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed ≤50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR436x0 and LMR436x0-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	60
Output not in specification – voltage or timing	30
PG false trip or fails to trip	5
Short circuit any two pins	5

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMR436x0 and LMR436x0-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LMR436x0 and LMR436x0-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LMR436x0 and LMR436x0-Q1 data sheet.

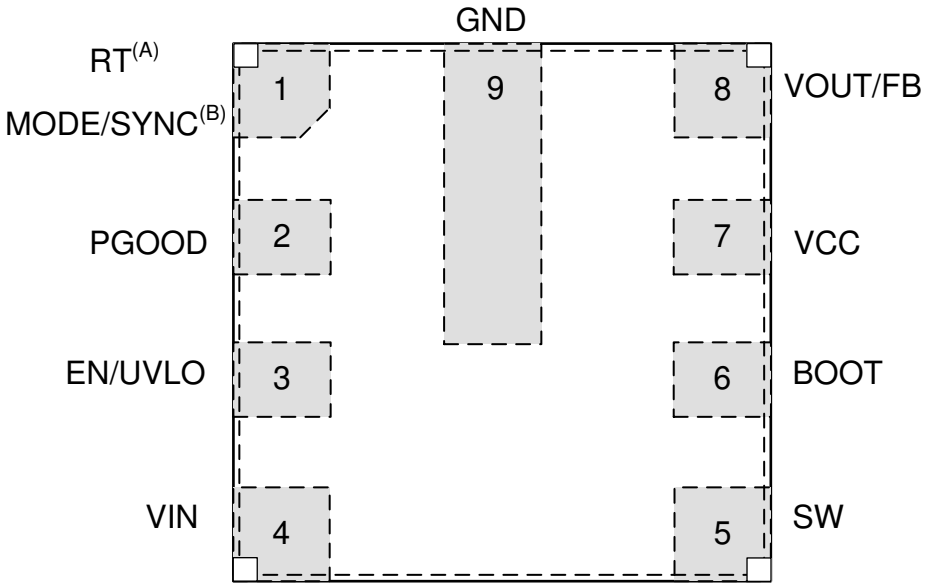

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the LMR436x0 and LMR436x0-Q1 data sheets is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RT or MODE/ SYNC	1	The switching frequency is 2.2MHz.	D
PGOOD	2	When not in use, this pin can be left grounded (PGOOD is not a valid signal and V_{OUT} is normal).	D
EN/UVLO	3	V_{OUT} = 0V. (Enable is off and functionality is halted.)	D
VIN	4	V_{OUT} = 0V.	B
SW	5	Damage to the HS FET.	A
BOOT	6	V_{OUT} = 0V. HS does not turn on.	B
VCC	7	V_{OUT} = 0V.	B
VOUT/BIAS or FB	8	When in adjustable output mode, V_{OUT} approaches VIN. When in fixed output mode, V_{OUT} = 0V.	B
GND	9	V_{OUT} is normal.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RT or MODE/ SYNC	1	If an RT part, frequency is not defined. If a MODE/SYNC part, then the part can go back and forth between FPWM/PFM. The part is up and functional.	C
PGOOD	2	When not in use, this pin can be left open (PGOOD is not a valid signal and V_{OUT} is normal).	D
EN/UVLO	3	Pin cannot be left floating.	B
VIN	4	V_{OUT} = 0V.	B
SW	5	V_{OUT} = 0V.	B
BOOT	6	V_{OUT} = 0V. HS does not turn on.	B
VCC	7	VCC output is unstable and can increase above 5.5V.	A
VOUT/BIAS or FB	8	V_{OUT} approaches VIN.	C
GND	9	V_{OUT} can be abnormal, as reference voltage is not fixed.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
RT or MODE/ SYNC	1	PGOOD	If PGOOD is high, and < 5.5V, F_{SW} = 1MHz. If PGOOD is low, F_{SW} = 2.2MHz. With PGOOD absolute maximum rating being 20V, RT ESD damages if PG goes to 20V.	A
PGOOD	2	EN/UVLO	If EN/UVLO > 20V, damages devices connected to the PGOOD pin.	A
EN/UVLO	3	VIN	V_{OUT} is normal (Enable is on and all other blocks work).	D
VIN	4	SW	Damage to LS FET.	A
SW	5	BOOT	V_{OUT} = 0V. HS does not turn on and there is no C_{BOOT}.	B
BOOT	6	VCC	Damage occurs and there is a break to the VCC pin.	A
VCC	7	VOUT/BIAS or FB	Does not work, but no damage occurs.	B
VOUT/BIAS or FB	8	GND	When in adjustable output mode, V_{OUT} approaches VIN. When in fixed output mode, V_{OUT} = 0V.	B
GND	9	RT or MODE/ SYNC	V_{OUT} is normal if the RT/MODE/SYNC pin is low, otherwise not functional.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RT or MODE/ SYNC	1	If V_{IN} > 5.5V, damage occurs. If V_{IN} < 5.5V, switching frequency is 1MHz.	A
PGOOD	2	If V_{IN} > 20V, damages PGOOD.	A
EN/UVLO	3	V_{OUT} is normal (Enable is on and all other blocks work).	D
VIN	4	V_{OUT} is normal.	D
SW	5	Damage to LS FET.	A
BOOT	6	Damage occurs and BOOT ESD clamp is damaged.	A
VCC	7	If V_{IN} > 5.5V, damage occurs.	A
VOUT/BIAS or FB	8	If V_{IN} > 16V, damage occurs.	A
GND	9	V_{OUT} = 0V.	B

5 Revision History

Changes from March 18, 2022 to August 27, 2025 (from Revision * (March 2022) to Revision A (August 2025)) **Page**

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265