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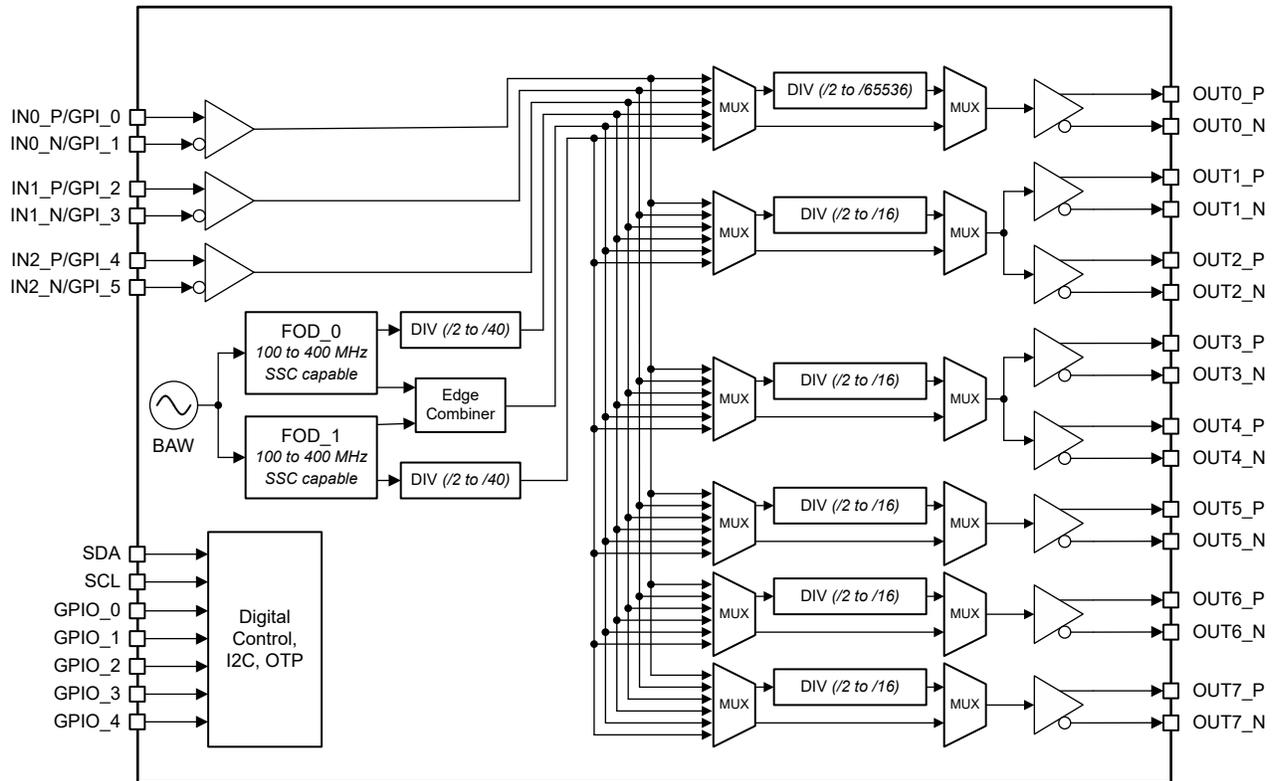
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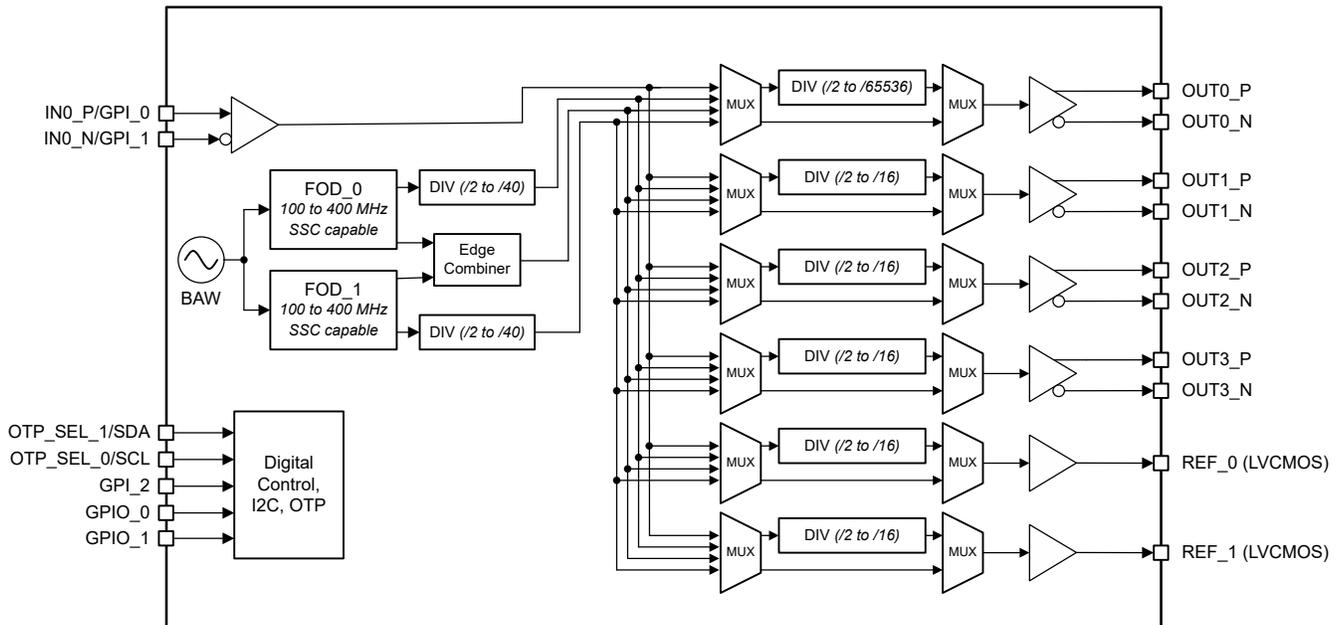
# 1 Overview

This document contains information for the LMK3H2108-Q1 and LMK3H2104-Q1 to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and failure mode distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)



**Figure 1-1. LMK3H2108-Q1 Functional Block Diagram**



**Figure 1-2. LMK3H2104-Q1 Functional Block Diagram**

The LMK3H2108-Q1 and LMK3H2104-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

### 2.1 LMK3H2108-Q1

This section provides functional safety failure in time (FIT) rates for the LMK3H2108-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total component FIT rate	27
Die FIT rate	3
Package FIT rate	24

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 580mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub> (°C)
5	CMOS, BICMOS ASICs analog and mixed ≤ 50V supply	70	70

The reference FIT rate and reference virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 2.2 LMK3H2104-Q1

This section provides functional safety failure in time (FIT) rates for the LMK3H2104-Q1 based on two different industry-wide used reliability standards:

- [Table 2-3](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-4](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total component FIT rate	14
Die FIT rate	3
Package FIT rate	11

The failure rate and mission profile information in [Table 2-3](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS, BICMOS ASICs analog and mixed ≤ 50V supply	70	70

The reference FIT rate and reference virtual T<sub>J</sub> (junction temperature) in [Table 2-4](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LMK3H2108-Q1 and LMK3H2104-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution (%)
No output clock	15
Inaccurate output frequency	20
Performance degradation of output clocks	30
Unable to configure or incorrect configurations	15
Clock input does not work properly	10
GPI or GPIO do not work properly	10

## 4 Pin Failure Mode Analysis (Pin FMA)

### 4.1 LMK3H2108-Q1

This section provides a failure mode analysis (FMA) for the pins of the LMK3H2108-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

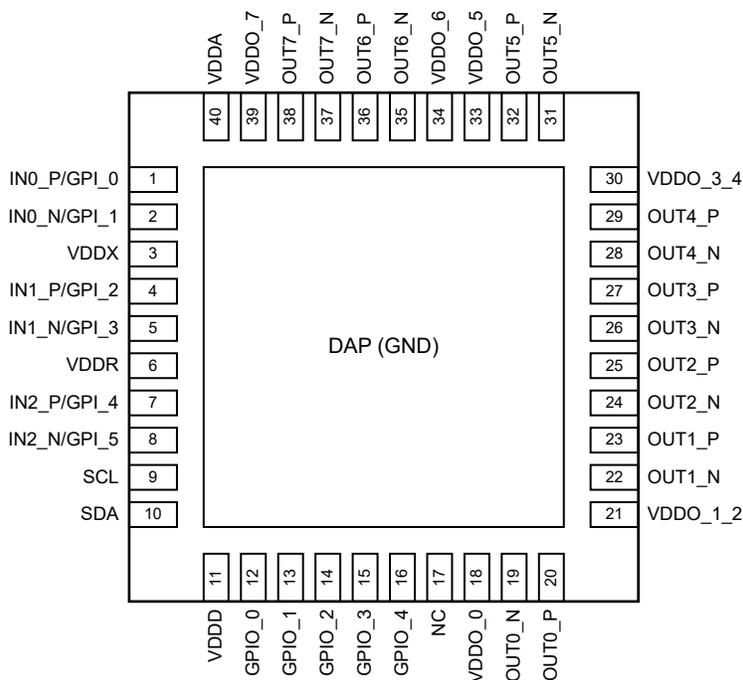
- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to VDD (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the LMK3H2108-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LMK3H2108-Q1 datasheet.



**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- VDDA = VDDD = VDDR = VDDX = VDDO\_x = 3.3V
- GPI\_0 = OE0#, GPI\_1 = OE1#, GPI\_2 = OE2#, GPI\_3 = OE3#, GPI\_4 = OE4#, GPI\_5 = OE5#, GPIO\_2 = OE6#, GPIO\_3 = OE7#. OE# means output enable for OUTx, active low. All OE pins have an internal pulldown resistor enabled.
- GPIO\_0 and GPIO\_1 are configured as dynamic OTP page select. Internal pulldown resistors are enabled.
- GPIO\_4 is configured as PWRGD/PWRDN#. Internal pulldown resistor is enabled.
- OUT0 through OUT7 are configured as 100MHz LP-HCSL.

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN0_P/GPI_0	1	OUT0 is enabled but cannot be controlled by the GPI_0 pin.	B
IN0_N/GPI_1	2	OUT1 is enabled but cannot be controlled by the GPI_1 pin.	B
VDDX	3	A power-ground short can damage the device.	A
IN1_P/GPI_2	4	OUT2 is enabled but cannot be controlled by the GPI_2 pin.	B
IN1_N/GPI_3	5	OUT3 is enabled but cannot be controlled by the GPI_3 pin.	B
VDDR	6	A power-ground short can damage the device.	A
IN2_P/GPI_4	7	OUT4 is enabled but cannot be controlled by the GPI_4 pin.	B
IN2_N/GPI_5	8	OUT5 is enabled but cannot be controlled by the GPI_5 pin.	B
SCL	9	There is no I2C communication.	B
SDA	10	There is no I2C communication.	B
VDDD	11	A power-ground short can damage the device.	A
GPIO_0	12	The OTP page selection does not work properly.	B
GPIO_1	13	The OTP page selection does not work properly.	B
GPIO_2	14	OUT6 is enabled but cannot be controlled by the GPIO_2 pin.	B
GPIO_3	15	OUT7 is enabled but cannot be controlled by the GPIO_3 pin.	B
GPIO_4	16	The device cannot be powered up.	B
NC	17	There is no impact to the device.	D
VDDO_0	18	A power-ground short can damage the device.	A
OUT0_N	19	There is a loss of clock output.	B
OUT0_P	20	There is a loss of clock output.	B
VDDO_1_2	21	A power-ground short can damage the device.	A
OUT1_N	22	There is a loss of clock output.	B
OUT1_P	23	There is a loss of clock output.	B
OUT2_N	24	There is a loss of clock output.	B
OUT2_P	25	There is a loss of clock output.	B
OUT3_N	26	There is a loss of clock output.	B
OUT3_P	27	There is a loss of clock output.	B
OUT4_N	28	There is a loss of clock output.	B
OUT4_P	29	There is a loss of clock output.	B
VDDO_3_4	30	A power-ground short can damage the device.	A
OUT5_N	31	There is a loss of clock output.	B
OUT5_P	32	There is a loss of clock output.	B
VDDO_5	33	A power-ground short can damage the device.	A
VDDO_6	34	A power-ground short can damage the device.	A
OUT6_N	35	There is a loss of clock output.	B
OUT6_P	36	There is a loss of clock output.	B
OUT7_N	37	There is a loss of clock output.	B
OUT7_P	38	There is a loss of clock output.	B
VDDO_7	39	A power-ground short can damage the device.	A
VDDA	40	A power-ground short can damage the device.	A
DAP	41	There is no impact to the device.	D

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN0_P/GPI_0	1	OUT0 is enabled but cannot be controlled by the GPI_0 pin.	B
IN0_N/GPI_1	2	OUT1 is enabled but cannot be controlled by the GPI_1 pin.	B
VDDX	3	Circuits that are powered by the VDDX pin are not powered up. See the LMK3H2108-Q1 datasheet for the circuits powered by the VDDX pin.	B
IN1_P/GPI_2	4	OUT2 is enabled but cannot be controlled by the GPI_2 pin.	B
IN1_N/GPI_3	5	OUT3 is enabled but cannot be controlled by the GPI_3 pin.	B
VDDR	6	Circuits that are powered by the VDDR pin are not powered up. See LMK3H2108-Q1 datasheet for the circuits powered by the VDDR pin,	B
IN2_P/GPI_4	7	OUT4 is enabled but cannot be controlled by the GPI_4 pin.	B
IN2_N/GPI_5	8	OUT5 is enabled but cannot be controlled by the GPI_5 pin.	B
SCL	9	There is no I2C communication.	B
SDA	10	There is no I2C communication.	B
VDDD	11	The device is not powered up properly.	B
GPIO_0	12	The OTP page selection does not work properly.	B
GPIO_1	13	The OTP page selection does not work properly.	B
GPIO_2	14	OUT6 is enabled but cannot be controlled by the GPIO_2 pin.	B
GPIO_3	15	OUT7 is enabled but cannot be controlled by the GPIO_3 pin.	B
GPIO_4	16	The device is powered up but the power-up sequence is not controlled by the PWRGD pin. The PWRDN function does not work.	B
NC	17	There is no impact to the device.	D
VDDO_0	18	The OUT0 driver is not powered up, there is no clock output.	B
OUT0_N	19	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT0_P	20	There is no impact to the device, but the receiver cannot receive the clock.	D
VDDO_1_2	21	The OUT1 and OUT2 drivers are not powered up, there is no clock output.	B
OUT1_N	22	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT1_P	23	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT2_N	24	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT2_P	25	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT3_N	26	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT3_P	27	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT4_N	28	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT4_P	29	There is no impact to the device, but the receiver cannot receive the clock.	D
VDDO_3_4	30	The OUT3 and OUT4 drivers are not powered up, there is no clock output.	B
OUT5_N	31	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT5_P	32	There is no impact to the device, but the receiver cannot receive the clock.	D
VDDO_5	33	The OUT5 driver is not powered up, there is no clock output.	B
VDDO_6	34	The OUT6 driver is not powered up, there is no clock output.	B
OUT6_N	35	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT6_P	36	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT7_N	37	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT7_P	38	There is no impact to the device, but the receiver cannot receive the clock.	D
VDDO_7	39	The OUT7 driver is not powered up, there is no clock output.	B
VDDA	40	The device is not powered up properly.	B
DAP	41	There is no ground connection. The device does not operate.	B

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN0_P/GPI_0	1	IN0_N/GPI_1	The GPI_0 and GPI_1 controls conflict.	B
IN0_N/GPI_1	2	VDDX	OUT1 is disabled and cannot be controlled by the GPI_1 pin.	B
VDDX	3	IN1_P/GPI_2	OUT2 is disabled and cannot be controlled by the GPI_2 pin.	B
IN1_P/GPI_2	4	IN1_N/GPI_3	The GPI_2 and GPI_3 controls conflict.	B
IN1_N/GPI_3	5	VDDR	OUT3 is disabled and cannot be controlled by the GPI_3 pin.	B
VDDR	6	IN2_P/GPI_4	OUT4 is disabled and cannot be controlled by the GPI_4 pin.	B
IN2_P/GPI_4	7	IN2_N/GPI_5	The GPI_4 and GPI_5 controls conflict.	B
IN2_N/GPI_5	8	SCL	The GPI_5 and SCL signals conflict.	B
SCL	9	SDA	There is no I2C communication.	B
SDA	10	VDDD	The pin is not considered. The pin is a corner pin.	D
VDDD	11	GPIO_0	The OTP page selection does not work properly.	B
GPIO_0	12	GPIO_1	The OTP page selection does not work properly.	B
GPIO_1	13	GPIO_2	The GPIO_1 and GPIO_2 controls conflict.	B
GPIO_2	14	GPIO_3	The GPIO_2 and GPIO_3 controls conflict.	B
GPIO_3	15	GPIO_4	The GPIO_3 and GPIO_4 controls conflict.	B
GPIO_4	16	NC	There is no impact to the device.	D
NC	17	VDDO_0	There is no impact to the device.	D
VDDO_0	18	OUT0_N	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT0_N	19	OUT0_P	There is a loss of clock output.	B
OUT0_P	20	VDDO_1_2	The pin is not considered. The pin is a corner pin.	D
VDDO_1_2	21	OUT1_N	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT1_N	22	OUT1_P	There is a loss of clock output.	B
OUT1_P	23	OUT2_N	There is a loss of clock output.	B
OUT2_N	24	OUT2_P	There is a loss of clock output.	B
OUT2_P	25	OUT3_N	There is a loss of clock output.	B
OUT3_N	26	OUT3_P	There is a loss of clock output.	B
OUT3_P	27	OUT4_N	There is a loss of clock output.	B
OUT4_N	28	OUT4_P	There is a loss of clock output.	B
OUT4_P	29	VDDO_3_4	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_3_4	30	OUT5_N	The pin is not considered. The pin is a corner pin.	D
OUT5_N	31	OUT5_P	There is a loss of clock output.	B
OUT5_P	32	VDDO_5	There is no output clock. High current flowing through output transistors for a long time can cause device damage	A
VDDO_5	33	VDDO_6	There is potential crosstalk between VDDO_5 and VDDO_6. There is no impact in this example since OUT5 and OUT6 are the same frequency.	D
VDDO_6	34	OUT6_N	There is no output clock. High current flowing through output transistors for a long time can cause device damage	A
OUT6_N	35	OUT6_P	There is a loss of clock output.	B
OUT6_P	36	OUT7_N	There is a loss of clock output.	B
OUT7_N	37	OUT7_P	There is a loss of clock output.	B
OUT7_P	38	VDDO_7	There is no output clock. High current flowing through output transistors for a long time can cause device damage	A
VDDO_7	39	VDDA	There is potential crosstalk noise from VDDO_7 to VDDA. There are increased jitter or spurs.	C
VDDA	40	IN0_P/GPI_0	The pin is not considered. The pin is a corner pin.	D

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
DAP	41	All pins	The same behaviors as described in <a href="#">Table 4-2</a> .	N/A

**Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN0_P/GPI_0	1	OUT0 is disabled and cannot be controlled by the GPI_0 pin.	B
IN0_N/GPI_1	2	OUT1 is disabled and cannot be controlled by the GPI_1 pin.	B
VDDX	3	There is no impact to the device.	D
IN1_P/GPI_2	4	OUT2 is disabled and cannot be controlled by the GPI_2 pin.	B
IN1_N/GPI_3	5	OUT3 is disabled and cannot be controlled by the GPI_3 pin.	B
VDDR	6	There is no impact to the device.	D
IN2_P/GPI_4	7	OUT4 is disabled and cannot be controlled by the GPI_4 pin.	B
IN2_N/GPI_5	8	OUT5 is disabled and cannot be controlled by the GPI_5 pin.	B
SCL	9	There is no I2C communication.	B
SDA	10	There is no I2C communication.	B
VDDD	11	There is no impact to the device.	D
GPIO_0	12	The OTP page selection does not work properly.	B
GPIO_1	13	The OTP page selection does not work properly.	B
GPIO_2	14	OUT6 is disabled and cannot be controlled by the GPIO_2 pin.	B
GPIO_3	15	OUT7 is disabled and cannot be controlled by the GPIO_3 pin.	B
GPIO_4	16	The device is powered up but the power-up sequence is not controlled by the PWRGD pin. The PWRDN function does not work.	B
NC	17	There is no impact to the device.	D
VDDO_0	18	There is no impact to the device.	D
OUT0_N	19	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT0_P	20	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_1_2	21	There is no impact to the device.	D
OUT1_N	22	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT1_P	23	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT2_N	24	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT2_P	25	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT3_N	26	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT3_P	27	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT4_N	28	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT4_P	29	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_3_4	30	There is no impact to the device.	D
OUT5_N	31	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A

**Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD (continued)**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT5_P	32	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_5	33	There is no impact to the device.	D
VDDO_6	34	There is no impact to the device.	D
OUT6_N	35	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT6_P	36	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT7_N	37	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT7_P	38	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_7	39	There is no impact to the device.	D
VDDA	40	There is no impact to the device.	D
DAP	41	A power-ground short can damage the device.	A

## 4.2 LMK3H2104-Q1

This section provides a failure mode analysis (FMA) for the pins of the LMK3H2104-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

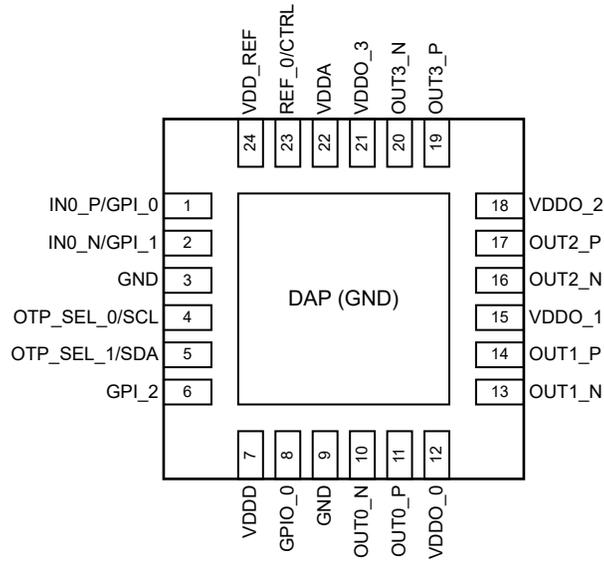
- Pin short-circuited to ground (see [Table 4-7](#))
- Pin open-circuited (see [Table 4-8](#))
- Pin short-circuited to an adjacent pin (see [Table 4-9](#))
- Pin short-circuited to VDD (see [Table 4-10](#))

[Table 4-7](#) through [Table 4-10](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-6](#).

**Table 4-6. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-2](#) shows the LMK3H2104-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LMK3H2104-Q1 data sheet.



**Figure 4-2. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- VDDD = VDDA = VDD\_REF = VDDO\_x = 3.3V
- GPI\_0 = OE0#, GPI\_1 = OE1#, GPI\_2 = OE2#, GPIO\_0 = OE3#. OEx# means output enable for OUTx, active low. An internal pulldown resistor is enabled on GPI\_0, GPI\_1, GPI\_2, and GPIO\_0.
- The device is configured to I2C-Mode.
- OTP\_SEL0/SCL and OTP\_SEL1/SDA are connected to an I2C bus.
- OUT0 to OUT3 are configured as 100MHz LP-HCSL.
- REF\_0/CTRL is configured as 25MHz LVCMOS output.
- REF\_0/CTRL is pulled down internally.

**Table 4-7. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN0_P/GPI_0	1	OUT0 is enabled but cannot be controlled by the GPI_0 pin.	B
IN0_N/GPI_1	2	OUT1 is enabled but cannot be controlled by the GPI_1 pin.	B
GND	3	There is no impact to the device.	D
OTP_SEL_0/SCL	4	There is no I2C communication.	B
OTP_SEL_1/SDA	5	There is no I2C communication.	B
GPI_2	6	OUT2 is enabled but cannot be controlled by the GPI_2 pin.	B
VDDD	7	A power-ground short can damage the device.	A
GPIO_0	8	OUT3 is enabled but cannot be controlled by the GPIO_0 pin.	B
GND	9	There is no impact to the device.	D
OUT0_N	10	There is a loss of clock output.	B
OUT0_P	11	There is a loss of clock output.	B
VDDO_0	12	A power-ground short can damage the device.	A
OUT1_N	13	There is a loss of clock output.	B
OUT1_P	14	There is a loss of clock output.	B
VDDO_1	15	A power-ground short can damage the device.	A
OUT2_N	16	There is a loss of clock output.	B
OUT2_P	17	There is a loss of clock output.	B
VDDO_2	18	A power-ground short can damage the device.	A
OUT3_P	19	There is a loss of clock output.	B

**Table 4-7. Pin FMA for Device Pins Short-Circuited to Ground (continued)**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT3_N	20	There is a loss of clock output.	B
VDDO_3	21	A power-ground short can damage the device.	A
VDDA	22	A power-ground short can damage the device.	A
REF_0/CTRL	23	There is a loss of clock output.	B
VDD_REF	24	A power-ground short can damage the device.	A
DAP		There is no impact to the device.	D

**Table 4-8. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN0_P/GPI_0	1	OUT0 is enabled but cannot be controlled by the GPI_0 pin.	B
IN0_N/GPI_1	2	OUT1 is enabled but cannot be controlled by the GPI_1 pin.	B
GND	3	The left side of the die is not grounded. Some circuits are not functional.	B
OTP_SEL_0/SCL	4	There is no I2C communication.	B
OTP_SEL_1/SDA	5	There is no I2C communication.	B
GPI_2	6	OUT2 is enabled but cannot be controlled by the GPI_2 pin.	B
VDDD	7	The device is not powered up properly.	B
GPIO_0	8	OUT3 is enabled but cannot be controlled by the GPIO_0 pin.	B
GND	9	The bottom side of the die is not grounded. Some circuits are not functional.	B
OUT0_N	10	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT0_P	11	There is no impact to the device, but the receiver cannot receive the clock.	D
VDDO_0	12	The OUT0 driver is not powered up, there is no clock output.	B
OUT1_N	13	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT1_P	14	There is no impact to the device, but the receiver cannot receive the clock.	D
VDDO_1	15	The OUT1 driver is not powered up, there is no clock output.	B
OUT2_N	16	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT2_P	17	There is no impact to the device, but the receiver cannot receive the clock.	D
VDDO_2	18	The OUT2 driver is not powered up, there is no clock output.	B
OUT3_P	19	There is no impact to the device, but the receiver cannot receive the clock.	D
OUT3_N	20	There is no impact to the device, but the receiver cannot receive the clock.	D
VDDO_3	21	The OUT3 driver is not powered up, there is no clock output.	B
VDDA	22	The device is not powered up properly.	B
REF_0/CTRL	23	At power-up, the device cannot enter OTP mode. After power-up, there is no impact on the device, but the receiver cannot receive the clock.	D
VDD_REF	24	The device is not power up properly.	B
DAP		The top side and right side of the die are not grounded. Some circuits are not functional.	B

**Table 4-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN0_P/GPI_0	1	IN0_N/GPI_1	GPI_0 and GPI_1 controls conflict.	B
IN0_N/GPI_1	2	GND	OUT1 is enabled but cannot be controlled by the GPI_1 pin.	B
GND	3	OTP_SEL_0/SCL	There is no I2C communication.	B
OTP_SEL_0/SCL	4	OTP_SEL_1/SDA	There is no I2C communication.	B
OTP_SEL_1/SDA	5	GPI_2	GPI_2 and SDA signals conflict.	B
GPI_2	6	VDDD	The pin is not considered. The pin is a corner pin.	D

**Table 4-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VDDD	7	GPIO_0	OUT3 is disabled and cannot be controlled by the GPIO_0 pin.	B
GPIO_0	8	GND	OUT3 is enabled but cannot be controlled by the GPIO_0 pin.	B
GND	9	OUT0_N	There is a loss of clock output.	B
OUT0_N	10	OUT0_P	There is a loss of clock output.	B
OUT0_P	11	VDDO_0	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_0	12	OUT1_N	The pin is not considered. The pin is a corner pin.	D
OUT1_N	13	OUT1_P	There is a loss of clock output.	B
OUT1_P	14	VDDO_1	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_1	15	OUT2_N	There is no output clock. High current flowing through output transistors for a long time can cause device damage	A
OUT2_N	16	OUT2_P	There is a loss of clock output.	B
OUT2_P	17	VDDO_2	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_2	18	OUT3_P	The pin is not considered. The pin is a corner pin.	D
OUT3_P	19	OUT3_N	There is a loss of clock output.	B
OUT3_N	20	VDDO_3	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_3	21	VDDA	There is potential crosstalk noise from VDDO_3 to VDDA. There is increased jitter or spurs.	C
VDDA	22	REF_0/CTRL	At power-up, the device cannot enter I2C mode. After power-up, REF_0 has no clock output. High current flowing through output transistors for a long time can cause device damage.	A
REF_0/CTRL	23	VDD_REF	At power-up, the device cannot enter I2C mode. After power-up, REF_0 has no clock output. High current flowing through output transistors for a long time can cause device damage.	A
VDD_REF	24	IN0_P/GPI_0	The pin is not considered. The pin is a corner pin.	D
DAP	25	All pins	The same behavior as described in <a href="#">Table 4-7</a> .	N/A

**Table 4-10. Pin FMA for Device Pins Short-Circuited to VDD**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN0_P/GPI_0	1	OUT0 is disabled and cannot be controlled by the GPI_0 pin.	B
IN0_N/GPI_1	2	OUT1 is disabled and cannot be controlled by the GPI_1 pin.	B
GND	3	A power-ground short can damage the device.	A
OTP_SEL_0/SCL	4	There is no I2C communication.	B
OTP_SEL_1/SDA	5	There is no I2C communication.	B
GPI_2	6	OUT2 is disabled and cannot be controlled by the GPI_2 pin.	B
VDDD	7	There is no impact to the device.	D
GPIO_0	8	OUT3 is disabled and cannot be controlled by the GPIO_0 pin.	B
GND	9	A power-ground short can damage the device.	A
OUT0_N	10	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT0_P	11	There is no output cloc. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_0	12	There is no impact to the device.	D
OUT1_N	13	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A

**Table 4-10. Pin FMA for Device Pins Short-Circuited to VDD (continued)**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT1_P	14	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_1	15	There is no impact to the device.	D
OUT2_N	16	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT2_P	17	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_2	18	There is no impact to the device.	D
OUT3_P	19	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
OUT3_N	20	There is no output clock. High current flowing through output transistors for a long time can cause device damage.	A
VDDO_3	21	There is no impact to the device.	D
VDDA	22	There is no impact to the device.	D
REF_0/CTRL	23	At power-up, the device cannot enter I2C mode. After power-up, REF_0 has no clock output. High current flowing through output transistors for a long time can cause device damage.	A
VDD_REF	24	There is no impact to the device.	D
DAP		A power-ground short can damage the device.	A

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2025	*	Initial Release

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