Functional Safety Information

OPA810-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the OPA810-Q1 (SOT-23 | DBV package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

OPA810-Q1 shows the device functional block diagram for reference.

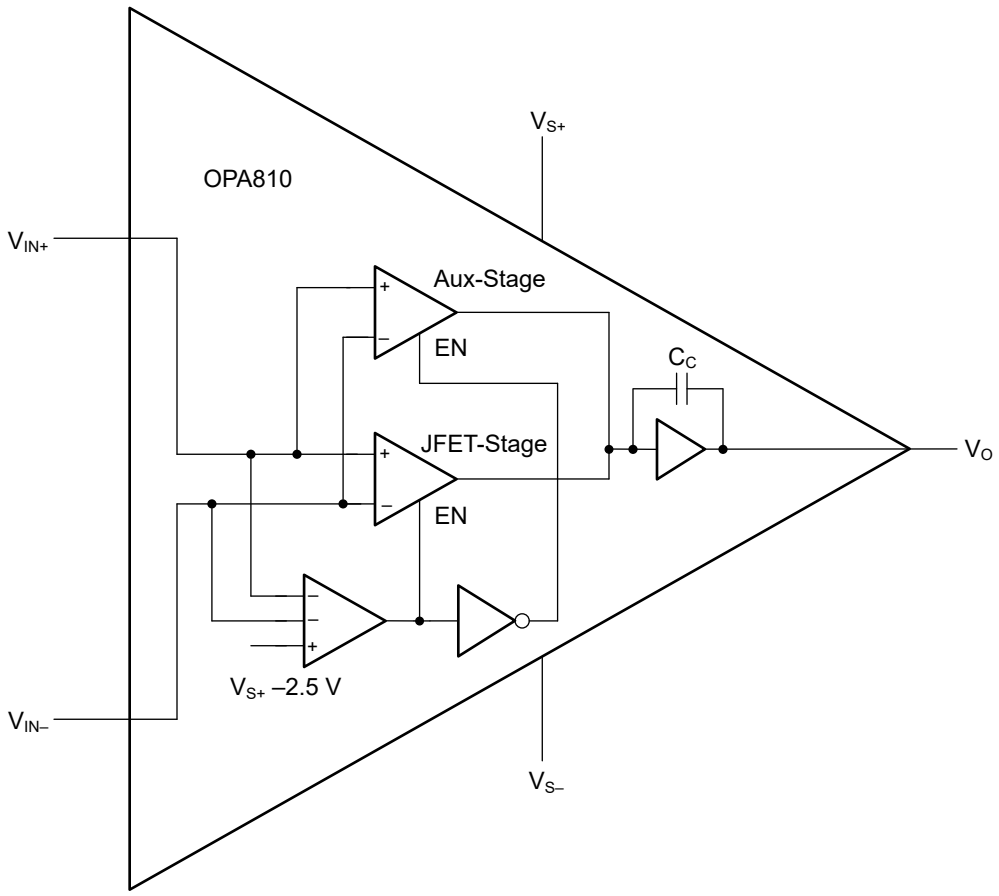

Figure 1-1. Functional Block Diagram

OPA810-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT-23 | DBV Package

This section provides functional safety failure in time (FIT) rates for the SOT-23 | DBV package of the OPA810-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	5
Die FIT rate	3
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 53mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op amp, comparators, and voltage monitors	4 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the OPA810-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output is floating, open	20
Output is stuck, high	20
Output is stuck, low	20
Output functional, not in specification	40

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the OPA810-Q1 (SOT-23 | DBV package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V+ (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- A total supply voltage of 10V, with the V+ connected to 5V and the V- connected to -5V.
- The input and output pins are biased to a GND reference point.
- The device is configured with the feedback network in a gain greater than or equal to 1V/V.

4.1 SOT-23 | DBV Package

Figure 4-1 shows the OPA810-Q1 pin diagram for the SOT-23 | DBV package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the OPA810-Q1 data sheet.

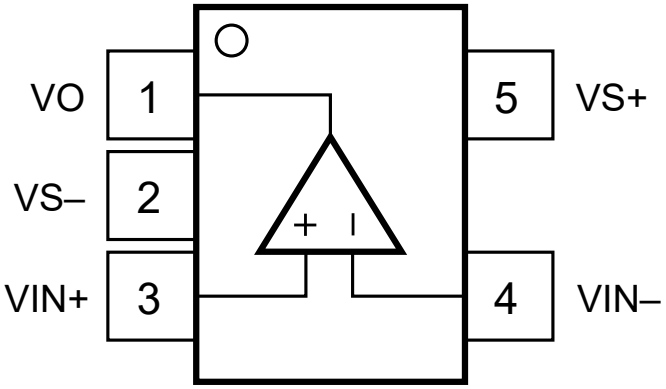

Figure 4-1. Pin Diagram (SOT-23 | DBV) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VO	1	A short to GND can cause the device to overheat.	B
VS-	2	Diodes from input to VS- can turn on due to an input signal and cause electrical overstress (EOS). Normal operation if a single supply voltage is intended.	A
VIN+	3	An input at GND (mid-supply) is a valid input, however, the desired application result is unlikely.	C
VIN-	4	An input at GND (mid-supply) is a valid input, however, the desired application result is unlikely.	C
VS+	5	Diodes from input to VS+ can turn on due to an input signal and cause electrical overstress (EOS).	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VO	1	The output can be left open. There is no effect on the device, but the output is not measured.	C
VS-	2	The lowest voltage output pin tries to power the VS- pin of the device.	B
VIN+	3	Floating input, circuit likely does not function as expected.	C
VIN-	4	Floating input, circuit likely does not function as expected.	C
VS+	5	The highest voltage output pin tries to power the VS+ pin of the device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VO	1	VS-	A short to VS- can cause device to overheat.	B
VS-	2	VIN+	An input at VS- is a valid input, however, the desired application result is unlikely.	C
VIN+	3	VIN-	No damage to the device. The application circuit does not work. The pins are not physically near to each other.	C
VIN-	4	VS+	An input at VS+ is a valid input, however, the desired application result is unlikely. Pins are not as near to each other due to package type.	B
VS+	5	VO	A short to VS+ can cause the device to overheat. The pins are not physically near to each other.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to V+

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VO	1	A short to VS+ can cause the device to overheat.	B
VS-	2	Diodes from input to VS- can turn on due to an input signal and cause electrical overstress (EOS).	A
VIN+	3	An input at VS+ is a valid input, however, the desired application result is unlikely.	C
VIN-	4	An input at VS+ is a valid input, however, the desired application result is unlikely.	C
VS+	5	Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2025	*	Initial Release

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