Functional Safety Information

LMR36506 and LMR36503 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LMR36506 and LMR36503 (VQFN-HR package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

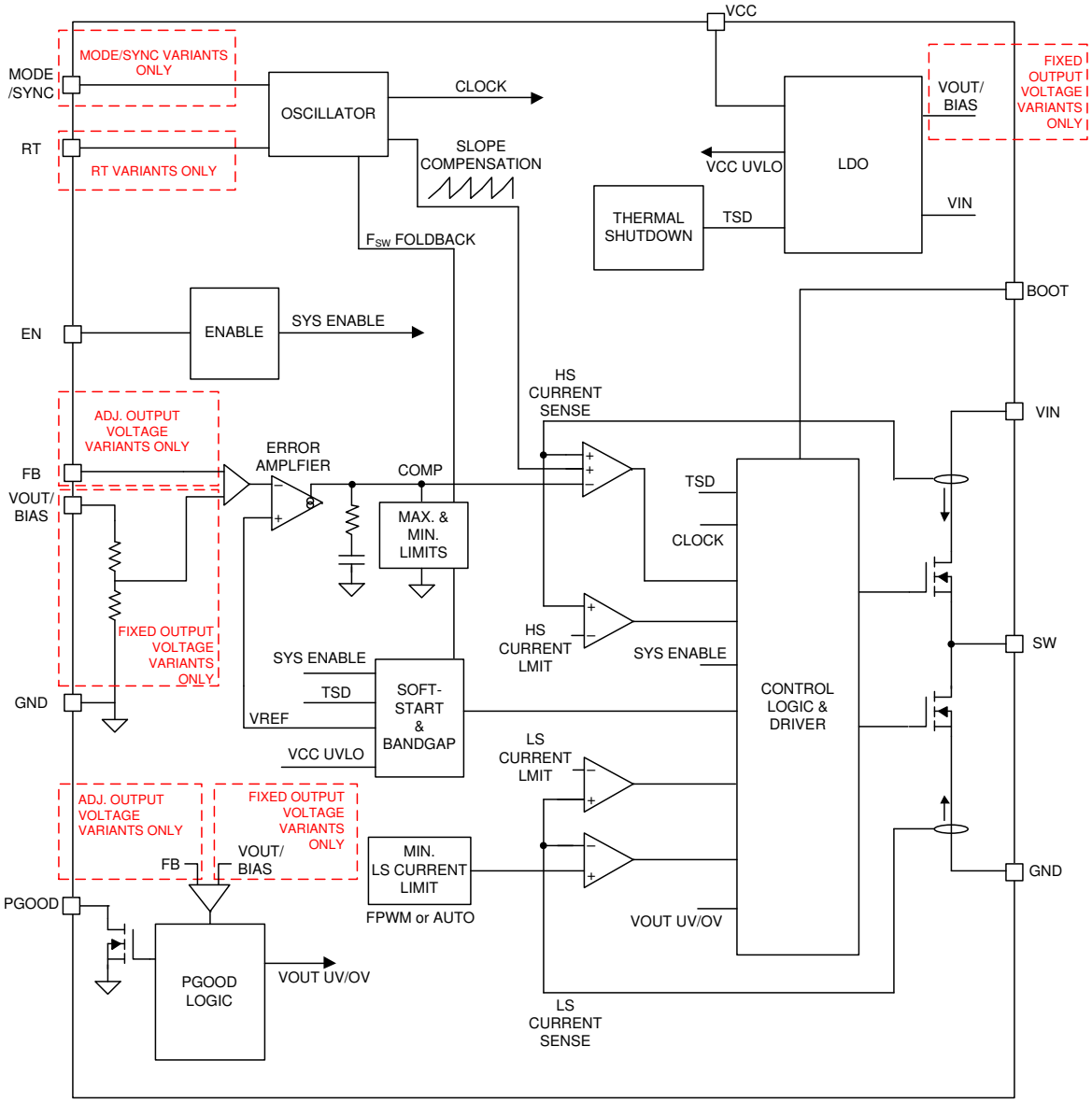


Figure 1-1. Functional Block Diagram

LMR36506 and LMR36503 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

2.1 LMR36506

This section provides functional safety failure in time (FIT) rates for LMR36506 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	20
Die FIT rate	12
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 600mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs, analog and mixed HV > 50V supply	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 LMR36503

This section provides functional safety failure in time (FIT) rates for LMR36503 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	14
Die FIT rate	6
Package FIT rate	8

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 300mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs, analog and mixed HV > 50V supply	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR36506 and LMR36503 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	60
Output not in specification—voltage or timing	30
Gate driver stuck on	5
Power Good—false trip or failure to trip	5

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMR36506 and LMR36503. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

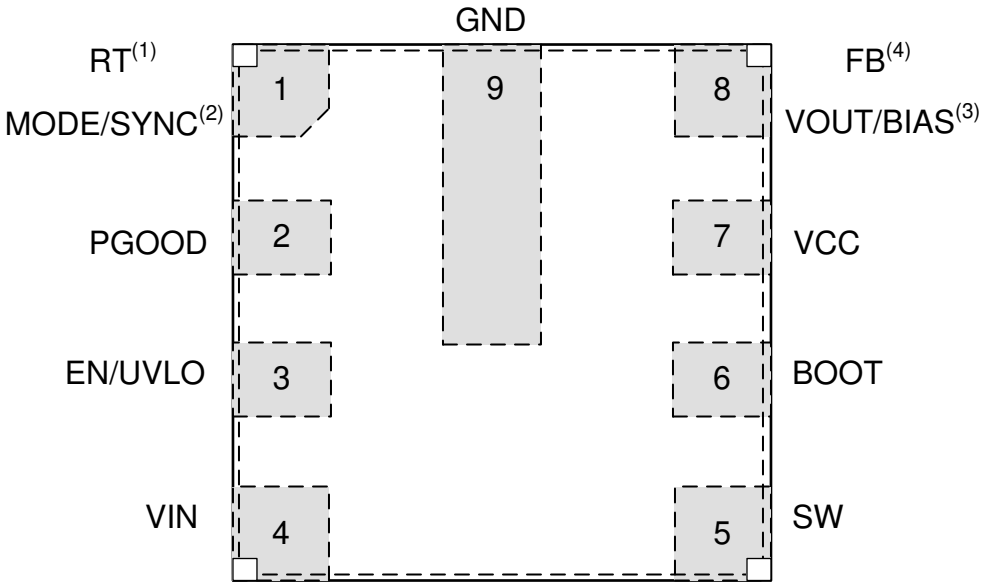
- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LMR36506 and LMR36503 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LMR36506 and LMR36503 data sheet.



1. See the *data sheet* for more details. Pin 1 is trimmed and factory-set for externally-adjustable-switching frequency RT variants only.
2. Pin 1 is factory-set for fixed-switching frequency MODE/SYNC variants only.
3. Pin 8 is trimmed and factory-set for fixed-output voltage VOUT/BIAS variants only.
4. Pin 8 is factory-set for adjustable-output voltage FB variants only.

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RT or MODE	1	The switching frequency is 2.2MHz.	D
PGOOD	2	When not in use, the pin can be left grounded (PGOOD is not a valid signal, VOUT is normal).	D
EN/UVLO	3	VOUT = 0V (enable is off and functionality is halted).	D
VIN	4	VOUT = 0V.	B
SW	5	There is damage to the high-side FET.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
BOOT	6	VOUT = 0V. The high-side FET does not turn on.	B
VCC	7	VOUT = 0V.	B
VOUT/BIAS or FB	8	VOUT = 0V.	B
GND	9	VOUT is normal.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RT or MODE	1	If the part is an RT part, the frequency is not defined. If the part is a MODE/SYNC part, the part can go back and forth between FPWM/PFM. The part is up and functional.	D
PGOOD	2	When not in use, the pin can be left open (PGOOD is not a valid signal, VOUT is normal).	D
EN/UVLO	3	The pin cannot be left floating.	B
VIN	4	VOUT = 0V.	B
SW	5	VOUT = 0V.	B
BOOT	6	VOUT = 0. The high-side FET does not turn on.	B
VCC	7	The VCC output is unstable, the output can increase above 5.5V.	A
VOUT/BIAS or FB	8	VOUT = 0V. Do not float this pin.	C
GND	9	VOUT can be abnormal, as the reference voltage is not fixed.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
RT or MODE	1	PGOOD	If PGOOD is high and < 5.5V, Fsw = 1MHz; If PGOOD is low, Fsw = 2.2MHz. Since the absolute maximum of the PGOOD pin is 20V, the RT ESD is damaged if PG goes to 20V.	A
PGOOD	2	EN/UVLO	If EN/UVLO >20V, devices that are connected to the PGOOD pin are damaged.	A
EN/UVLO	3	VIN	VOUT is normal (enable is on and all other blocks work).	D
VIN	4	SW	There is damage to the low-side FET.	A
SW	5	BOOT	VOUT = 0V. The high-side FET does not turn on; no Cboot.	B
BOOT	6	VCC	Damage occurs, the VCC pin breaks.	A
VCC	7	VOUT/BIAS or FB	The device does not work, but no damage occurs.	B
VOUT/BIAS or FB	8	GND	VOUT = 0V.	B
GND	9	RT or MODE	VOUT is normal if the RT or MODE/SYNC pins are low; otherwise, the device is not functional.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RT or MODE	1	If VIN > 5.5V, damage occurs. If VIN <5.5V, the switching frequency is 1MHz.	A
PGOOD	2	If VIN >20V, PGOOD is damaged.	A
EN/UVLO	3	VOUT is normal (enable is on and all other blocks work).	D
VIN	4	VOUT is normal.	D
SW	5	There is damage to the low-side FET.	A
BOOT	6	Damage occurs, the BOOT ESD clamp is damaged.	A
VCC	7	If VIN > 5.5V, damage occurs.	A
VOUT/BIAS or FB	8	If VIN > 20V, damage occurs.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	9	VOUT = 0V.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

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