Functional Safety Information

LMH6551Q-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LMH6551Q-Q1 (DGK package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

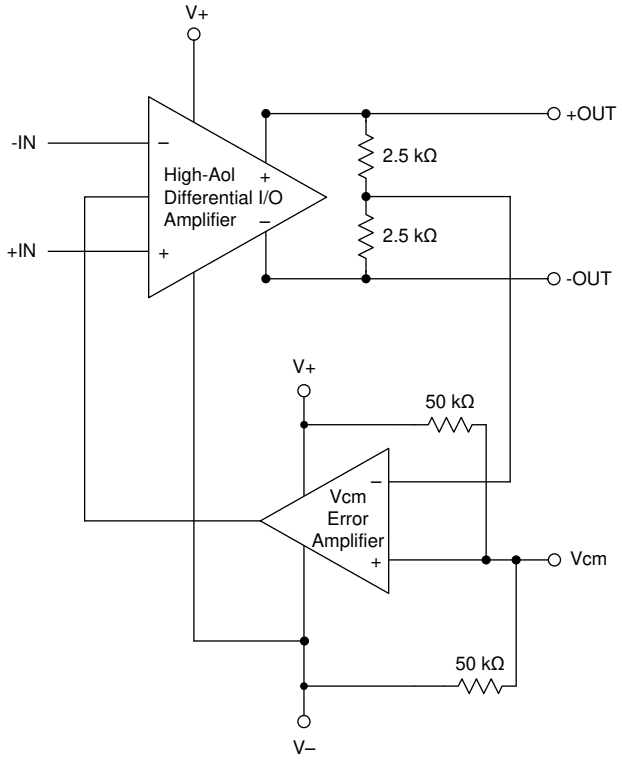

Figure 1-1. Functional Block Diagram

LMH6551Q-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LMH6551Q-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	12
Die FIT rate	8
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 229mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Bipolar operation amplifier, comparators, and voltage monitors	12 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMH6551Q-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
V_{OUT+} open V_{OUT-} open	20
V_{OUT+} to V_{S-} V_{OUT-} to V_{S-}	20
V_{OUT+} to VS+ V_{OUT-} to VS+	20
V_{OUT+} or V_{OUT-} functional, not in specification	35
Pin-to-pin short, any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMH6551Q-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V+ (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LMH6551Q-Q1 pin diagram. For a detailed description of the device pins please refer to the *Connection Diagram* section in the LMH6551Q-Q1 datasheet.

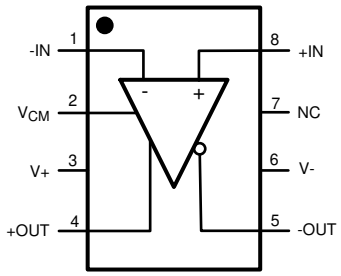

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is running in the typical application, please refer to the *Typical Application* graphic in the LMH6551Q-Q1 datasheet.
- A total supply voltage of 10V with V+ connected to 5V and V- connected to –5V is implemented.
- The input and output pins are biased to a GND reference point.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN-	1	An input at mid-supply (GND) is a valid input; however, the desired result for the application is unlikely.	C
V_{CM}	2	The device operates as normal, unless a single supply voltage is intended.	D
V+	3	The diodes from the input to the V+ pin potentially turn on due to an input signal and this results in electrical overstress (EOS).	A
+OUT	4	The device potentially overheats.	B
-OUT	5	The device potentially overheats.	B
V-	6	The diodes from the input to the V- pin potentially turn on due to an input signal and cause electrical overstress (EOS). The device operates as normal if a single supply configuration is used.	A
NC	7	The device operates as normal. The pin has no internal connection.	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	8	An input at mid-supply (GND) is a valid input; however, the desired result for the application is unlikely.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN-	1	The input is floating, the circuit potentially does not function as expected.	C
V_{CM}	2	The device operates as normal. The output common-mode is set to mid-supply.	D
V+	3	The output pin with the highest voltage tries to power the V+ pin of the device.	B
OUT+	4	The output can be left open. There is no effect on the device, but the output is not measured.	C
OUT-	5	The output can be left open. There is no effect on the device, but the output is not measured.	C
V-	6	The output pin with the lowest voltage tries to power the V- pin of the device.	B
NC	7	The device operates as normal. The NC pin has no internal connection.	D
IN+	8	There input is floating, the circuit likely does not function as expected.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
1	IN-	V_{CM}	Tying the input pin to the V_{CM} pin is valid; however, the desired result for the application is unlikely.	C
2	V_{CM}	V+	Tying the V_{CM} pin to the V+ pin is valid; however, the desired result for the application is unlikely.	C
3	V+	OUT+	Tying the V+ pin to the output pin is valid; however, the desired result for the application is unlikely.	C
4	OUT+	OUT-	TI does not recommend tying the output pin to the other output pin; the desired result for the application is unlikely, the device potentially overheats and damage occurs. The pins are separated across the device package.	B
5	OUT-	V-	Tying the output pin to the V- pin is valid; however, the desired result for the application is unlikely.	C
6	V-	NC	The device operates as normal. The NC pin has no internal connection.	D
7	NC	IN-	The device operates as normal. The NC pin has no internal connection.	D
8	IN+	IN-	TI does not recommend tying the input pin to the other input pin; the desired result for the application is unlikely, the device potentially overheats and damage occurs. The pins are separated across the device package.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to V+

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
NC	7	The device operates as normal. The NC pin has no internal connection.	D
IN-	1	Input at V+ is a valid input; however, the desired result for the application is unlikely.	C
OUT+	4	The device potentially overheats.	B
V_{CM}	2	Tying the V_{CM} pin at the V+ pin is a valid input; however, the desired result for the application is unlikely.	C
V+	3	The device operates as normal.	D
OUT-	5	The device potentially overheats.	B
IN+	8	Input at V+ is a valid input; however, the desired result for the application is unlikely.	C
V-	6	The diodes from input to the V- pin potentially turn on due to an input signal and this results in electrical overstress (EOS).	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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