Functional Safety Information

UCC34141-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the UCC34141-Q1 (DHA-16 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

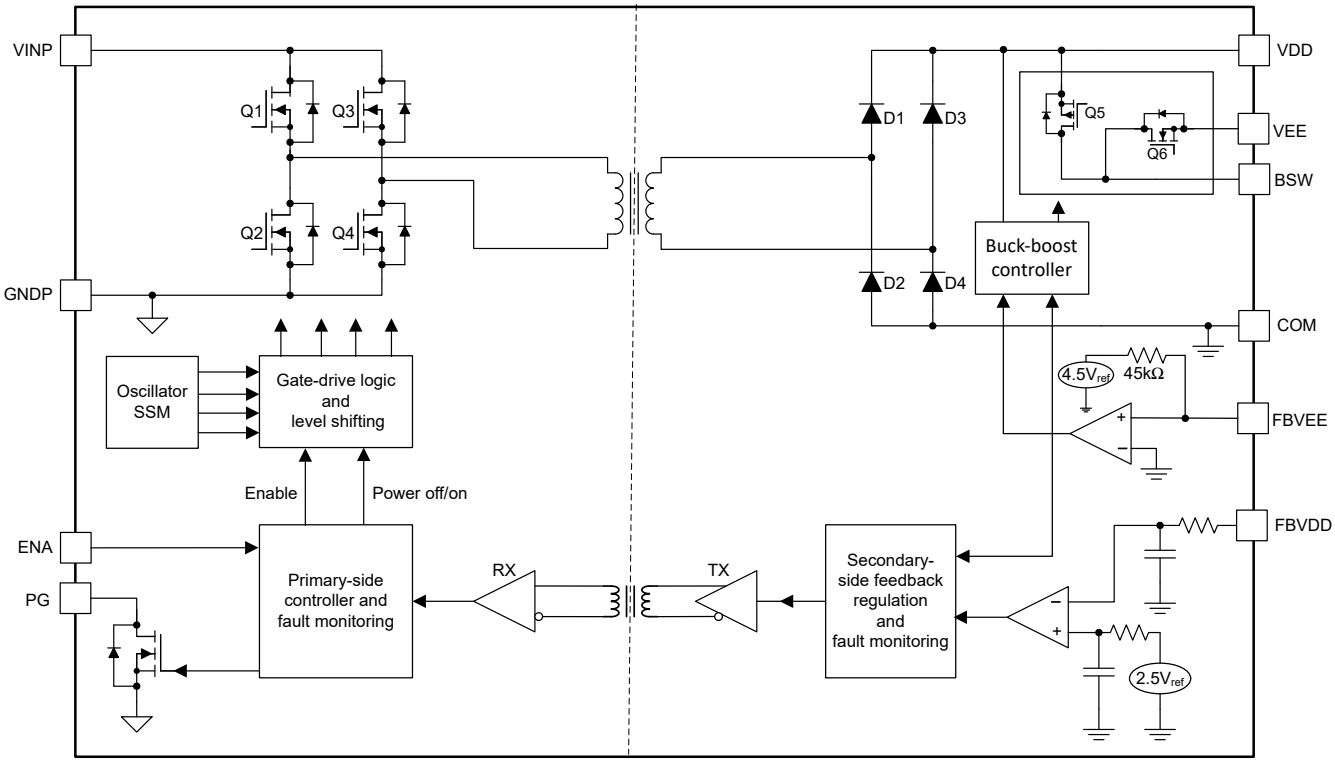

Figure 1-1. Functional Block Diagram

The UCC34141-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DHA-16 Package

This section provides functional safety failure in time (FIT) rates for the DHA-16 package of the UCC34141-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	1500	58
	1000	35
	500	24
Die FIT rate	1500	37
	1000	16
	500	7
Package FIT rate	1500	21
	1000	19
	500	17

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1500mW, 1000mW, 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the UCC34141-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VDD or VEE has no power	65
VDD or VEE accuracy not meeting specification	23
PG indicates the wrong state	1
Degraded EMI performance	10
Degraded testability (no mission impact)	1

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC34141-Q1 (DHA-16 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is configured as shown in the *Dual Adjustable Output Configuration* diagram in the *Typical Application* section of the datasheet
- The VIN pin is considered as the supply pin for the primary-side pins
- The GNDP pin is considered as the ground pin for the primary-side pins
- The VDD pin is considered as the supply pin for the secondary-side pins
- The VEE pin is considered as the ground pin for the secondary-side pins

4.1 DHA-16 Package

Figure 4-1 shows the UCC34141-Q1 pin diagram for the DHA-16 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC34141-Q1 datasheet.

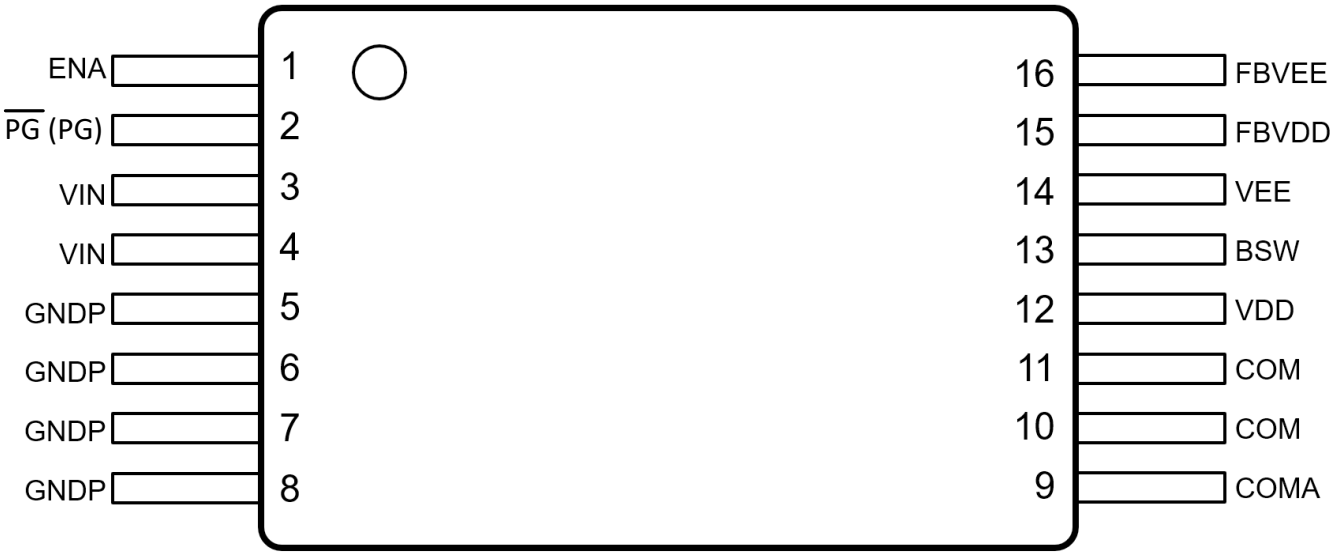

Figure 4-1. Pin Diagram (DHA-16) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ENA	1	The device is disabled. There is no output.	B
$\overline{\text{PG}}$ (PG)	2	The power good signal is always low. The MCU cannot detect the status of the bias supply.	C
VIN	3	The device is not powered. There is no output.	B
VIN	4	The device is not powered. There is no output.	B
GNDP	5	There is no effect on the device.	D
GNDP	6	There is no effect on the device.	D
GNDP	7	There is no effect on the device.	D
GNDP	8	There is no effect on the device.	D
COMA	9	There is no effect on the device.	D
COM	10	There is no effect on the device.	D
COM	11	There is no effect on the device.	D
VDD	12	The device is disabled. There is no output.	B
BSW	13	The device is disabled. There is no output.	B
VEE	14	The device is disabled. There is no output.	B
FBVDD	15	The device is disabled. There is no output.	B
FBVEE	16	The device is disabled. There is no output.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ENA	1	The state of the device is undetermined. The device can be on or off, depending on the noise on ENA pin.	B
$\overline{\text{PG}}$ (PG)	2	The MCU cannot detect the status of the bias supply.	C
VIN	3	There is no effect on the device.	D
VIN	4	There is no effect on the device.	D
GNDP	5	There is no effect on the device.	D
GNDP	6	There is no effect on the device.	D
GNDP	7	There is no effect on the device.	D
GNDP	8	There is no effect on the device.	D
COMA	9	The feedback reference voltage and the VDD regulation voltage have offset.	B
COM	10	There is no effect on the device.	D
COM	11	The power stage current goes through the internal diode. There is more noise on the feedback signals.	C
VDD	12	The device is disabled. There is no output.	B
BSW	13	The device is disabled. There is no output.	B
VEE	14	The device is disabled. There is no output.	B
FBVDD	15	The device is disabled. There is no output.	B
FBVEE	16	The device is disabled. There is no output.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ENA	1	$\overline{PG}$ (PG)	The device is disabled. There is no output.	B
$\overline{PG}$ (PG)	2	VIN	The absolute maximum rating is exceeded for the pin. Damage to the device is possible.	A
VIN	3	VIN	There is no effect on the device.	D
VIN	4	GNDP	The device is not powered. There is no output.	B
GNDP	5	GNDP	There is no effect on the device.	D
GNDP	6	GNDP	There is no effect on the device.	D
GNDP	7	GNDP	There is no effect on the device.	D
GNDP	8	N/A	N/A	N/A
COMA	9	COM	There is no effect on the device.	D
COM	10	COM	There is no effect on the device.	D
COM	11	VDD	The device is disabled. There is no output.	B
VDD	12	BSW	The device is disabled. There is no output.	B
BSW	13	VEE	The device is disabled. There is no output.	B
VEE	14	FBVDD	The device is disabled. There is no output.	B
FBVDD	15	FBVEE	The device is disabled. There is no output.	B
FBVEE	16	N/A	N/A	N/A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ENA	1	The absolute maximum rating is exceeded for the pin. Damage to the device is possible.	A
$\overline{PG}$ (PG)	2	The absolute maximum rating is exceeded for the pin. Damage to the device is possible.	A
VIN	3	There is no effect on the device.	D
VIN	4	There is no effect on the device.	D
GNDP	5	The device is not powered. There is no output.	B
GNDP	6	The device is not powered. There is no output.	B
GNDP	7	The device is not powered. There is no output.	B
GNDP	8	The device is not powered. There is no output.	B
COMA	9	The device is not powered. There is no output.	B
COM	10	The device is disabled. There is no output.	B
COM	11	The device is disabled. There is no output.	B
VDD	12	There is no effect on the device.	D
BSW	13	The device is disabled. There is no output.	B
VEE	14	The device is disabled. There is no output.	B
FBVDD	15	The device is disabled. There is no output.	B
FBVEE	16	The absolute maximum rating is exceeded for the pin. Damage to the device is possible.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2026	*	Initial Release

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