



Table of Contents

1 Overview	2
2 Functional Safety Failure In Time (FIT) Rates	3
2.1 DGS (VSSOP, 10) Package.....	3
2.2 DSQ (WSON, 10) Package.....	4
3 Failure Mode Distribution (FMD)	5
4 Pin Failure Mode Analysis (Pin FMA)	6
4.1 DGS (VSSOP, 10) and DSQ (WSON, 10) Packages.....	6
5 Revision History	8

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1 Overview

This document contains information for the TMP4719-Q1 (DGS (VSSOP, 10) and DSQ (WSON, 10) packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

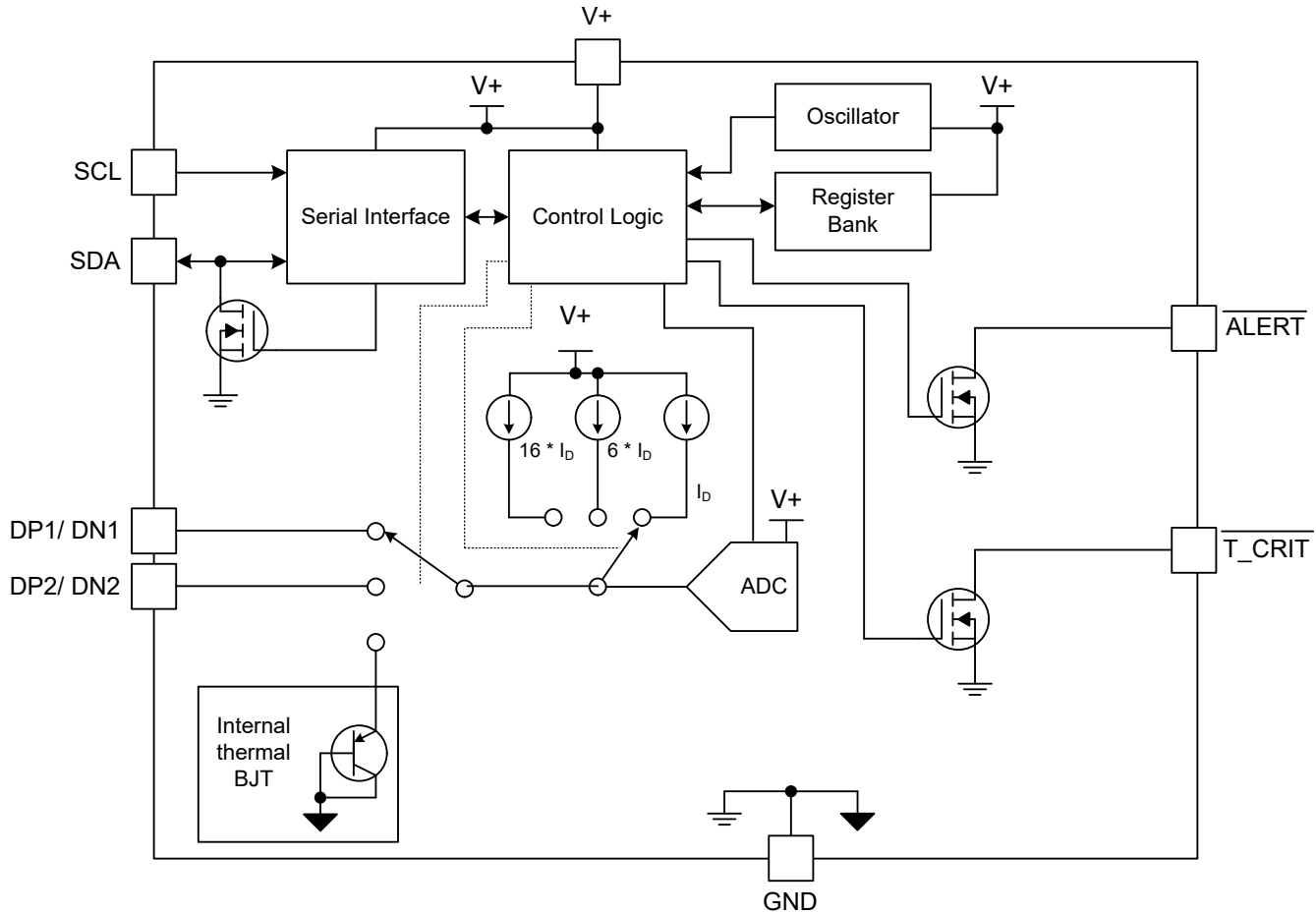


Figure 1-1. Functional Block Diagram

The TMP4719-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DGS (VSSOP, 10) Package

This section provides functional safety failure in time (FIT) rates for the TMP4719-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	6
Die FIT rate	2
Package FIT rate	4

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 2mW
- Climate type: World-wide table 8 or figure 13
- Package factor (λ_3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DSQ (WSON, 10) Package

This section provides functional safety failure in time (FIT) rates for the DSQ (WSON, 10) package of the TMP4719-Q1 based on two different industry-wide used reliability standards:

- [Table 2-3](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-4](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in [Table 2-3](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 and figure 16
- Power dissipation: 2mW
- Climate type: World-wide table 8 and figure 13
- Package factor (lambda 3): From table 17b and figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-4](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TMP4719-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Local temperature measurement error	30
Remote temperature measurement error	25
Serial communication error	30
Register bank data bit error	10
ALERT/T_crit false trip, fails to trip	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TMP4719-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- A bypass capacitor of 0.1 μ F on the input voltage pin is implemented.
- External pull-up resistor on SDA pin is implemented.

4.1 DGS (VSSOP, 10) and DSQ (WSON, 10) Packages

[Figure 4-1](#) and [Figure 4-2](#) shows the TMP4719-Q1 pin diagram for the DGS (VSSOP, 10) and DSQ (WSON, 10) packages. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMP4719-Q1 datasheet.

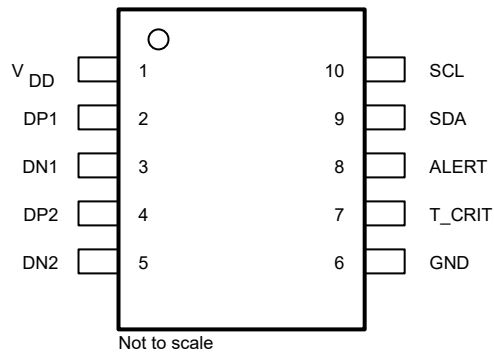


Figure 4-1. Pin Diagram (DGS (VSSOP, 10)) Package

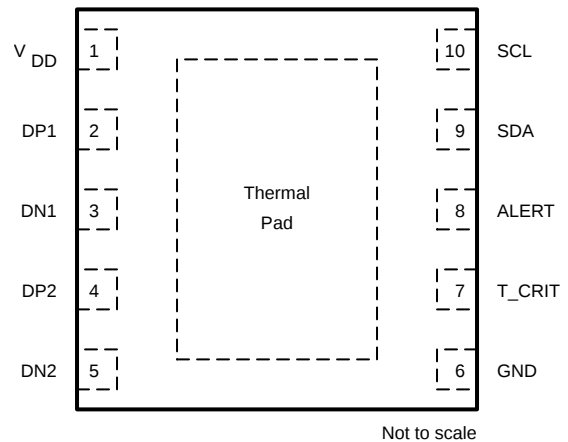


Figure 4-2. Pin Diagram (DSQ (WSON, 10)) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V _{DD}	1	The device is not powered. The device is not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is plausible.	A
DP1	2	The positive remote connection is stuck low. The remote temperature measurement is out of specification.	B
DN1	3	There is no effect. Operation is normal.	D
DP2	4	The positive remote connection is stuck low. The remote temperature measurement is out of specification.	B
DN2	5	There is no effect. Operation is normal.	D
GND	6	There is no effect. Operation is normal.	D
T_CRIT	7	T_CRIT is stuck low and is not functional. T_CRIT falsely asserts.	B
ALERT	8	ALERT is stuck low and is not functional. ALERT falsely asserts.	B
SDA	9	SDA is stuck low. I2C communication with the device is not possible.	B
SCL	10	SCL is stuck low. I2C communication with the device is not possible.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V _{DD}	1	The functionality of the device is undetermined. If there is voltage on the other pins, the device can power up through internal ESD diodes.	B
DP1	2	DP1 is undetermined. The channel 1 remote temperature measurement is out of specification.	B
DN1	3	DN1 is undetermined. The channel 1 remote temperature measurement is out of specification.	B
DP2	4	DP2 is undetermined. The channel 2 remote temperature measurement is out of specification.	B
DN2	5	DN2 is undetermined. The channel 2 remote temperature measurement is out of specification.	B
GND	6	The functionality of the device is undetermined. The device can be not powered or connected to ground internally through an alternate pin ESD diode and powered up.	B
T_CRIT	7	The state of T_CRIT is undetermined. T_CRIT can falsely assert or fail to assert.	B
ALERT	8	The state of ALERT is undetermined. ALERT can falsely assert or fail to assert.	B
SDA	9	The state of SDA is undetermined. I2C communication with the device is not possible.	B
SCL	10	The state of SDA is undetermined. I2C communication with the device is not possible.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
V _{DD}	1	DP1	DP1 is stuck high. The channel 1 remote temperature measurement is out of specification.	B
DP1	2	DN1	DP1 and the DN1 are shorted. The channel 1 remote temperature measurement is out of specification.	B
DN1	3	DP2	DN1 and DP2 are shorted. The channel 1 and 2 remote temperature measurements are out of specification.	B
DP2	4	DN2	DP2 and DN2 is shorted. The channel 2 remote temperature measurement is out of specification.	B
DN2	5	GND	There is no effect. Operation is normal.	D
GND	6	T_CRIT	T_CRIT is stuck low and not functional. T_CRIT falsely asserts.	B
T_CRIT	7	ALERT	T_CRIT and ALERT are shorted. T_CRIT or ALERT can falsely assert.	B
ALERT	8	SDA	The SDA communication line is stuck high or low. I2C communication with the device is not possible.	B
SDA	9	SCL	The communication lines are shorted. I2C communication with the device is not possible.	B
SCL	10	V _{DD}	SCL is stuck high. I2C communication with the device is not possible.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
V _{DD}	1	There is no effect. Operation is normal.	D
DP1	2	DP1 is stuck high. The channel 1 remote temperature measurement is out of specification.	B
DN1	3	DN1 is stuck high. The channel 1 remote temperature measurement is out of specification.	B
DP2	4	DP2 is stuck high. The channel 2 remote temperature measurement is out of specification.	B
DN2	5	DN2 is stuck high. The channel 2 remote temperature measurement is out of specification.	B
GND	6	The device functionality is undetermined. Observe that the absolute maximum ratings for all pins of the device are met, otherwise, device damage is plausible.	A
T_CRIT	7	T_CRIT is stuck high and is not functional. T_CRIT does not assert.	B
ALERT	8	ALERT is stuck high and is not functional. ALERT does not assert.	B
SDA	9	SDA is stuck high. I2C communication with the device is not possible.	B
SCL	10	SCL is stuck high. I2C communication with the device is not possible.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

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Last updated 10/2025