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1 Overview

This document contains information for the [TXE8124](#) (VSSOP and VQFN) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

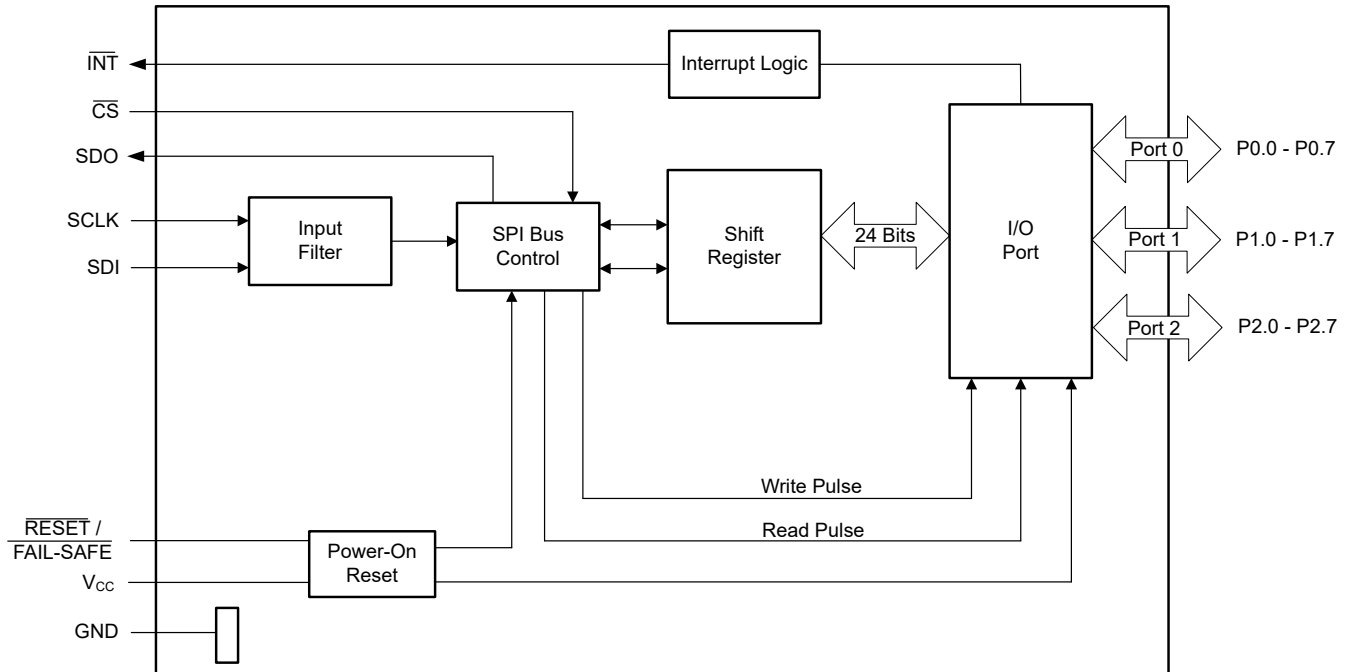


Figure 1-1. Functional Block Diagram

The TXE8124 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSSOP Package

This section provides functional safety failure in time (FIT) rates for the VSSOP package of the TXE8124 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	15
Die FIT rate	2
Package FIT rate	13

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 14.9mW
- Climate type: Table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VQFN Package

This section provides functional safety failure in time (FIT) rates for the VQFN package of the TXE8124 based on two different industry-wide used reliability standards:

- [Table 2-3](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-4](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	18
Die FIT rate	2
Package FIT rate	16

The failure rate and mission profile information in [Table 2-3](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 14.9mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-4](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TXE8124 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SPI communication error	30
Power management (LDO) error	6
Logic blocks error	6
I/O blocks error	58

4 Pin Failure Mode Analysis (Pin FMA)

4.1 VSSOP Package

This section provides a failure mode analysis (FMA) for the pins of the TXE8124. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to VCC (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the TXE8124 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TXE8124 datasheet.

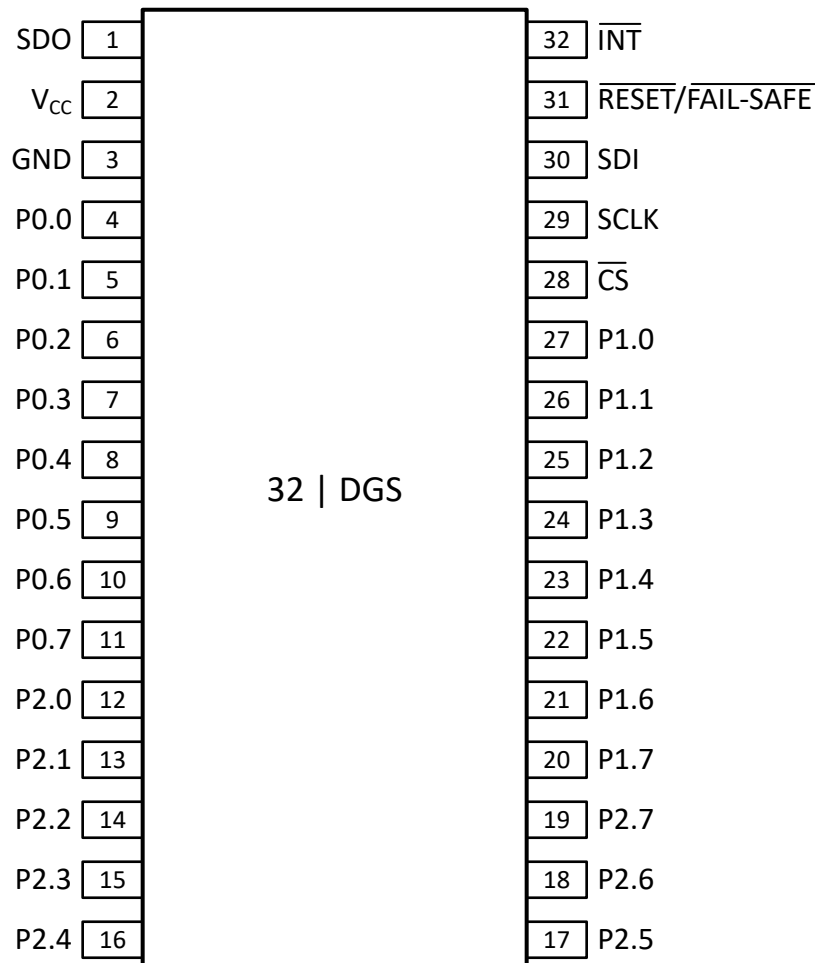


Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SDO	1	The push-pull SDO pin is stuck in a logic-low state. Damage to the p-channel FET potentially occurs due to high current draw when driving logic-high during communication.	A
VCC	2	The device is held in reset and all functionality of the pin is lost. All the Px.y pins become Hi-Z.	B
GND	3	There is no effect on the device. GND is the intended connection for this pin.	D
P0.0 – P0.7 P1.0 – P1.7 P2.0 – P2.7	4 – 27	If the pin is configured to be an output high, damage to the p-channel FET potentially occurs due to high current draw.	A
		If the pin is configured as an input or output low, functionality of the pin is lost.	B
\overline{CS}	28	Chip select is always in an active state, and SPI communication is not possible.	B
SCLK	29	The communication clock is stuck in a logic-low state, disabling the data shift register from the SDI pin and not allowing SDO data to be available to the controller.	B
SDI	30	The SDI pin is stuck in a logic-low state, which does not allow any data from the controller to be sent through the SPI to the device.	B
RESET/FAIL-SAFE	31	The device is held in reset, functionality of the pin is lost, and the Px.y pins remain Hi-Z inputs.	B
INT	32	The interrupt function is stuck low, and the functionality of the pin is lost.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SDO	1	The device cannot send SPI data to the SPI controller, and the functionality of the pin is lost.	B
VCC	2	The functionality of the pin is lost.	B
GND	3	The device is not biased to GND. There is damage to the device if GND floats high or low excessively.	A
P0.0 – P0.7 P1.0 – P1.7 P2.0 – P2.7	4 – 27	If the pin is configured to be an input, higher in-rush supply current potentially triggers the \overline{INT} pin due to a floating input.	B
		If the pin is configured as an output, there is no damage to device.	D
\overline{CS}	28	A floating \overline{CS} pin potentially makes SPI communication indeterminate, and the functionality of the pin is lost.	B
SCLK	29	A floating SCLK pin potentially makes SPI communicate indeterminate, disabling the data shift register from the SDI pin and not allowing SDO data to be available to the controller.	B
SDI	30	A floating SDI pin potentially causes incorrect data to be latched, and the functionality of the pin is lost.	B
RESET/FAIL-SAFE	31	A floating RESET pin potentially makes the device unresponsive or affects the programmed pin functions if the pin floats to logic-low.	B
\overline{INT}	32	The \overline{INT} pin can no longer assert low, and the controller cannot be notified of interrupts.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
SDO	1	VCC	The push-pull SDO pin is stuck in a logic-low state. Damage to the p-channel FET potentially occurs due to high current draw when driving logic-high during communication.	A
VCC	2	GND	The device is not powered, and all functionality of the pin is lost.	B
GND	3	P0.0	If the pin is configured as an input or output low, the functionality of the pin is lost.	B
			If the pin is configured to be an output high, damage to the p-channel FET potentially occurs due to high current draw.	A
P0.0	4	P0.1	If pins P0.0 and P0.1 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.0 and P0.1 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.0 and P0.1 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.0 and P0.1 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P0.1	5	P0.2	If pins P0.1 and P0.2 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.1 and P0.2 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.1 and P0.2 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.1 and P0.2 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P0.2	6	P0.3	If pins P0.2 and P0.3 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.2 and P0.3 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.2 and P0.3 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.2 and P0.3 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P0.3	7	P0.4	If pins P0.3 and P0.4 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.3 and P0.4 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.3 and P0.4 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.3 and P0.4 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
P0.4	8	P0.5	If pins P0.4 and P0.5 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.4 and P0.5 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.4 and P0.5 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.4 and P0.5 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P0.5	9	P0.6	If pins P0.5 and P0.6 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.5 and P0.6 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.5 and P0.6 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.5 and P0.6 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P0.6	10	P0.7	If pins P0.6 and P0.7 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.6 and P0.7 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.6 and P0.7 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.6 and P0.7 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P0.7	11	P2.0	If pins P0.7 and P2.0 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.7 and P2.0 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.7 and P2.0 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.7 and P2.0 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.0	12	P2.1	If pins P2.0 and P2.1 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.0 and P2.1 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.0 and P2.1 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.0 and P2.1 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
P2.1	13	P2.2	If pins P2.1 and P2.2 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.1 and P2.2 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.1 and P2.2 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.1 and P2.2 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.2	14	P2.3	If pins P2.2 and P2.3 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.2 and P2.3 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.2 and P2.3 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.2 and P2.3 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.3	15	P2.4	If pins P2.3 and P2.4 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.3 and P2.4 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.3 and P2.4 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.3 and P2.4 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.4	16	P2.5	If pins P2.4 and P2.5 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.4 and P2.5 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.4 and P2.5 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.4 and P2.5 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.5	17	P2.6	If pins P2.5 and P2.6 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.5 and P2.6 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.5 and P2.6 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.5 and P2.6 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
P2.6	18	P2.7	If pins P2.6 and P2.7 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.6 and P2.7 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.6 and P2.7 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.6 and P2.7 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.7	19	P1.7	If pins P2.7 and P1.7 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.7 and P1.7 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.7 and P1.7 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.7 and P1.7 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.7	20	P1.6	If pins P1.7 and P1.6 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.7 and P1.6 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.7 and P1.6 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.7 and P1.6 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.6	21	P1.5	If pins P1.6 and P1.5 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.6 and P1.5 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.6 and P1.5 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.6 and P1.5 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.5	22	P1.4	If pins P1.5 and P1.4 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.5 and P1.4 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.5 and P1.4 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.5 and P1.4 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
P1.4	23	P1.3	If pins P1.4 and P1.3 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.4 and P1.3 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.4 and P1.3 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.4 and P1.3 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.3	24	P1.2	If pins P1.3 and P1.2 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.3 and P1.2 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.3 and P1.2 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.3 and P1.2 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.2	25	P1.1	If pins P1.2 and P1.1 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.2 and P1.1 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.2 and P1.1 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.2 and P1.1 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.1	26	P1.0	If pins P1.1 and P1.0 are configured as outputs with opposite logic levels, then contention between the pins occur. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.1 and P1.0 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.1 and P1.0 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.1 and P1.0 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.0	27	\overline{CS}	If pin P1.0 is an input, false interrupts potentially occur when the \overline{CS} pin toggles.	C
			If pin P1.0 is as output, the \overline{CS} pin is potentially unusable and functionality is lost.	B
\overline{CS}	28	SCLK	The \overline{CS} pin toggles with the SCLK pin, SPI communication is not usable, and functionality is lost.	B
SCLK	29	SDI	SPI communication to the device is incorrect and functionality is lost.	B
SDI	30	$\overline{RESET/FAIL-SAFE}$	The device is reset when the SDI pin is logic low and functionality is lost.	B
$\overline{RESET/FAIL-SAFE}$	31	\overline{INT}	The device goes into RESET when an interrupt is triggered and functionality is lost	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SDO	1	The push-pull SDO pin is stuck in a logic-high state. Damage to the n-channel FET potentially occurs due to high current sink when driving logic-high during communication.	A
VCC	2	There is no effect on the device. This is the intended use of this pin.	D
GND	3	The device is unpowered and all functionality is lost.	B
P0.0 – P0.7 P1.0 – P1.7 P2.0 – P2.7	4 – 27	If the pin is configured as an input or output high, the functionality of the pin is lost.	B
		If the pin is configured to be an output low, damage to the n-channel FET potentially occurs due to high current sink.	A
\overline{CS}	28	The chip select pin is stuck in the logic-high state, SPI communication is not possible.	B
SCLK	29	The communication clock is stuck in a logic-high state, disabling the data shift register from the SDI pin and not allowing SDO data to be available to the controller.	B
SDI	30	The SDI pin is stuck in a logic-high state, not allowing for any data from the controller to be sent through the SPI to the device.	B
RESET / FAIL-SAFE	31	If the \overline{RESET} pin is tied to a pullup voltage, then higher leakage currents potentially occur.	C
		If the \overline{RESET} pin is tied to a pullup voltage, and an external circuit attempts to drive the \overline{RESET} , the device is not able to be reset through this hardware pin.	B
INT	32	If the \overline{INT} pin is asserted low, damage to the n-channel FET potentially occurs due to high current sink.	A

4.2 VQFN Package

This section provides a failure mode analysis (FMA) for the pins of the TXE8124. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-7](#))
- Pin open-circuited (see [Table 4-8](#))
- Pin short-circuited to an adjacent pin (see [Table 4-9](#))
- Pin short-circuited to VCC (see [Table 4-10](#))

[Table 4-7](#) through [Table 4-10](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-6](#).

Table 4-6. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Table 4-6](#) shows the TXE8124 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TXE8124 datasheet.

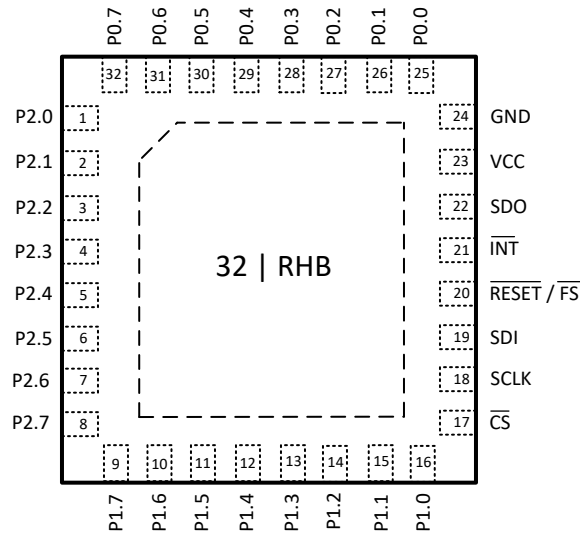


Figure 4-2. Pin Diagram

Table 4-7. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
P2.0 – P2.7 P1.0 – P1.7	1 – 16	If the pin is configured to be an output high, damage to the p-channel FET potentially occurs due to high current draw.	A
		If the pin is configured as an input or output low, functionality of the pin is lost.	B
\overline{CS}	17	Chip select is always in an active state and SPI communication is not possible.	B
SCLK	18	The communication clock is stuck in a logic-low state, disabling the data shift register from the SDI pin and not allowing SDO data to be available to the controller.	B
SDI	19	The SDI pin is stuck in a logic-low state, and does not allow for any data from the controller to be sent through the SPI to the device.	B
RESET / \overline{FS}	20	The device is held in reset, functionality of the pin is lost, and the Px.y pins remain Hi-Z inputs.	B
\overline{INT}	21	The interrupt function is stuck low and not able to indicate any interrupts including.	B
SDO	22	The push-pull SDO pin is stuck in a logic-low state. Damage to the p-channel FET potentially occurs due to high current draw when driving logic-high during communication.	A
VCC	23	The device is held in reset and all functionality is lost. All the Px.y pins become Hi-Z.	B
GND	24	There is no effect on the device. GND is the intended connection for this pin.	D
P0.0 – P0.7	25 – 32	If the pin is configured to be an output high, damage to the p-channel FET potentially occurs due to high current draw.	A
		If the pin is configured as an input or output low, functionality of the pin is lost.	B

Table 4-8. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
P2.0 – P2.7 P1.0 – P1.7	1 – 16	If the pin is configured to be an input, higher in-rush supply current potentially triggers INT due to a floating input.	B
		If the pin is configured as an output, there is no damage to the device.	D
\overline{CS}	17	A floating CS pin potentially makes SPI communication indeterminate and functionality of the pin is lost.	B
SCLK	18	A floating SCLK pin potentially makes SPI communicate indeterminate, disables the data shift register from the SDI pin, and does not allow SDO data to be available to the controller.	B
SDI	19	A floating SDI pin potentially causes the wrong data to get latched and functionality of the pin is lost.	B
RESET / \overline{FS}	20	A floating RESET pin potentially makes the device unresponsive, or affects the programmed pin functions, if the pin floats to logic-low.	B
\overline{INT}	21	The INT pin can no longer assert low, and the controller cannot be notified of interrupts.	B
SDO	22	The device cannot send SPI data to the SPI controller, and the functionality of the pin is lost.	B
VCC	23	The functionality of the pin is lost.	B
GND	24	The device is not biased to GND. There is damage to the device if GND floats excessively high or low.	A
P0.0 – P0.7	25 – 32	If the pin is configured to be an input, higher in-rush supply current potentially triggers INT due to a floating input.	B
		If the pin is configured as an output, there is no damage to the device.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
P2.0	1	P2.1	If pins P2.0 and P2.1 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.0 and P2.1 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.0 and P2.1 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.0 and P2.1 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.1	2	P2.2	If pins P2.1 and P2.2 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.1 and P2.2 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.1 and P2.2 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.1 and P2.2 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.2	3	P2.3	If pins P2.2 and P2.3 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.2 and P2.3 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.2 and P2.3 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.2 and P2.3 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.3	4	P2.4	If pins P2.2 and P2.3 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.3 and P2.4 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.3 and P2.4 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.3 and P2.4 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.4	5	P2.5	If pins P2.4 and P2.5 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.4 and P2.5 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.4 and P2.5 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.4 and P2.5 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C

Table 4-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
P2.5	6	P2.6	If pins P2.5 and P2.6 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.5 and P2.6 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.5 and P2.6 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.5 and P2.6 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.6	7	P2.7	If pins P2.6 and P2.7 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.6 and P2.7 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.6 and P2.7 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.6 and P2.7 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P2.7	8	P1.7	If pins P2.7 and P1.7 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P2.7 and P1.7 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P2.7 and P1.7 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P2.7 and P1.7 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.7	9	P1.6	If pins P1.7 and P1.6 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.7 and P1.6 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.7 and P1.6 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.7 and P1.6 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.6	10	P1.5	If pins P1.6 and P1.5 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.6 and P1.5 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.6 and P1.5 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.6 and P1.5 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C

Table 4-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
P1.5	11	P1.4	If pins P1.5 and P1.4 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.5 and P1.4 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.5 and P1.4 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.5 and P1.4 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.4	12	P1.3	If pins P1.4 and P1.3 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.4 and P1.3 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.4 and P1.3 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.4 and P1.3 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.3	13	P1.2	If pins P1.3 and P1.2 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.3 and P1.2 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.3 and P1.2 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.3 and P1.2 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.2	14	P1.1	If pins P1.2 and P1.1 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.2 and P1.1 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.2 and P1.1 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.2 and P1.1 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.1	15	P1.0	If pins P1.1 and P1.0 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I _{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P1.1 and P1.0 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P1.1 and P1.0 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P1.1 and P1.0 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P1.0	16	\overline{CS}	If pin P1.0 is an input, false interrupts potentially occur when the CS pin toggles.	C
			If pin P1.0 is as output, the CS pin is potentially unusable and functionality of the pin is lost.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
\overline{CS}	17	SCLK	The CS pin toggles with the SCLK pin, SPI communication is not usable, and functionality of the pin is lost.	B
SCLK	18	SDI	SPI communication to the device is incorrect and functionality of the pin is lost.	B
SDI	19	RESET / FS	The device is reset when the SDI pin is logic low and functionality is lost.	B
RESET / FS	20	INT	The device goes into RESET when an interrupt is triggered and functionality is lost.	B
INT	21	SDO	The SDO pin toggles INT and causes false interrupts to trigger.	B
SDO	22	VCC	The push-pull SDO pin is stuck in a logic-low state. Damage to the p-channel FET potentially occurs due to high current draw when driving logic-high during communication.	A
VCC	23	GND	The device is not powered and all functionality is lost.	B
GND	24	P0.0	If the pin is configured as an input or output low, functionality of the pin is lost.	B
			If the pin is configured to be an output high, damage to the p-channel FET potentially occurs due to high current draw.	A
P0.0	25	P0.1	If pins P0.0 and P0.1 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.0 and P0.1 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.0 and P0.1 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.0 and P0.1 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P0.1	26	P0.2	If pins P0.1 and P0.2 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.1 and P0.2 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.1 and P0.2 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.1 and P0.2 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P0.2	27	P0.3	If pins P0.2 and P0.3 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.2 and P0.3 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.2 and P0.3 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.2 and P0.3 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P0.3	28	P0.4	If pins P0.3 and P0.4 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.3 and P0.4 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.3 and P0.4 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.3 and P0.4 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C

Table 4-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
P0.4	29	P0.5	If pins P0.4 and P0.5 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.4 and P0.5 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.4 and P0.5 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.4 and P0.5 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P0.5	30	P0.6	If pins P0.5 and P0.6 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.5 and P0.6 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.5 and P0.6 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.5 and P0.6 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
P0.6	31	P0.7	If pins P0.6 and P0.7 are configured as outputs with opposite logic levels, then contention between the pins occurs. If the I_{OH} specification is exceeded, then damage to the device potentially occurs.	A
			If pins P0.6 and P0.7 are configured as outputs with the same logic level, then damage to the device does not occur.	D
			If pins P0.6 and P0.7 are configured so that one pin is an output and the other pin is an input, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C
			If pins P0.6 and P0.7 are configured as inputs, then no damage to the device is expected, but this configuration potentially leads to false interrupts.	C

Table 4-10. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
P2.0 – P2.7 P1.0 – P1.7	1 – 16	If the pin is configured as an input or output high, functionality of the pin is lost.	B
		If the pin is configured to be an output low, damage to the n-channel FET potentially occurs due to high current sink.	A
\overline{CS}	17	The chip select pin is stuck in the logic-high state, and SPI communication is not possible.	B
SCLK	18	The communication clock is stuck in a logic-high state, which disables the data shift register from the SDI pin, and does not allow SDO data to be available to the controller.	B
SDI	19	The SDI pin is stuck in a logic-high state, which does not allow for any data from the controller to be sent through the SPI to the device.	B
$\overline{RESET} / \overline{FS}$	20	If the \overline{RESET} pin is tied to a pullup voltage, then higher leakage currents potentially occur.	C
		If the \overline{RESET} pin is tied to a pullup voltage, and an external circuit attempts to drive RESET, the device is not able to be reset through this hardware pin.	B
\overline{INT}	21	If the \overline{INT} pin is asserted low, damage to the n-channel FET potentially occurs due to high current sink.	A
SDO	22	The push-pull SDO pin is stuck in a logic-high state. Damage to the n-channel FET potentially occurs due to high current sink when driving logic-high during communication.	A
VCC	23	There is no effect on the device. This is the intended use of this pin.	D
GND	24	The device is not powered and all functionality is lost.	B
P0.0 – P0.7	25 – 32	If the pin is configured as an input or output high, the functionality of the pin is lost.	B
		If the pin is configured to be an output low, damage to the n-channel FET potentially occurs due to high current sink.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2026	*	Initial Release

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Last updated 10/2025