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10-Bit Area CCD Analog Front-End Evaluation Module

Application Report

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10-Bit Area CCD Analog Front-End Evaluation Module

ABSTRACT

This application report describes the evaluation module (EVM) for Texas Instruments family of 10-bit, area CCD, analog front end (AFE) devices.

1 Feature Highlights

A list of the EVM features is illustrated with a schematic diagram. This EVM supports the following AFE devices.

- TLV977-10
- TLV986-10
- TLV987-10

The EVM provides a platform for the lab prototype evaluation of the family of 10-bit, area CCD, AFEs. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. The EVM uses standard SMA miniature RF connectors for the high-speed analog inputs and the outputs.

2 Power Supply Requirements

The EVM is designed to be powered by regulated lab power supplies. Three supplies are needed for powering the AFE under evaluation and the digital interface circuitry. One additional supply is required as the analog power for the onboard op amps. The specifications and the connectors used are as shown in Table 1:

Table 1. Power Supply Requirements

SUPPLY	CONNECTOR	USE
AVDD (3 V)	P2	Analog power
DVDD (3 V)	P3	Digital internal logic supply
DIVDD (2 – 4.4 V)	P4	Digital interface logic supply
5 V	P1	Analog supply to the op amps

The EVM has an additional DIVDD supply so the user can interface to different logic devices (having logic supplies in the range of 2 V to 4.4 V). The analog ground (AGND) and the digital ground (DGND/DIGND) are isolated from each other on the ground plane. Pads are provided so that the grounds can be tied together directly below the AFE IC or at the power supply inputs. This provides low-inductive ground connections for return current paths.

3 Analog Input

The analog input is provided through the SMA connector J1. This signal is routed to the DIN pin of the AFE by one of three paths.

- Direct input
- AC coupled input
- User supplied input
  - **Direct Input**
    To route the signal from the CCD directly to the DIN pin of the AFE, connect JP2. This provides a 50 Ω load (R11) at the input connector. A termination is required, since unterminated loads such as coaxial cables can provide reactive loads to the inputs.
  - **AC Coupled Input**
    If AC coupling is desired, JP1 needs to be connected (JP2 is open). In addition to the 50 Ω termination, this provides a series 0.1 μF capacitor for coupling AC inputs. This allows the CCD sensor to be directly connected to the J1 input.
  - **User Supplied Input Circuit**
    A breadboarding area allows the user to use custom input filters or other signal conditioning circuits. To route the signal from the breadboarding area, open Jumpers JP1 and JP2, and connect the requisite circuitry on the breadboard. This connects the DIN SMA to pin 1 of the AFE.

Only one of the above configurations can be used at any one time, to prevent excessive capacitance on the signal path, which could degrade the signal quality at high frequencies. JP3 needs to be connected to terminate the input at 50 Ω.

JP4 optionally connects DIN and PIN together or PIN to analog ground. Normally, PIN is connected to DIN.

4 Analog Outputs

The outputs of the PGA (TPP and TPM) and the outputs of the DAC's (DACO1, DACO2 and DACT) are provided as outputs through SMA and vertical pin connectors. These outputs are buffered through high-speed op amps, to provide proper driving capability at the output.

5 Digital Inputs/Outputs

Four buffers (U6–U9) drive input and output digital signals. Damping resistors of 22 Ω are in series to all high frequency inputs and outputs. Inputs are provided through the connector J7, and the ADC outputs and the 3-state enable are provided at the connector J11. For further information, refer to the Table 2 and the schematic.

The buffers U8 and U9 can be used as high-impedance by opening the jumper connection on JP8. To assist enabling the buffers from an external circuit, the connector J11 and JP8 are arranged so logic analyzer cable can be directly connected to both of them.

JP5 can be removed if external control on the STBY pin is required. The AFE can be reset using the pushbutton switch S1, which temporarily connects the RESET pin to the digital ground. Under normal operation, the RESET pin is connected to DVDD.

6 Clock Circuit

Two external clocks are required for proper operation of the EVM. One of the clocks (ADCCLK) provides the input to the internal ADC. The other (SCLK) synchronizes the serial data transfer. These clock sources are provided through the SMA J8 for ADCCLK, and through pin 16 of connector J7 for SCLK. The SMA is terminated at 50 Ω. Noninverting drivers buffer both clocks. The ADCCLK also has a series termination to prevent spikes and instability at higher frequencies.

7 Test Points

Test point TP1 monitors the input signal. TP7 checks the signals on ADCCLK (pin 1), $\overline{SR}$ (pin 2) and $\overline{SV}$ (pin 3). Other test points not labeled are for the user to connect a probe to the reference ground or the supply voltages.

8 Breadboarding Areas

Two separate breadboarding areas (analog and digital) are provided for user supplied input/output circuitry. These allow the user to condition the response as desired for any particular application.

9 Summary

The EVM provides the user ease in evaluating the TI AFE devices. Inputs and outputs are provided through simple ribbon connectors, making it easy to connect to any logic analyzer. The programming capabilities and speed of these devices can thus be easily evaluated using the EVM.

10 Pin Connection Definitions

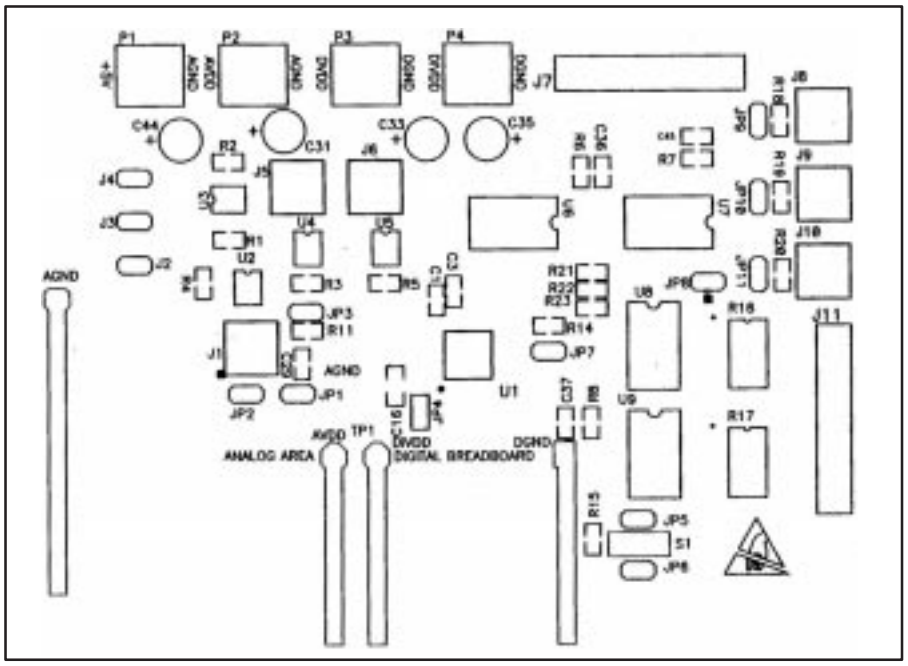
Table 2. Connector Pin Out

Connectors	Description
J1	Analog signal input from CCD
J2	Buffered DACT output
J3	Buffered DACO1 output
J4	Buffered DACO2 output
J5	Buffered TPM output (PGA noninverting output or inverted PGA clock)
J6	Buffered TPP output (PGA inverting output or inverted CDS clock)
J7	Connector for digital inputs. All odd numbered pins connected to digital ground. **PIN** **FUNCTION** **PIN** **FUNCTION** 2 $\overline{\text{CLAMP}}$ 14 SDIN 4 $\overline{\text{BLKG}}$ 16 SCLK 6 $\overline{\text{OBCLP}}$ 18 ADCCLK (opt) 8 $\overline{\text{STBY}}$ 20 $\overline{\text{SR}}$ (opt) 10 $\overline{\text{RESET}}$ 22 $\overline{\text{SV}}$ (opt) 12 $\overline{\text{CS}}$
J8	ADCCLK input (JP9 needs to be open)
J9	SRB input (JP10 needs to be open)
J10	SVB input (JP11 needs to be open)
J11	Output connector for ADC outputs **PIN** **FUNCTION** **PIN** **FUNCTION** 2 D9 12 D4 4 D8 14 D3 6 D7 16 D2 8 D6 18 D1 10 D5 20 D0 All odd numbered pins are connected to digital ground.

Table 3. Jumper Layout

JUMPERS	DESCRIPTION
JP1	Capacitively couple analog signal input from CCD through J1
JP2	Directly couple analog signal input through J1
JP3	Connect 50 Ω termination to the analog input signal
JP4	Optionally connect DIN and PIN together, or PIN to analog ground
JP5	Put the AFE in $\overline{\text{STBY}}$ mode (connect $\overline{\text{STBY}}$ to ground)
JP7	Enable AFE by pulling $\overline{\text{OE}}$ to ground
JP8	Enable the buffers U8 and U9
JP9	Allows ADCCLK to take its input from connector J7
JP10	Allows $\overline{\text{SR}}$ to take its input from connector J7
JP11	Allows $\overline{\text{SV}}$ to take its input from connector J7

11 EVM Component Location Diagram

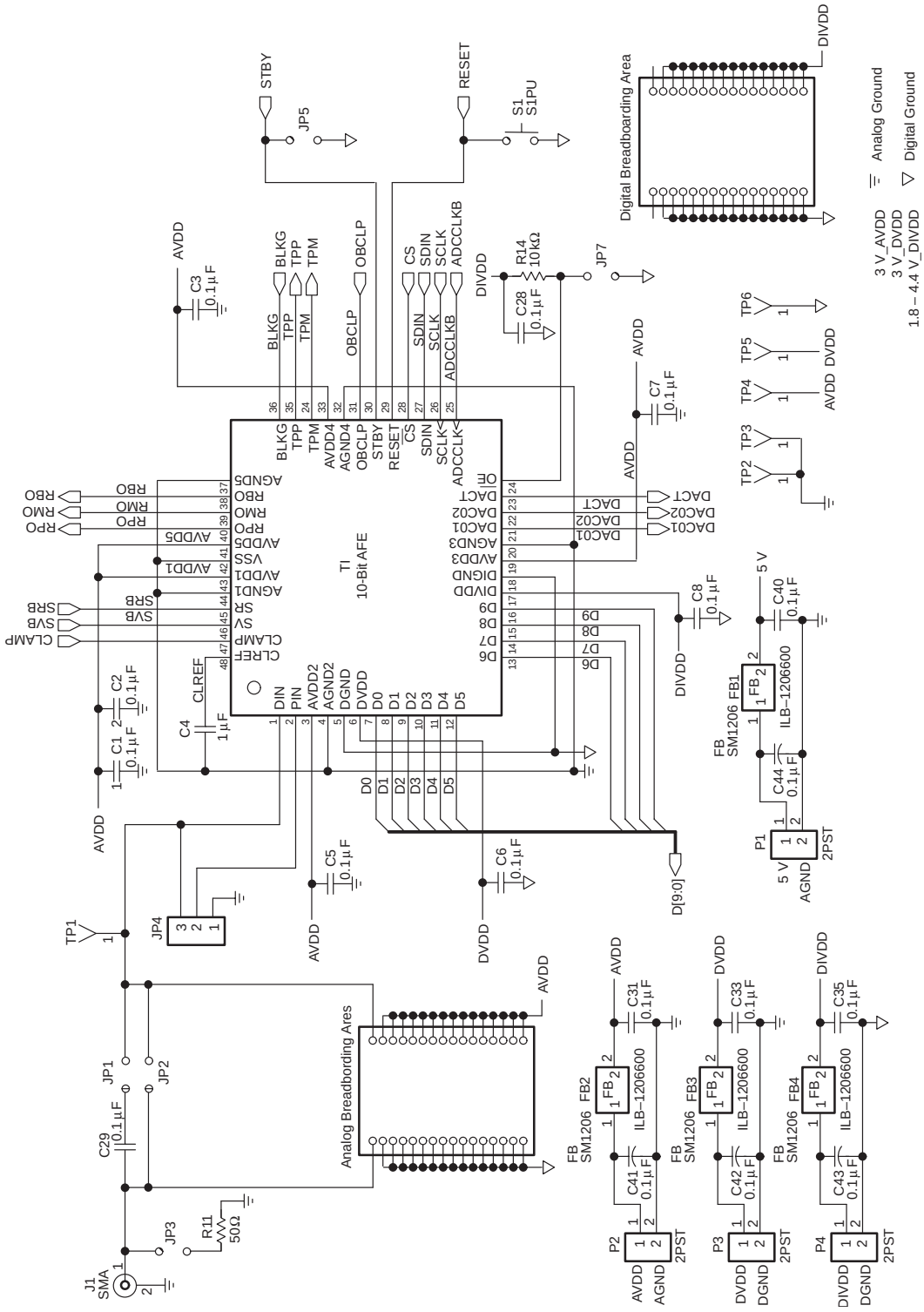


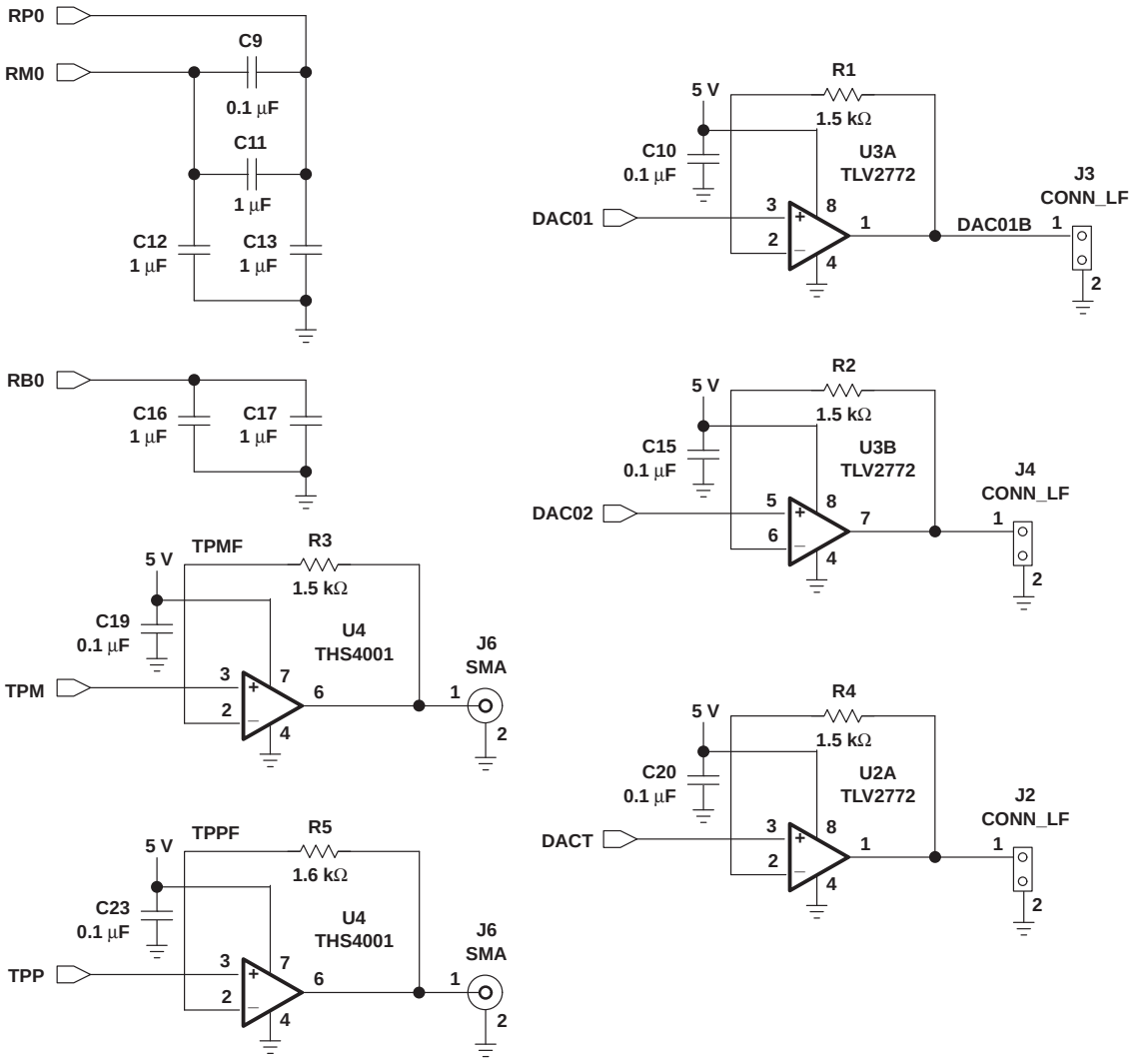
BOARD LAYOUT

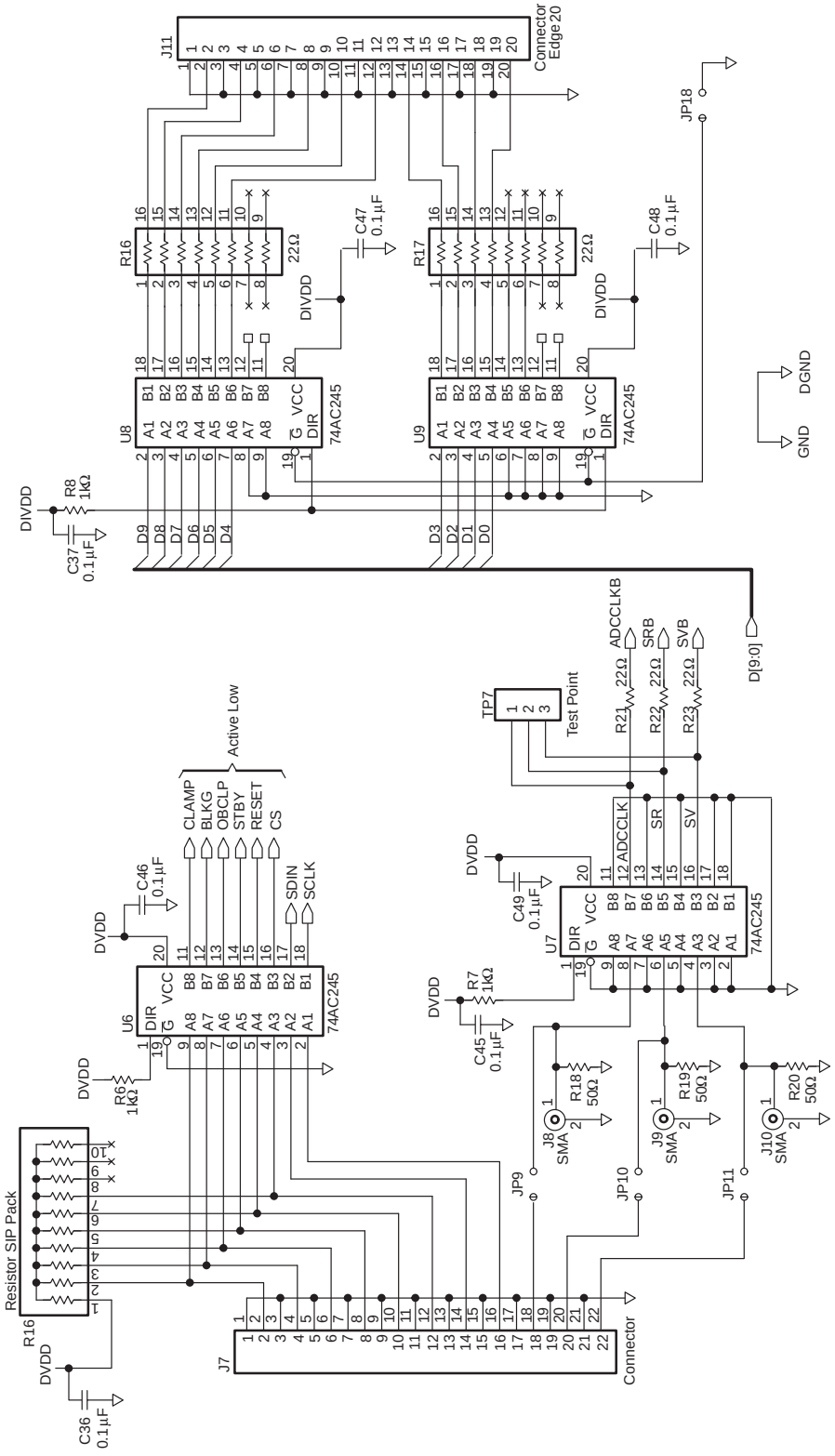
12 EVM Bill of Materials

ITEM	QTY.	REFERENCE	PART	PCB FOOTPRINT
1	27	C1, C2, C3, C5, C6, C7, C8, C9, C10, C15, C17, C19, C20, C23, C28, C29, C36, C37, C40, C41, C42, C43, C45, C46, C47, C48, C49	0.1 µ	0805
2	5	C4, C11, C12, C13, C16	1 µ	1206
3	4	C31, C33, C35, C44	0.1 µ	CAP100RP
4	4	FB1, FB2, FB3, FB4	ILB-1206600	1206
5	9	JP1, JP2, JP3, JP5, JP7, JP8, JP9, JP10, JP11	JUMPER	JUMPER
6	1	JP4	CONNECTOR EDGE3	JUMPER
7	6	J1, J5, J6, J8, J9, J10	SMA	SMA
8	3	J2, J3, J4	CONN_LF	Jumper type connectors
9	1	J7	CONNECTOR	HDR2X11
10	14	J11	CONNECTOR EDGE20	HDR2X10
11	5	P1,P2,P3,P4	2PST	PWRCON2
12	3	R1,R2,R3,R4,R5	1.5K	0805
13	4	R6,R7,R8	1K	0805
14	4	R11,R18,R19,R20	50	0805
15	1	R14	10K	0805
16	1	R15	RES_SIP_PACK	RES10SIPB
17	2	R16,R17	22	4816P
18	3	R21,R22,R23	22	0805
19	1	S1	S1PU	SWITVH
20	1	TP1	TP	TP
21	2	TP3,TP2	AGND	TP
22	1	TP4	AVDD	TP
23	1	TP5	DVDD	TP
24	1	TP6	DGND	TP
25	1	TP7	TEST POINT	HDR1X3
26	1	U1	TLV9xxCPFB	QFP48 (device under evaluation)
27	2	U3, U2	TLV2772	TLV2772
28	2	U4, U5	THS4001	THS4001
29	3	U6, U7, U8	74AC245	74AC245
30	1	U9	74AHC245	74AC245
31	1	U10	Analog breadboarding area	
32	1	U11	Digital breadboarding area	

13 EVM Board Schematic




RP0
RM0
C9
0.1 µF
C11
1 µF
C12
1 µF
C13
1 µF
RB0
C16
1 µF
C17
1 µF
5 V
TPMF
R3
1.5 kΩ
C19
0.1 µF
U4
THS4001
TPM
J6
SMA
TPPF
R5
1.6 kΩ
C23
0.1 µF
TPP
R1
C10
0.1 µF
U3A
TLV2772
DAC01
J3
CONN_LF
DAC01B
R2
C15
0.1 µF
U3B
TLV2772
DAC02
J4
CONN_LF
R4
C20
0.1 µF
U2A
TLV2772
DACT
J2
CONN_LF


J11
Connector Edge20
R16
22Ω
R17
22Ω
C47
0.1µF
C48
0.1µF
DIVDD
JP18
U8
U9
74AC245
VCC
DIR
R8
1kΩ
C37
0.1µF
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
D[9:0]
DGND
GND
ADCCLKB
SRB
SVB
R21
R22
R23
TP7
Test Point
DVDD
C49
0.1µF
U7
ADCCLK
SR
SV
R7
1kΩ
C45
0.1µF
R18
50Ω
R19
50Ω
R20
50Ω
J8
J9
J10
SMA
JP9
JP10
JP11
C46
0.1µF
U6
R6
1kΩ
Active Low
CLAMP
BLKG
OBCLP
STBY
RESET
CS
SDIN
SCLK
Resistor SIP Pack
R16
J7
Connector
C36
0.1µF