Application Report
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# Upgrading From ADS7808/09 to ADS8508/09 Devices

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**ABSTRACT**

The information contained in this document applies to current applications using the ADS7808 or ADS7809 in a surface-mount SOIC (DW) package. This document is a guide to users of the ADS7808/09 devices with regards to potential compatibility issues when upgrading to the new ADS8508 and ADS8509 series of devices.

## 1 Package and Pin Compatibility

The ADS8508 and ADS8509 were designed to be fully pin-compatible with the surface-mount SO-20 (DW package) versions of the ADS7808 and ADS7809 devices. The updated chips feature greater throughput (up to 250 ksps), lower power, and better ac and dc performance

The following table is hyperlinked to provide easy access to the associated data sheets of both the ADS78xx and ADS85xx devices.

| Current ADS78xx Family | New ADS85xx Family |
|---|---|
| ADS7808 – SBAS018 | ADS8508 – SLAS433 |
| ADS7809 – SBAS017 | ADS8509 – SLAS324 |

## 2 Electrical Compatibility

The following section describes potential electrical compatibility issues.

### *2.1 Absolute MAX Voltage Input Changes*

The new ADS8508 and ADS8509 devices differ in the maximum working voltage. These items are presented in Table 1.

**Table 1. ADS8508 and ADS8509 Maximum Working Voltage**

| **ADS78xx MAX Voltage Specification** | |
|---|---|
| $V_{ANA}$ | 7 V |
| $V_{DIG}$ | 7 V |
| **ADS85xx MAX Voltage Specification** | |
| $V_{ANA}$ | 6 V |
| $V_{DIG}$ | 6 V |

### 2.2 Input Impedance and Capacitance Changes

The new ADS85xx devices have different input impedance and capacitance features as well. The major differences are noted in Table 2.

**Table 2. ADS85xx Input Impedances and Capacitances**

| PARAMETER | CONDITIONS | 78 SERIES | | | 85 SERIES | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ADSxx08** | | | | | | | | |
| Impedance | ±10-V Range | | 22.9 | | | 11.5 | | kΩ |
| | ±5-V Range | | 13.3 | | | 6.7 | | kΩ |
| | ±3.3-V Range | | 10.7 | | | 5.4 | | kΩ |
| | 0-V to 10-V Range | | 13.3 | | | 6.7 | | kΩ |
| | 0-V to 5-V Range | | 10.0 | | | 5.0 | | kΩ |
| | 0-V to 4-V Range | | 10.7 | | | 5.4 | | kΩ |
| Capacitance | | | 35 | | | 45 | | pF |
| **ADSxx09** | | | | | | | | |
| Impedance | ±10-V Range | | 22.9 | | | 11.5 | | kΩ |
| | ±5-V Range | | 13.3 | | | 6.7 | | kΩ |
| | ±3.3-V Range | | 10.7 | | | 5.4 | | kΩ |
| | 0-V to 10-V Range | | 13.3 | | | 6.7 | | kΩ |
| | 0-V to 5-V Range | | 10.0 | | | 5.0 | | kΩ |
| | 0-V to 4-V Range | | 10.7 | | | 5.4 | | kΩ |
| Capacitance | | | 35 | | | 45 | | pF |

### 2.3 Performance Compatibility

The new ADS8508 and ADS8509 devices have performance characteristics that meet or exceed the B-grade specifications listed in the ADS7808 and ADS7809 device data sheets. Primary interest regarding specific improvements depend on the actual application. In ac applications for example, the spurious-free dynamic range (SFDR) has improvements of up to 16 dB (typical).

For applications where dc performance is critical, integral nonlinearity (INL) and differential nonlinearity (DNL) have been improved by nearly 50%.

## 3 Functional and Timing Differences

The following sections discuss the functionality and timing differences between the ADS7808/09 and the ADS8508/09.

### 3.1 Functional Compatibility

The ADS8508 and ADS8509 devices retain the same basic functionality of the ADS7808 and ADS7809.

### 3.2 Timing Compatibility

The timing changes related to the ADS8508 and ADS8509 devices are discussed in detail throughout the following section. Depending on the specific application, these timing changes can affect the drop in replacement or ease of use in designs or end systems currently using the ADS7808 or ADS7809. A careful review of Table 3 and Table 4 highlights the timing differences between the ADS7808/09 and ADS8508/09.

## 3.3 Comparison of the ADS7808 and ADS8508 Timing Characteristics

The **bold** items inTable 3 show the affected timing parameters associated with the ADS7808 and ADS8508 device.

**Table 3. ADS7808 and ADS8508 Timing Parameters**

| SYMBOL | DESCRIPTION | ADS7808 | | | ADS8508 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| ADS7808 / ADS8508 | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **t1 / $t_{w1}$** | **Convert Pulse Width** | **40** | | **4500** | **40** | | | ns |
| **t2 / $t_{d1}$** | **BUSY Delay** | | | **65** | | **6** | **20** | ns |
| **t3 / $t_{w2}$** | **BUSY LOW** | | | **8** | | | **2.2** | µs |
| **t4 / $t_{d2}$** | **BUSY Delay after End of Conversion** | | **220** | | | **5** | | ns |
| **t5 / $t_{d3}$** | **Aperture Delay** | | **40** | | | **5** | | ns |
| **t6 / $t_{conv}$** | **Conversion Time** | | **5.7** | **8** | | | **2.2** | µs |
| t7 / $t_{acq}$ | Acquisition Time | | | 2 | 1.8 | | | µs |
| **t6 +t7 / $t_{conv}$ + $t_{acq}$** | **Throughput Time** | | **9** | **10** | | | **4** | µs |
| t8 / $t_{d4}$ | R/C LOW to DATACLK Delay | | 450 | | | 270 | | ns |
| **t9 / $t_{c1}$** | **DATACLK Period** | | **440** | | | **110** | | ns |
| **t10 / $t_{d5}$** | **Data Valid to DATACLK HIGH Delay** | **20** | **75** | | **15** | **35** | | ns |
| **t11 / $t_{d6}$** | **Data Valid to DATACLK LOW Delay** | **100** | **125** | | **20** | **35** | | ns |
| **t12 / $t_{c2}$** | **External DATACLK Period** | **100** | | | **35** | | | ns |
| t13 / $t_{w3}$ | External DATACLK HIGH | 20 | | | 15 | | | ns |
| t14 / $t_{w4}$ | External DATACLK LOW | 30 | | | 15 | | | ns |
| t15 / $t_{su1}$ | DATACLK HIGH Setup Time | 20 | | t12 + 5 | 15 | | $t_{c2}$ + 5 | ns |
| t16 / $t_{su2}$ | R/C to CS Setup Time | 10 | | | 10 | | | ns |
| t17 / $t_{d7}$ | SYNC Delay after DATACLK HIGH | 15 | | 35 | 3 | | 35 | ns |
| t18 / $t_{d8}$ | Data Valid Delay | 25 | | 55 | 2 | | 20 | ns |
| t19 / $t_{d9}$ | CS to Rising Edge Delay | 25 | | | 10 | | | ns |
| **t20 / $t_{d10}$** | **Data Available after CS LOW** | **4.5** | | | **2** | | | µs |

## 3.4 Comparison of the ADS7809 and ADS8509 Timing Characteristics

The **bold** items in Table 4 show the affected timing parameters associated with the ADS7809 and ADS8509 device.

**Table 4. ADS7809 and ADS8509 Timing Characteristics**

| SYMBOL | DESCRIPTION | ADS7809 | | | ADS8509 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| ADS7809 / ADS8509 | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **t1 / $t_{w1}$** | **Convert Pulse Width** | **40** | | **4500** | **40** | | | ns |
| **t2 / $t_{d1}$** | **BUSY Delay** | | | **65** | | **6** | **20** | ns |
| **t3 / $t_{w2}$** | **BUSY LOW** | | | **8** | | | **2.2** | µs |
| **t4 / $t_{d2}$** | **BUSY Delay after End of Conversion** | | **220** | | | **5** | | ns |
| **t5 / $t_{d3}$** | **Aperture Delay** | | **40** | | | **5** | | ns |
| **t6 / $t_{conv}$** | **Conversion Time** | | **5.7** | **8** | | | **2.2** | µs |
| t7 / $t_{acq}$ | Acquisition Time | | | 2 | 1.8 | | | µs |
| t6 +t7 / $t_{conv}$ + $t_{acq}$ | Throughput Time | | 9 | 10 | | | 4 | µs |

**Table 4. ADS7809 and ADS8509 Timing Characteristics (continued)**

| SYMBOL | DESCRIPTION | ADS7809 | | | ADS8509 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| ADS7809 / ADS8509 | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t8 / $t_{d4}$ | R/C LOW to DATACLK Delay | | 450 | | | 270 | | ns |
| **t9 / $t_{c1}$** | **DATACLK Period** | | **440** | | | **110** | | ns |
| **t10 / $t_{d5}$** | **Data Valid to DATACLK HIGH Delay** | **20** | **75** | | **15** | **35** | | ns |
| **t11 / $t_{d6}$** | **Data Valid to DATACLK LOW Delay** | **100** | **125** | | **20** | **35** | | ns |
| **t12 / $t_{c2}$** | **External DATACLK Period** | **100** | | | **35** | | | ns |
| t13 / $t_{w3}$ | External DATACLK HIGH | 20 | | | 15 | | | ns |
| t14 / $t_{w4}$ | External DATACLK LOW | 30 | | | 15 | | | ns |
| t15 / $t_{su1}$ | DATACLK HIGH Setup Time | 20 | | t12 + 5 | 15 | | | ns |
| t16 / $t_{su2}$ | R/C to CS Setup Time | 10 | | | 10 | | | ns |
| t17 / $t_{d7}$ | SYNC Delay after DATACLK HIGH | 15 | | 35 | 3 | | 35 | ns |
| t18 / $t_{d8}$ | Data Valid Delay | 25 | | 55 | 2 | | 20 | ns |
| t19 / $t_{d9}$ | CS to Rising Edge Delay | 25 | | | 10 | | | ns |
| **t20 / $t_{d10}$** | **Data Available after CS LOW** | **4.5** | | | **2** | | | µs |

# 4 Potential Application Issues

## *4.1 When Using Internal Serial Clock*

Customers using the internal SCLK function must ensure that their host processor is capable of handling the increased serial clock speed. The ADS85xx devices output a serial clock on the order of 9 MHz; the ADS78xx provide a serial clock of approximately 2 MHz. The increased conversion clock speed also means that the BUSY signal returns to its active-high state much faster - 8 µs with the ADS78xx devices, versus 2.2 µs with the ADS85xx devices. Processors that use the BUSY output to signal an interrupt service routine may need to add delays to the system in order to accommodate the speed increase.

## *4.2 When Using External Serial Clock*

Customers using the ADS7808/09 serial interface parts with an external DATA clock may need to modify their software depending on the application of the R/C input. Customers using an external DATA clock must ensure that the R/C is released before attempting to read data. If the BUSY signal is used to trigger an SPI interrupt/transfer routine, the host processor must be prepared to handle the higher data rate of the ADS85xx device.

As noted in the timing tables of section 3, the BUSY signal returns high nearly four times faster in the ADS85xx. If the R/C input is longer than 2.2 µs, BUSY could go active-high before the R/C input is released. If the serial clock is started while R/C is low, output data can be missed and or improperly received because the output data is high-z while R/C is low.

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