Application Note

How to Improve the Efficiency of TAS58xx Audio Amplifier

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ABSTRACT

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Class-D digital audio amplifiers are widely used in the audio field due to their high efficiency, small form factor, and cost-effective performance. For portable speakers, battery life is a critical metric. However, legacy Class-D audio amplifiers have some efficiency limitations, such as efficiency losses from switching loss and conduction loss, as well as audio signal distortion. This article briefly introduces two methods to improve the efficiency of TI's TAS58xx audio amplifiers through system-level designs. One method is to use the digital Class-H mode to implement PVDD audio envelope tracking, which reduces efficiency losses from switching loss and conduction loss. The other method is to provide higher-efficiency external power supplies to GVDD and AVDD. The audio amplifier's GVDD rail powers the internal drive circuitry, while the AVDD rail powers the internal analog circuitry. Typically, these rails are supplied by internally integrated LDOs, which are less efficient. By supplying high-efficiency external power, the efficiency can be improved.

TI's mainstream consumer mid-power audio amplifiers, including the TAS58xx family (TAS5825, TAS5827, TAS5828, and TAS5830) and the SN0058xx family, as well as mainstream automotive audio amplifiers like the TAS6584 and TAS6582, can all achieve significant efficiency improvements using these two methods. Meanwhile, the low-power audio amplifiers like the TAS257x and TAS278x families all support Class-H mode.

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1 Power Architecture of a Class-D Digital Audio Amplifier and Its Loss Breakdown

To improve the efficiency of a Class-D digital audio amplifier, it is first necessary to understand its power architecture and power loss breakdown. Taking the TAS58xx as an example, a TAS58xx audio amplifier normally requires only two power supplies: DVDD and PVDD.

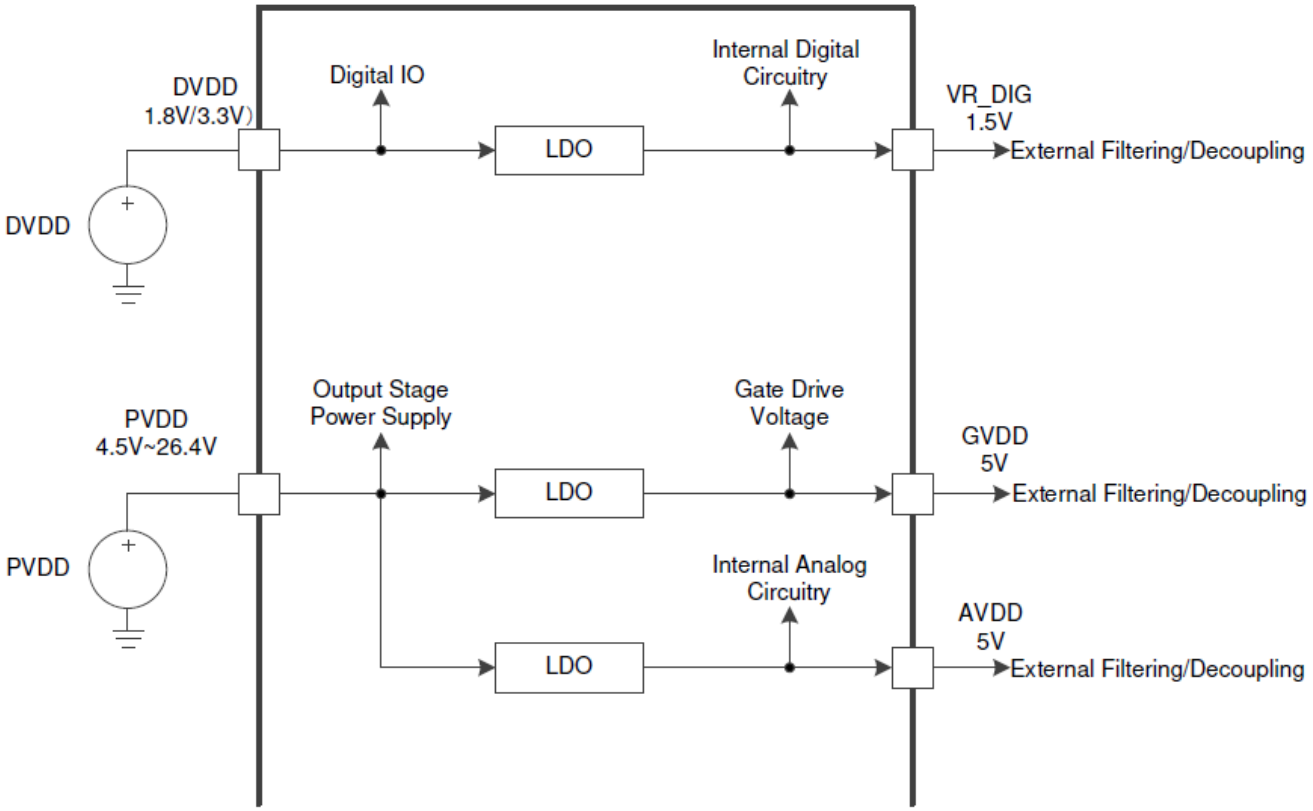

Figure 1-1. TAS58xx Power Architecture

DVDD is generally 1.8V or 3.3V, typically draws around 22mA, and supplies the internal digital circuitry of the digital input audio amplifier, such as the digital IO, and also provides power to digital circuits like the DSP core after being converted to VR_DIG (1.5V) by an LDO. Common analog input Class-D audio amplifiers, such as the TPA3128D2, do not have digital circuitry and therefore do not have the DVDD supply. The most significant loss of the DVDD supply comes from the low efficiency of the LDO step-down and the power consumption of the DSP during operation. The amount of DSP power dissipation is closely related to the DSP architecture, semiconductor process, operating modes such as operating frequency, signal sampling rate, DSP processing flow, and so forth. To optimize this power dissipation, these aspects can be considered. This article focuses solely on an in-depth study of PVDD power optimization.

The PVDD supply ranges from 4.5V to 26.4V, and its quiescent current consumption typically ranges from 20mA to 100mA, depending on the voltage and operating mode. It supplies the audio amplifier's power output stage, as well as the analog circuitry (AVDD) and drive circuitry (GVDD) after being stepped down by an LDO. PVDD losses mainly include conduction loss, switching loss, GVDD drive loss, AVDD analog circuitry loss, dead time loss, and LC filter circuitry loss.

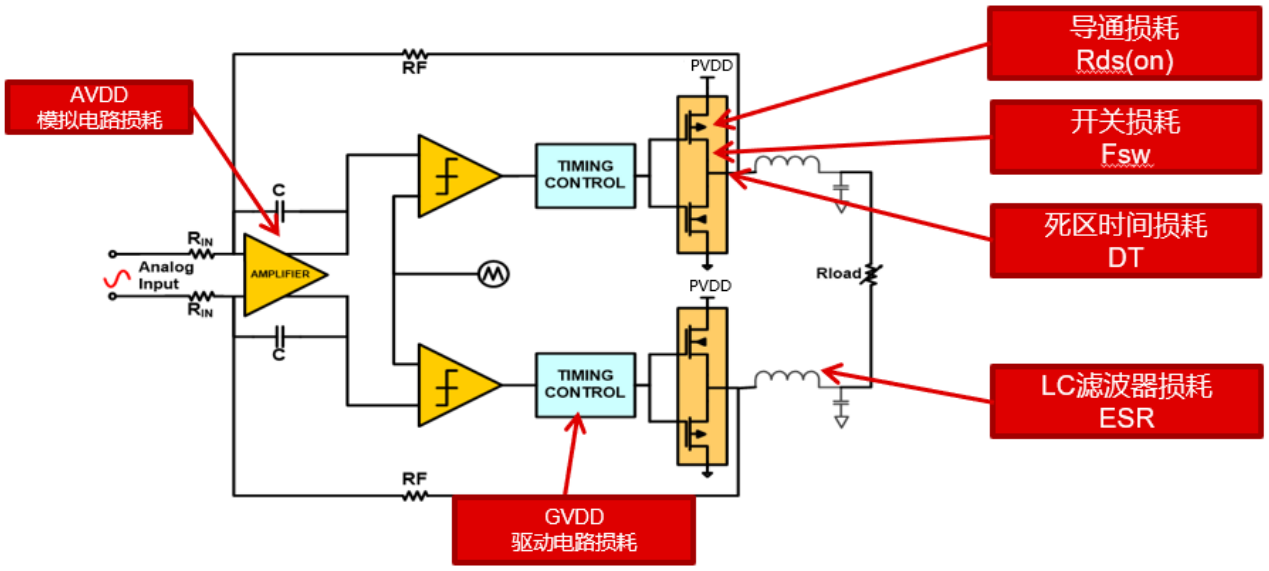

Figure 1-2. Loss Breakdown of PVDD

Conduction loss is caused by the impedance Rds(on) of MOSFETs during conduction. During conduction, both the high-side and low-side MOSFETs are turned on. This impedance forms a voltage divider with the speaker (load), resulting in power dissipation and heat generation, as shown in Equation 1 below. Conduction loss increases when Rds(on) and PVDD voltage are higher. As the output power increases, the PVDD voltage becomes greater, and the conduction current also rises. Consequently, the loss caused by the conduction impedance becomes larger. Therefore, the conduction loss dominates at high-power output.

$$P_{cond} = I^2 \times R = 2 \times \left\{ \frac{V_{pvdd}}{2R_{ds(on)} + R_L} \right\}^2 \times \left(2R_{ds(on)} \right) \quad (1)$$

Switching loss is caused by the non-ideal states of MOSFETs during turn-on and turn-off transitions. Because it takes a certain period of time for MOSFETs to fully turn on or off, power is dissipated during this process. A full-bridge audio amplifier has four MOSFETs, and the switching loss is given by Equation 2. As the equation shows, the switching loss is proportional to the switching frequency, PVDD voltage, and output current.

$$P_{sw} = 2 \times V_{pvdd} \times I_{out} \times \left(t_{swon} + t_{swoff} \right) \times f_{sw} \quad (2)$$

Drive loss is the power dissipated to drive MOSFETs on and off. It is related to the drive voltage, the MOSFET's Q_g parameter, and the switching frequency. The drive voltage is obtained from PVDD through an LDO step-down and a bootstrap circuit. The LDO efficiency is $\eta = V_{gvdd} \div V_{pvdd}$. The drive loss is given by Equation 3 below, which shows that the higher the PVDD voltage, the lower the LDO efficiency, and the greater the drive loss.

$$P_{gd} = 4 \times Q_g \times V_{pvdd} \times \eta \times f_{sw} \quad (3)$$

Dead time loss occurs during the dead time. Because the turn-off and turn-on of the high-side and low-side transistors require a certain amount of time, a specific dead time delay is added to avoid shoot-through, where the high-side and low-side transistors are simultaneously turned on. The dead time is related to audio performance metrics and shoot-through current, and it is generally not adjustable by users in integrated audio amplifiers. The dead time loss is given by Equation 4, which shows that the dead time loss is also proportional to the PVDD voltage.

$$P_{DT} = 4 \times V_F \times I_{out} \times t_{DT} \times f_{sw} = 4 \times V_F \times \left(\frac{V_{pvdd}}{2R_{ds(on)} + R_L} \right) \times t_{DT} \times f_{sw} \quad (4)$$

The LC filter loss mainly comes from the inductor's impedance loss, especially the DCR loss. As given by $P_{L(DCR)} = 2 \times \left(\frac{V_{pvdd}}{2R_{ds(on)} + R_L}\right)^2 \times DCR$, this type of loss is also proportional to the PVDD voltage.

Conduction loss dominates at high-power output, while switching loss and drive loss dominate at low-power output. These losses add up to the total loss that affects the operating efficiency of an audio amplifier. They must be optimized during the design phase based on real-world application conditions. Parameters such as f_{sw}, Q_g, $R_{ds(on)}$, and t_{DT} have a significant impact on losses. However, they are generally less likely to be adjustable in integrated audio amplifiers. For example, the switching frequency f_{sw} of the TAS58xx can only be selected from 384kHz, 480kHz, 576kHz, and 768kHz, and parameters such as Q_g, $R_{ds(on)}$, and t_{DT} are not adjustable by users. How to optimize efficiency then? Here are two effective methods to reduce losses and optimize audio amplifier efficiency.

2 Improving Audio Amplifier Efficiency with Class-H Mode

2.1 How Class-H Mode Improves Efficiency

A typical portable speaker consists of a lithium battery, a boost converter, an audio amplifier, and so forth. The main power supply (PVDD) of the audio amplifier is provided by the lithium battery, with the voltage stepped up by the boost converter. The signal source to be amplified by the audio amplifier is music, which usually features a wide dynamic range. An appropriate amplitude of PVDD helps prevent clipping distortion of music peaks. For most smaller-amplitude signals in music, however, a fixed PVDD voltage is a waste of energy: It can be found from the equations above that the audio amplifier generates higher losses when operating at a higher PVDD voltage, and the boost converter also has a lower efficiency in this case. As a result, the system efficiency is lower than that at a relatively low PVDD voltage.

The boost converter's efficiency is also low when it outputs a relatively high step-up voltage, and the ratio of output to input voltages is large. As shown in Figure 2-1 below, taking the efficiency data from the specifications for the TPS61288, TI's mainstream boost converter, as an example: Under the same conditions of VIN = 3.6V and IOUT = 0.1A, the efficiency at VOUT = 5.5V is about 3% higher than the efficiency at VOUT = 13V.

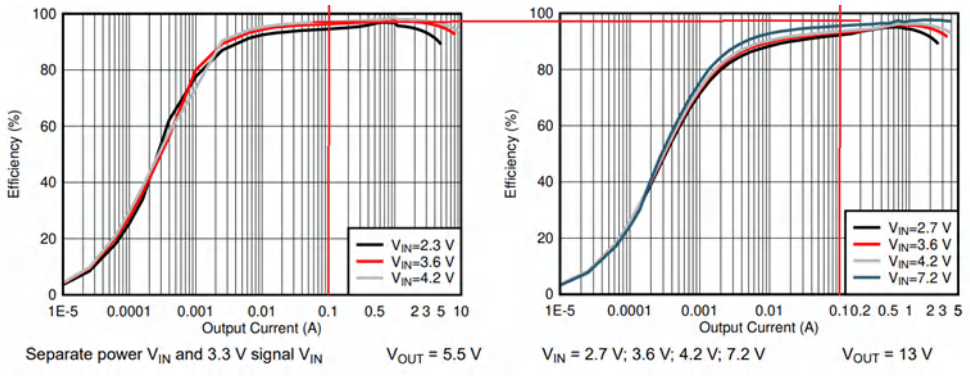

Figure 2-1. TPS61288 VOUT = 5.5V Efficiency vs VOUT = 13V Efficiency

Similarly, audio amplifiers also have lower efficiency at a higher PVDD voltage. As shown in Figure 2-2 below, taking the efficiency data from the specifications for the TAS5825P, TI's mainstream audio amplifier, as an example: Under the same output power (for example, 10W), the efficiency at PVDD = 12V shows a significant difference, being nearly 10% higher than the efficiency at PVDD = 24V.

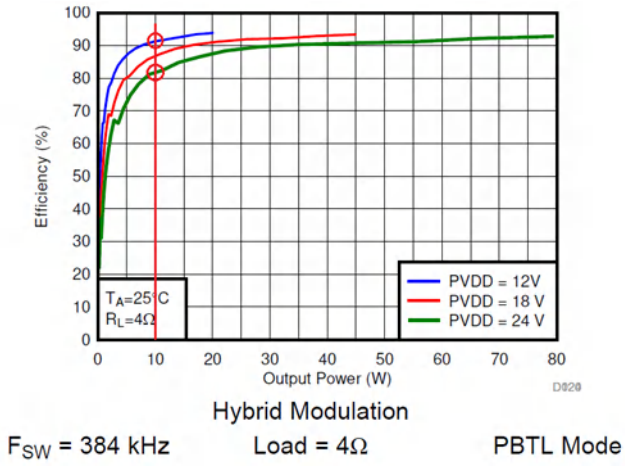

Figure 2-2. TAS5825P Efficiency vs PVDD

Therefore, if the PVDD voltage dynamically follows the music waveform dynamics to achieve envelope tracking, it will be possible to improve efficiency for both the boost converter and the audio amplifier. Figure 2-3 shows that the PVDD voltage changes with the amplitude variations of the music waveform:

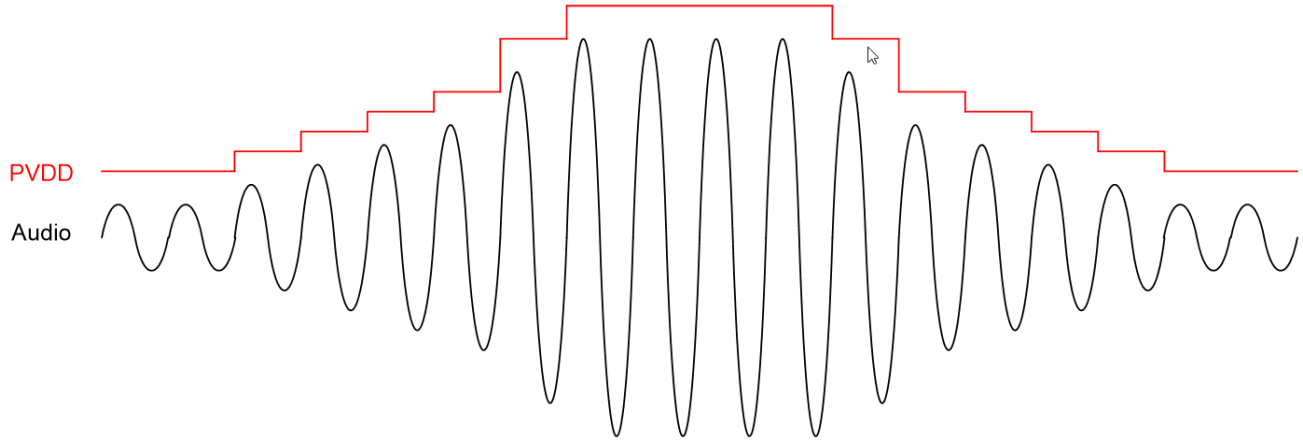

Figure 2-3. PVDD Music Envelope Tracking

2.2 TI's Digital Class-H Innovation

In legacy envelope tracking circuits, such as the reference design in TIDA-050024 shown in Figure 2-3, an analog op amp is used to sample the music waveform at the audio amplifier output. After shaping and filtering, the PVDD voltage is adjusted by the boost converter. However, the PVDD voltage tracking lags behind the music waveform, resulting in severe clipping distortion. In addition, complex analog op-amp circuits are required, leading to high circuit complexity and BOM cost.

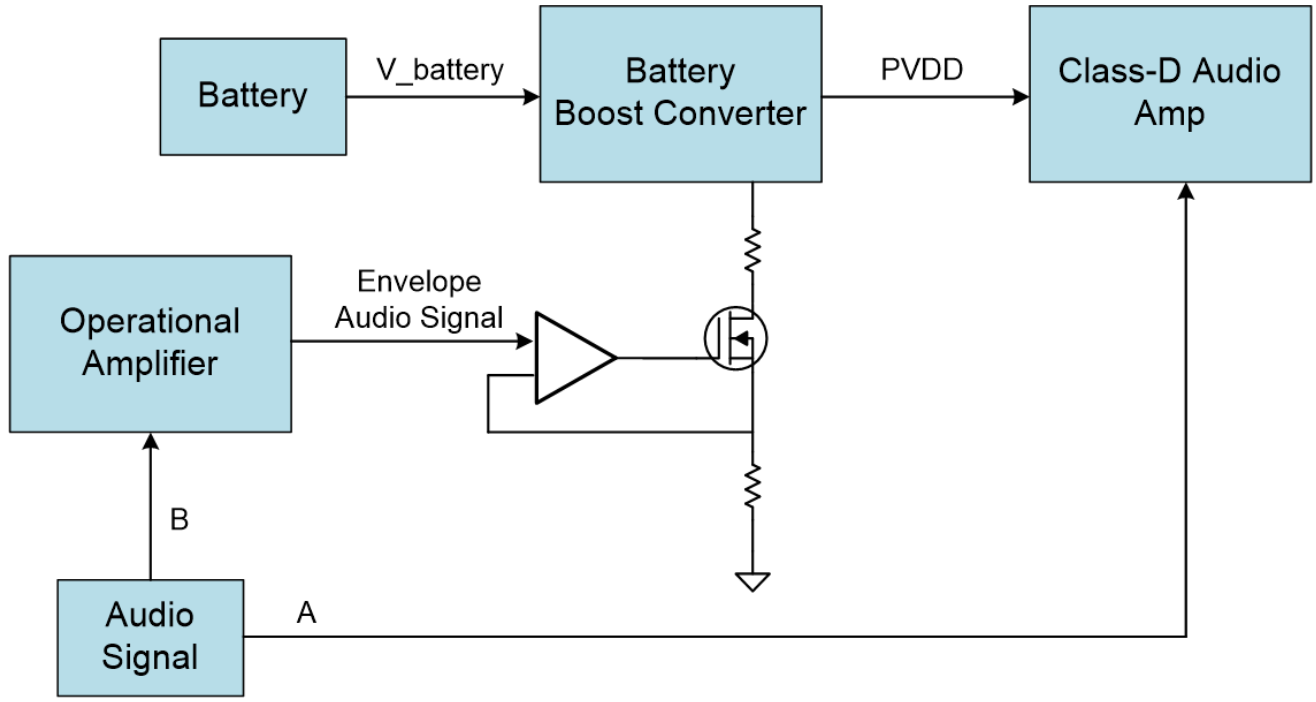

Figure 2-4. Diagram of a Music Envelope Tracking Simulation Scheme

TI's innovative Hybrid-Pro algorithm for PVDD music envelope tracking is integrated into the audio amplifier's DSP. The TAS5825P is the first audio amplifier solution to innovatively use digital Hybrid-Pro, also commonly referred to as Class-H. This algorithm controls the output voltage of the boost circuitry by providing easily controlled PWM feedback. In addition, with the delay between the music waveform and the Class-H waveform, it provides advance control of the PVDD voltage, which enables accurate adjustment of the PVDD voltage before music peaks arrive, perfectly preventing clipping distortion of the music waveform.

The amount of delay between the music peak output and the PVDD adjustment control is mainly affected by two factors. One is the delay length that the customer can accept, which is determined by the customer's product type. For example, in some Partybox products, a microphone input is present. The total delay of the entire link from the microphone input to the audio amplifier output is typically required to be less than 5ms. In this case, the audio amplifier delay must be as small as possible, so that listeners cannot perceive a delay between the original voice and the sound output from the speaker. The other consideration is that the time delay must be greater than the time required for PVDD to rise to its target level, so as to avoid clipping distortion. In this case, the main influencing factors include the boost converter's loop reaction time, the output capacitance, and the current power with load. Given so many factors, debugging must be done based on real-world conditions. To debug the Class-H mode, TI provides easy-to-use PurePath™ - Console 3 (PPC3) software.

The Class-H mode is implemented on the TAS5825P as shown in Figure 2-5 below. The music signal enters the audio amplifier's DSP and is split into two processing paths. In the first path, the music signal is processed by the Class-H algorithm, which calculates the signal level and outputs a PWM feedback signal with varying duty cycles related to the music amplitude. This feedback signal is then filtered by a second-order RC low-pass filter (LPF) and fed to the FB (feedback) control pin of the boost converter, adjusting the PVDD output voltage to the level just sufficient to prevent music clipping, thereby minimizing the power consumption. In the other path, the music signal waits in the DSP for an adjustable delay before being output from the amplifier until the PVDD voltage is adjusted to the required level.

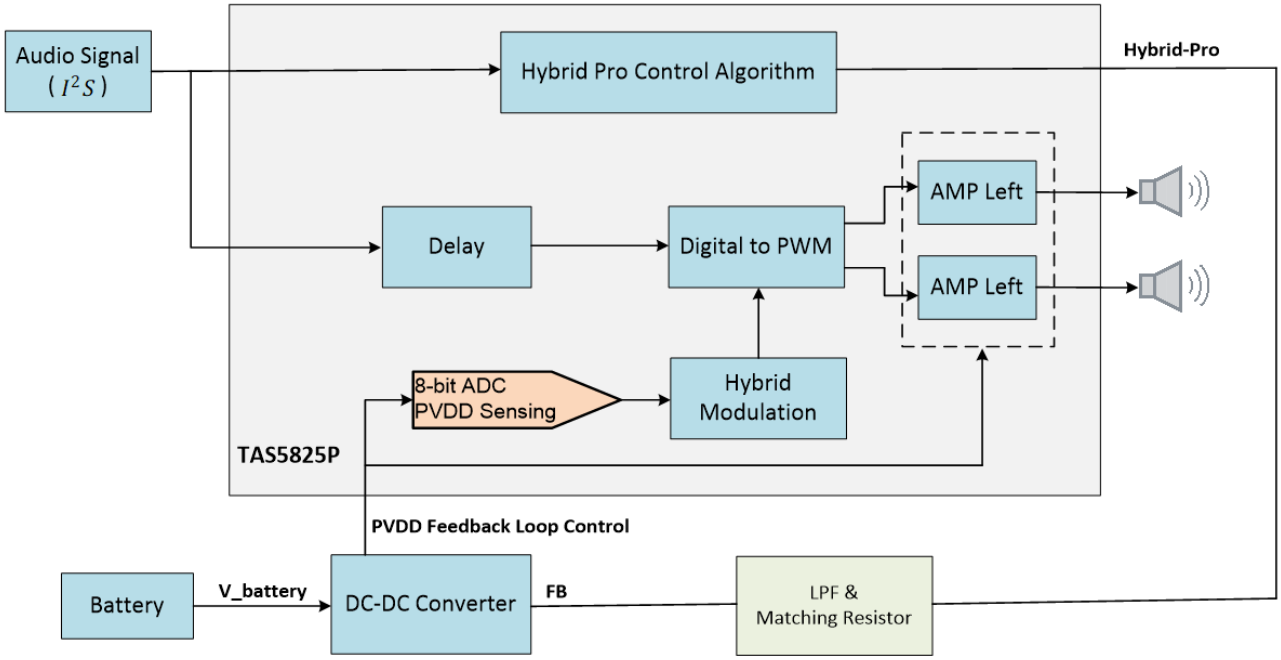

Figure 2-5. Diagram of a Music Envelope Tracking Simulation Scheme

The PPC3 Class-H mode debugging interface is shown in Figure 2-6 below. This GUI tool makes it easy to set the PVDD voltage range, calculate the feedback resistor parameters of the boost converter, and calculate the RC filter parameters.

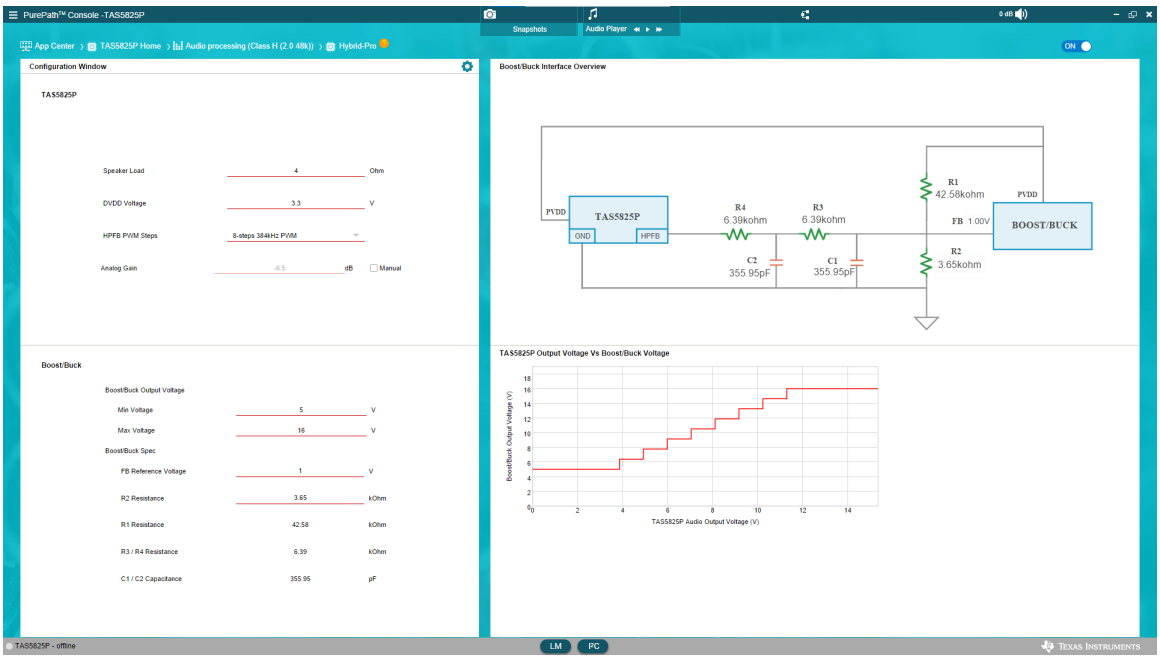

Figure 2-6. TAS5825P PPC3 Tool Class-H Mode Debugging Window

As shown in Figure 2-7, the efficiency data from the TAS5825P specifications shows that a significant improvement in audio amplifier efficiency is achieved by using the Class-H mode: The blue line shows up to a 15% improvement in efficiency when the Hybrid-pro (Class-H) mode is enabled.

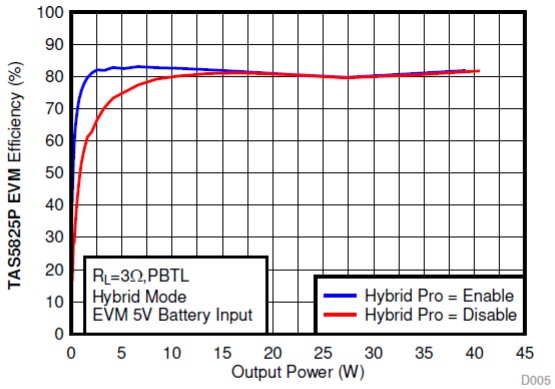

Figure 2-7. EVM Hybrid On and Off Efficiency Comparison

3 Improving Efficiency With External GVDD and AVDD and Considerations

The internal power architecture of the TAS5825P is shown in Figure 3-1 below. GVDD and AVDD are 5V power rails that supply the audio amplifier's internal analog and drive circuitry. They are derived from PVDD after an LDO step-down. When the PVDD voltage is high (for example, PVDD = 26V), a simple calculation shows that the efficiency of this supply is low to about 19.2%.

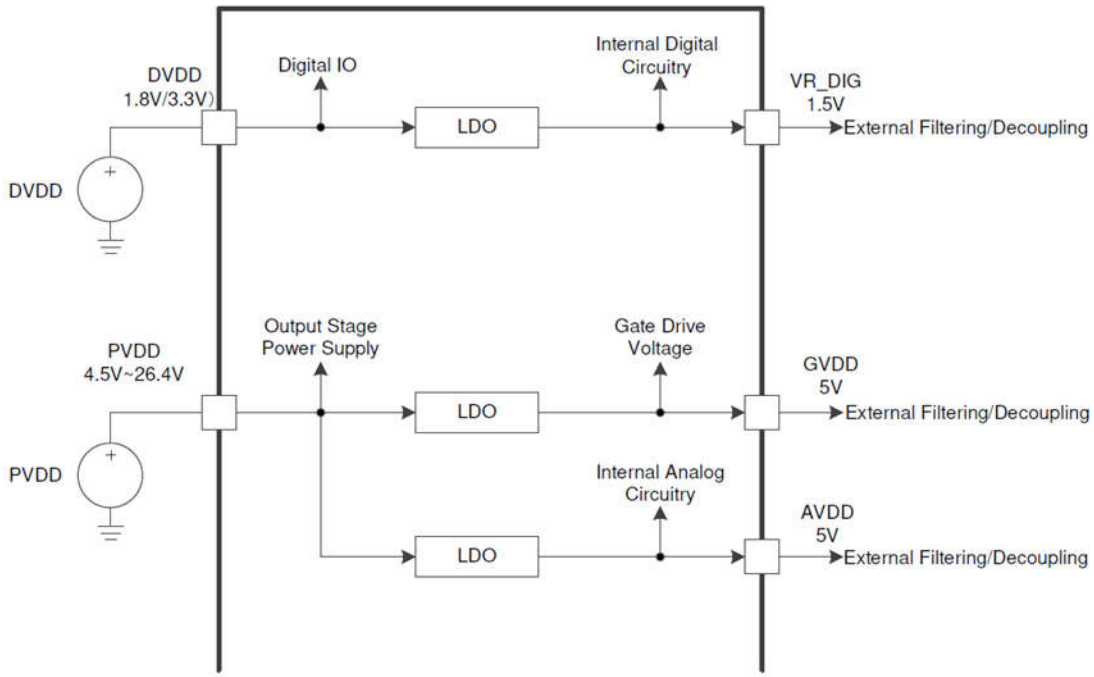

Figure 3-1. TAS5825P Internal Power Architecture

So, if an external high-efficiency DC/DC converter is used to supply GVDD and AVDD, there will be a significant increase in efficiency and a reduction in the audio amplifier's power consumption. TI's TAS5825, TAS5827, TAS5828, and TAS5830 audio amplifiers all support the option of external GVDD and AVDD.

3.1 Testing Power Saving from External GVDD and AVDD and Testing the Impact on Audio Metrics

Figure 3-2 below presents the data of static power saving from external GVDD and AVDD. As the PVDD voltage rises, the power saving becomes more significant. At PVDD = 26V, external GVDD and AVDD can save approximately 431mW of power.

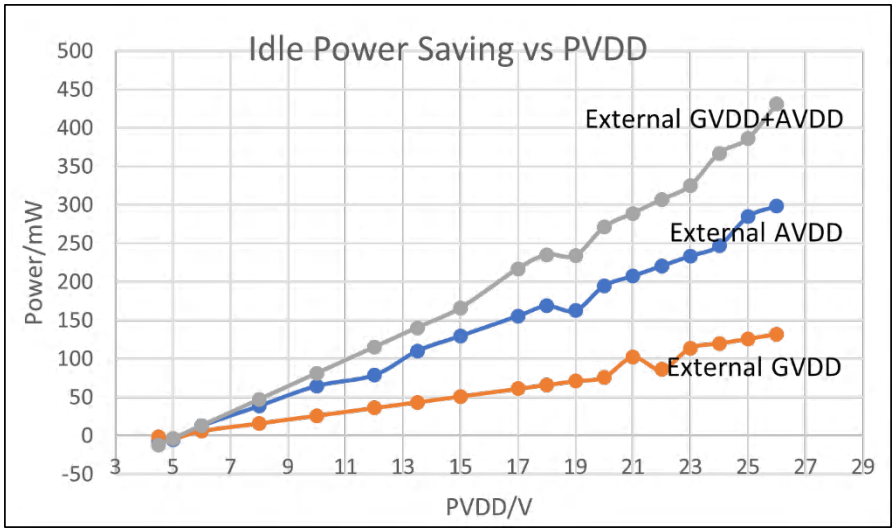

Figure 3-2. image11_TAS5825P External GVDD/AVDD Idle Power Saving vs PVDD

Test Condition: Idle status, 384kHz, Hybrid mode, 10uH+0.68uF filter, external GVDD/AVDD 5.1V.

Table 3-1 compares the efficiency with load. It shows efficiency improvements under both light and heavy loads, with more significant improvements under light loads. In portable speakers, which operate at low power for most of the time, this approach provides a significant efficiency improvement.

Table 3-1. External GVDD/AVDD Efficiency vs Internal AVDD/GVDD Efficiency

Efficiency	Internal GVDD/AVDD	External 5.1 V to AVDD/GVDD
2 * 0.5W	59.400%	63.873%
2 * 1W	68.876%	71.690%
2 * 5W	83.333%	84.817%
2 * 10W	85.910%	86.421%
2 * 20W	86.955%	87.856%

The following Figure 3-3 and Figure 3-4 show that testing the audio amplifier's THD metrics reveals that the external GVDD and AVDD have no impact on audio amplifier performance.

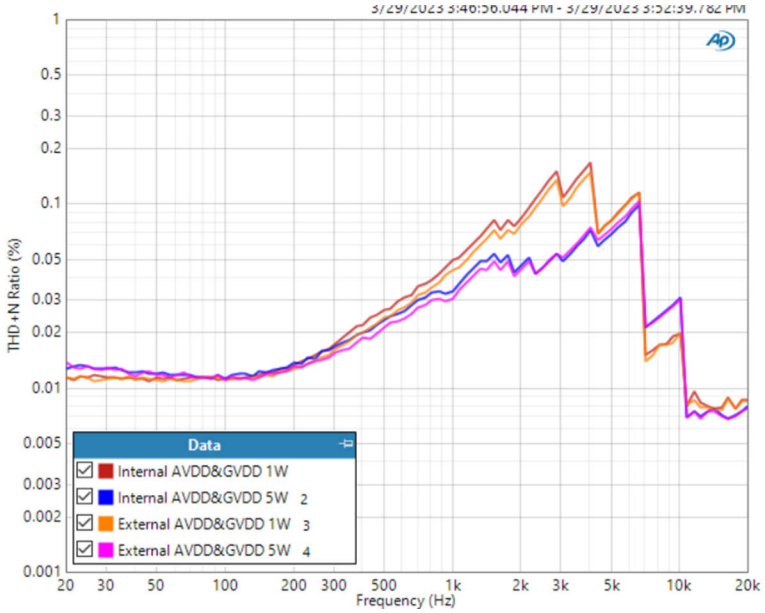

Figure 3-3. image12_THD vs Frequency

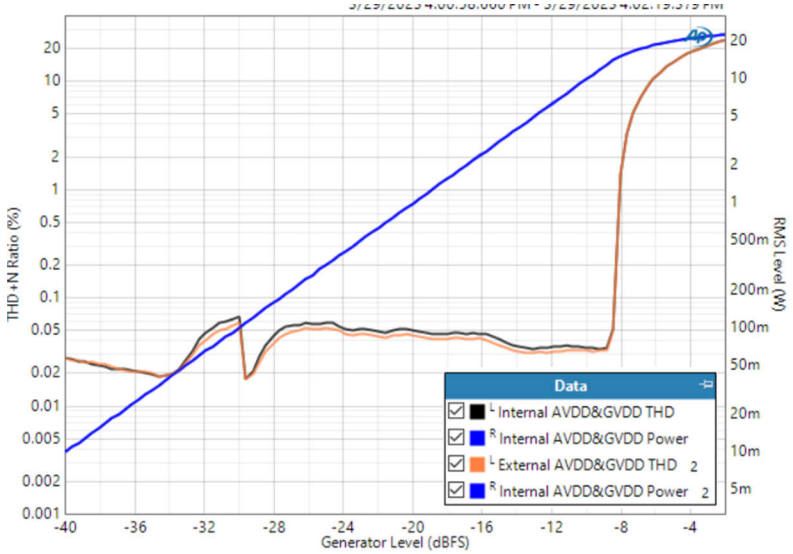

Figure 3-4. image13_THD vs Output Power

3.2 Considerations for External GVDD and AVDD:

3.2.1 Voltage Range of External GVDD and AVDD:

The TAS58xx does not have the option to turn off the internal LDO. Therefore, it must be ensured that the minimum external voltage is higher than the audio amplifier's internal LDO output voltage when external supplies are provided. In this case, the internal LDO output will be cut off, and the internal circuitry will be powered by the external voltage. The internal circuitry uses whichever voltage is higher: the external voltage or the internal LDO voltage, posing no particular risks. It is generally recommended that the external supply voltage does not exceed 5.5V.

In particular, note that the power-up and power-down sequences for external supplies must meet TI's requirements; otherwise, unexpected issues may arise due to electrical leakage. TI's recommended sequences are provided below. There have been issues in other customers' applications where AVDD leakage interfered with OTP Memory due to non-compliance with TI's specified sequences.

- The TAS5825P has a customized part number, SN005825P. It has been calibrated for GVDD and AVDD voltages before shipment, and its maximum internal LDO output voltage will not exceed 5.0V. Therefore, it is only necessary to ensure that the external voltage ranges from 5.0V to 5.5V.
- The TAS5827, TAS5828, and TAS5830 can reduce the internal LDO output voltage center value to 4.3V by adding software code, which also ensures that the internal output voltage will not exceed 5.0V. Therefore, it is only necessary to ensure that the external voltage ranges from 5.0V to 5.5V.

The code for TAS5827, TAS5828, and TAS5830 to modify the internal LDO output voltage to 4.3V is as follows:

```
w c0 00 00
w c0 7f 00
w c0 00 00 # enter book0 page0
w c0 7d 11
w c0 7e ff
w c0 00 02 # enter page2
r c0 08 01 # read the value of register 0x08
w c0 08 xx #only change bit7 of register 0x08, other bit remains no change.
# for example, the default value of register 0x08 is 0x0f (00001111), then should write 0x8f to
register 0x08 (10001111).
w c0 00 00 # enter page0
w c0 7f 00
w c0 7d 00
w c0 7e 00 #exit engineer mode
```

3.2.2 Sequence Requirements for External GVDD and AVDD:

Always follow the power-up and power-down sequences specified by TI for GVDD and AVDD to be supplied externally:

- SN005825P sequences for external GVDD and AVDD:
  - Audio amplifier startup sequence:
    1. Turn on PVDD and DVDD
    2. When power supplies are stable, pull up PDN and start supplying I2S.
    3. After the I2S clock is stable, start writing the audio amplifier configuration via I2C.
    4. Start the external GVDD/AVDD supply after the audio amplifier configuration is complete

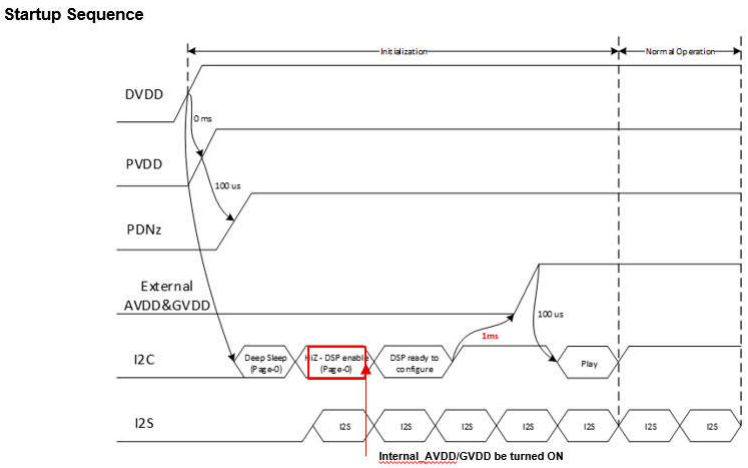

Figure 3-5. SN005825P Startup Sequence for External GVDD/AVDD

  - Key considerations:
    1. After the audio amplifier enters HIZ, internal GVDD and AVDD will be turned on.
    2. After internal GVDD and AVDD are turned on, external GVDD and AVDD can be turned on after a 1ms delay
    3. External GVDD and AVDD supplies are turned on only after PVDD power-up and PDN has been pulled high.
  - Audio amplifier power-down sequence:
    1. Use the I2C command to let the audio amplifier enter HIZ
    2. Delay at least 6ms (48kHz) for digital volume ramp down
    3. Turn off external GVDD and AVDD supplies
    4. Turn off PVDD and DVDD

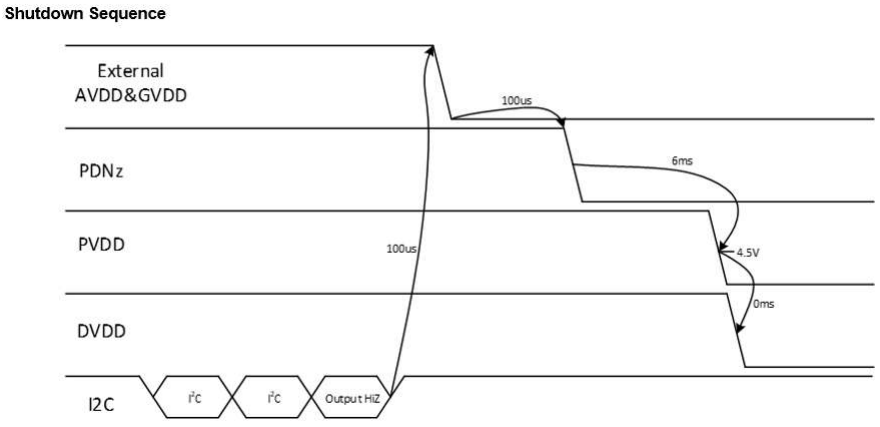

Figure 3-6. SN005825P Power-Down Sequence for External GVDD/AVDD

Key consideration: External GVDD and AVDD must be turned off before PDN is pulled low.

- TAS5827/TAS5828/TAS5830 Sequence Requirements for External GVDD and AVDD:
  - Startup sequence (Figure 3-7):
    1. Bring up power supplies (PVDD, DVDD)
    2. Once power supplies are stable, bring up PDN.
    3. Configure I2C initialization. 4.3V code insert to 'DSP ready to configure' section
    4. Provide external power rail to AVDD/GVDD
    5. Complete I2C initialization.
    6. No special requirement for I2S sequence, but suggest to provide stable clock before enter play.
    7. Enter play mode.

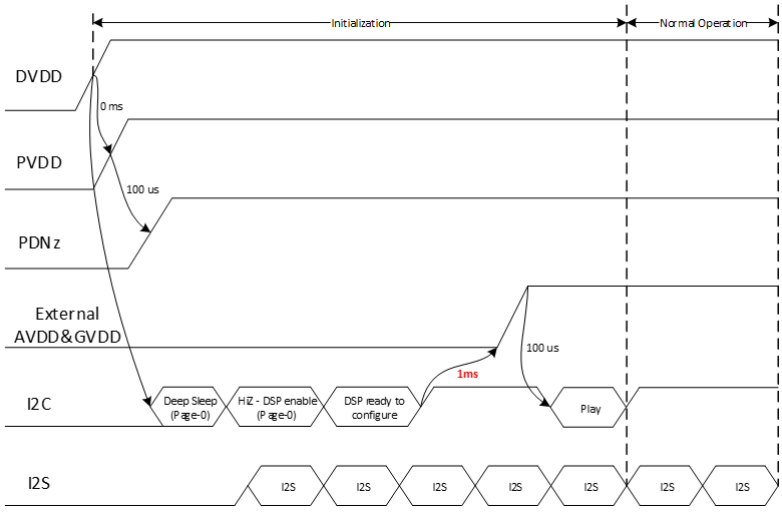

Figure 3-7. TAS5828/TAS5827 Power-up Sequence for External GVDD/AVDD

  - Power-down sequence (Figure 3-8):
    1. I2C command let AMP enter HIZ.
    2. Turn off external GVDD & AVDD supply.
    3. I2C command enter deep sleep or pull PDN down
    4. Delay at least 6ms (48kHz) for volume ramp down.
    5. Turn off PVDD and then DVDD

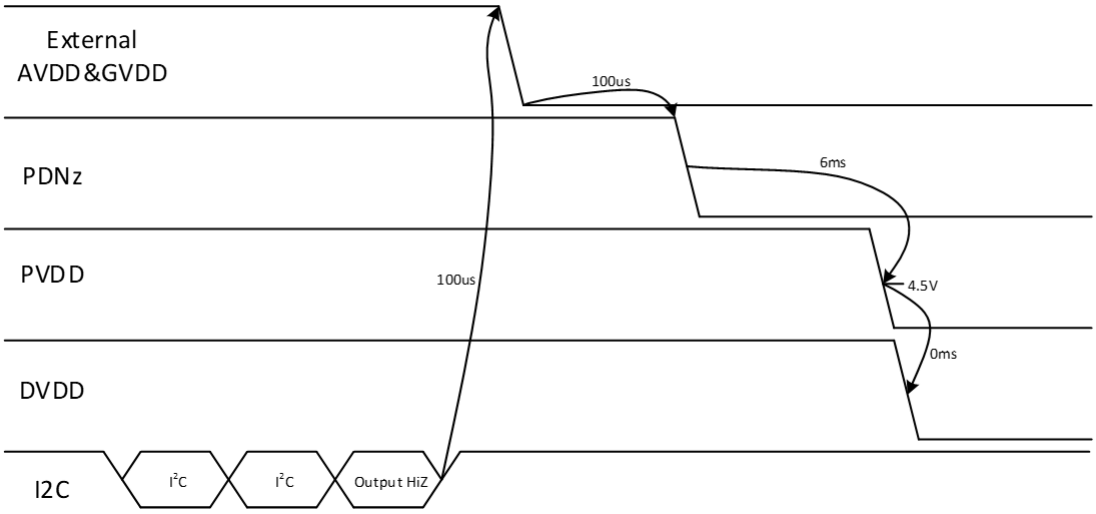

Figure 3-8. TAS5828/TAS5827 Power-Down Sequence for External GVDD/AVDD

4 Summary

Audio amplifier efficiency is crucial in portable speakers, as its improvement means a noticeably longer playback experience for users. The efficiency of Class-D audio amplifiers can be effectively improved through TI's innovative Class-H envelope tracking algorithm and external GVDD and AVDD. These efficiency improvements also bring system benefits, including reduced temperature rise and extended battery life, ultimately benefiting end users.

5 References

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3. PurePath™- Console 3 (PPC3). https://www.ti.com/video/5817768371001?keyMatch=PPC3&tisearch=universal_search
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