



## **JESD204B Xilinx/Ti ADS42JB69 Interoperability Report**

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### Introduction

This document describes the method and tests carried out to test interoperability between the Xilinx LogiCORE JESD204 v5.1 IP and the Ti ADS42JB69 ADC.

### Date

January 2014

### Scope

Interoperability testing was limited to use existing hardware supporting JESD204B Subclass 1 only. Testing of JESD204B Subclass 2 functionality is not included at this time.

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## Hardware

### Xilinx KC705 Evaluation Board

The Kintex<sup>®</sup>-7 FPGA KC705 Evaluation Kit includes all the basic components of hardware, design tools, IP, and a pre-verified reference design for system designs that demand high-performance, serial connectivity and advanced memory interfacing. The included pre-verified reference designs and industry-standard FPGA Mezzanine Connectors (FMC) allow scaling and customization with daughter cards.

The Xilinx KC705 is described in detail here: <http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm>

### Ti ADS42JB69 System Evaluation Board

The TI ADS42JB69 evaluation module contains a 16-bit ADS42JB69 dual-channel, 250-MSPS analog-to-digital converter and a TI LMK04828 clock jitter cleaner. It has transformer-coupled analog inputs accommodating a wide range of signal sources and frequencies. Both the ADC device and the LMK04828 clock generator are controller via a software GUI.

The ADS42JB69 dual-channel ADC supports the JESD204B serial interface (Subclass 0,1, and 2 compliant) with data rates up to 3.125Gbps. The buffered analog input provides uniform input impedance across a wide frequency range.

## Hardware Setup

The KC705 board is configured in its default state and powered using the supplied PSU. The USB JTAG is required for connection to the controlling PC. Two FPGA design bitstreams were generated to support the corresponding ADS42JB69 operating modes. The FPGA designs are based around the Xilinx JESD204 v5.1 LogiCORE IP with additional external supporting logic. Xilinx Vivado Lab Tools were used to configure, monitor and control the operation of the hardware. The FPGA designs support initial device setup and on-the-fly configuration changes via control register accesses. These facilities allow access to the AXI-Lite accessible registers of the Xilinx JESD204 LogiCORE IP.

The ADS42JB69 Evaluation board is connected to the HPC FMC of the KC705 board. Additional 5V supply is required to power the ADS42JB69 system evaluation kit. The ADS42JB69 is configured and controlled via USB from the TI ADC GUI application running on a windows PC. The analog inputs were sourced from the Agilent 81130A Pattern Generator.

The ADS42JB69 evaluation board (EVM) includes the LMK04828 clock generator that provides a low-jitter ADC sampling clock along with the transceiver reference clocks, device clocks, and master SYSREF signal for a complete JESD204B subclass 1 clocking solution. The reference and device clocks and the continuous SYSREF signal are forwarded to the FPGA-based JESD204 receiver IP via the FMC interface. The LMK04828 device is also configured via the ADC GUI.

## Deterministic Latency Test Setup

In order to prove deterministic latency for the entire system (analog in to samples out), the following test setup was used. Agilent 81130A pattern generator was setup to output a low-frequency (2 Mhz) square wave that was connected to one of the differential analog inputs of the ADS42JB69 device (Channel A), as well as one channel of an oscilloscope.

The FPGA JESD204 receiver IP data stream output was decoded into converter samples using the configuration-specific mapping format. The MSB of Converter A’s samples was connected to an SMA jack on the KC705 board and this was then connected to the second oscilloscope channel.

This setup allowed the time between the rising edge of the input signal entering the ADC and the corresponding MSB toggling at the receiver IP output to be measured directly using oscilloscope cursors. The obtained measurement incorporates the overall system latency, not just the JESD204B link latency.

## Xilinx IP Configuration

The Xilinx LogiCORE JESD204 v5.1 IP Core supports JESD204B on Artix-7, Kintex-7, Zynq and Virtex-7 devices. See the IP User Guide for details. The IP is configured for Kintex-7 devices using the GTX transceivers only for this interoperability testing.

The tested designs used the LogiCORE configured as 4-lane, JESD204B, Subclass 1. For the dual lane ADS42JB69 mode, software selectable lane disable was used to disable the unused lanes. ILA Disabled mode was not applicable for the tested multi-lane configurations.

## ADS42JB69 Device Configuration

The ADS42JB69 device supports two JESD204 formats. The tested configurations are shown in Table 1 :

Lanes (L)	Convertors (M)	Octets per Frame (F)	Samples per Frame (S)	Frames per Multiframe (K)	Sample Rate (MHz)	Serial Line Rate (Gb/s)	GT Reference Clock (MHz)	Xilinx JESD204 RX Core Clock (MHz)
4	2	1	1	20	250	2.5	250	62.5
2	2	2	1	20	156.25	3.125	156.25	78.125

Table 1- ADS42JB69 JESD204B configurations

## Interoperability Tests

The following table outlines the tests carried out.

Test Number	Test	Description	Interoperable	Notes
1	Sync request	Test correct operation when sync~ is requested by the receiver. The receiver should request sync following reset. It is also possible to force sync~ low when the FPGA is the receiver to re-request sync.		
1.1		Check K28.5 transmitted by transmitter in response to sync request.	Yes	The receiver was seen to drive SYNC~ low after a reset and using test design "Force ReSync" facility.  K28.5 characters were seen at the receiver in response to a SYNC request.
1.2		Check ILA or Data follows K28.5 when sync~ goes high.	Yes	The ILA was seen after SYNC~ goes high.
1.3		Check ILA or Data following K28.5 is aligned to frame clock.	Yes	At the receiver data was observed to be correctly aligned after the ILA sequence (using Vivado Integrated Logic Analyzer).
2	Initialization	Test the link initializes correctly from reset and power on.		
2.1		Check Alignment correct at receiver by inspecting sync~ de-assertion.	Yes	The link was seen to initialize correctly. Lane Alignment was seen to be correct for multi-lane modes.
2.2		Check ILA transmitted and received following K28.5 when ILA supported.	Yes	Duplicate of 1.2.
2.3		Check data transmitted and received following K28.5 when ILA disabled.	N/A	

3	Framing	Test the data passes correctly for all framing formats supported by the hardware.		
3.1		For each frame format supported by the ADC the IP will be reconfigured and the link reestablished and the sample data verified by comparing the analogue data with the expected pattern.	Yes	<p>Modes tested : (see Table 1 )</p> <p>LMF=421 OK LMF=222 OK</p> <p>Data captured, demapped, and displayed using “analog” bus plot in Vivado ILA at ADC sampling rate.</p> <p>Tested using analog signal sources and ADS42JB69 digital test patterns.</p>
4	Initial Lane Sync Sequence	Test the initial lane sequence is generated and received correctly including correct passing of the JESD204 configuration bytes.		
4.1		Check the ILA is generated with the correct frame and multiframe numbers.	Yes	Captured and viewed in Vivado ILA.
4.2		Check the Configuration data bytes are transferred correctly by inspecting register contents.	Yes	The configuration bytes were captured and viewed in Vivado ILA, and by interrogating values in Xilinx JESD204 IP registers.
5	Idle Mode	Test the link operation when one or more convertors connected to the link are inactive		
5.1		Check the link is kept alive when one or more convertors is disabled	Yes	<p>Once synchronization is achieved, SYNC<sup>~</sup> remains deasserted when one or both ADS42JB69 convertors are disabled.</p> <p>The link remains operational and dummy samples were observed using Vivado ILA.</p>

5.2		Check the inserted dummy samples do not prevent the generation of alignment characters	Yes	Alignment characters were observed on inactive convertor lanes with scrambling enabled and disabled.
6	Scrambling	Test for correct link operation with scrambling enabled and disabled.		
6.1		Check for correct data with scrambling disabled.	Yes	Correct output observed. As expected, incorrect data was received with scrambling enabled in TX or RX JESD204 device only.  Tested using analog signal sources and ADS42JB69 digital test patterns.
6.2		Check for correct data with scrambling enabled.	Yes	Correct output observed.  Tested using analog signal sources and ADS42JB69 digital test patterns.
6.3		Check the first few octets following the ILA are correct by using logic analyzer to check early sync option.	Yes	The received data was correct immediately following the ILA sequence.  Tested using ADS42JB69 digital test patterns.
7	Deterministic Latency	Test Subclass 1 deterministic latency		
7.1	LMFC Alignment	Check ADC and FPGA correctly align to all supported LMF periods	Yes	Implied LMFC alignment observed via Vivado ILA - relative alignment of SYSREF, ILA sequence and RX core data output.
7.2	SYSREF Capture	Check ADC and FPGA capture SYSREF correctly and restart LMF Counter.	Yes	Implied LMFC alignment (hence SYSREF capture)

				observed via Vivado ILA - relative alignment of SYSREF, ILA sequence and RX core data output.
7.3	End to End Latency	Check Latency is fixed between resets and using all supported lane and frame formats.	Yes	<p>Low-frequency “square” wave applied to ADC input, and it’s inverse to oscilloscope channel 1. Data output (sign bit only – “zero crossing”) displayed on oscilloscope channel 2.</p> <p>Overall end-to-end latency was thus directly measured, showing excellent repeatability between resets</p>
8	Test Patterns	Test generation and reception of test patterns detailed in JESD204B.		
8.1	Link Layer Test Modes	Check Sequences defined in section 5.3.3.8.2 are transmitted by the Tx device, and received and verified correctly by the Rx device where appropriate.	<p>Yes</p> <p>D21.5</p> <p>K28.5</p> <p>Repeated ILA</p> <p>RPAT</p>	D21.5, K28.5, Repeated ILA, and RPAT test sequences observed and inspected using Vivado ILA; No link errors were detected.
9	Supported Line Rates	Test correct operation at all rates supported by hardware.		
9.1		Check operation at MIN Gbps line rate.	YES	<p>The link was tested at 1 Gbps line rate by scaling the ADC sampling rate and JESD204 interface rate by modifying the LMK04828 clock divider settings.</p> <p>1 Gbps is the minimum line rate supported by the Xilinx JESD204 IP.</p>

9.2		Check operation at MAX Gbps line rate.	Yes	The link was tested at configuration-specific maximum line rates:  LMF=421 Mode – 2.5 Gbps LMF=222 Mode – 3.125Gbps
10	Alignment character replacement	Test the correct insertion (Tx) and reinstatement (Rx) of alignment characters during normal data transmission as per 5.3.3.4.2 and 5.3.3.4.3. Check for alignment character insertion using logic analyzer in FPGA.		
10.1		Check for alignment character insertion when scrambling disabled.	Yes	Alignment characters were observed in Vivado ILA at the receiver.
10.2		Check for alignment character insertion when scrambling enabled.	Yes	Alignment characters were observed in Vivado ILA at the receiver.

## Compliance to JESD204B Specification

The interoperability tests in the previous section shall cover the items detailed in the table below.

Spec section	Contents	Tested by Interop	Notes
1	Scope	N/A	
2	References	N/A	
3	Terminology	N/A	
4	Electrical	Partial	Electrical interoperability is tested but compliance is not.
4.1	Overview	Partial	Electrical interoperability is tested but compliance is not.
4.2	Compliance Types	Partial	Electrical interoperability is tested but compliance is not.
4.3	Interconnect	Partial	Electrical interoperability is tested but compliance is not.
4.4	Compliance to OIF SxI-5	Partial	Electrical interoperability is tested but compliance is not.
4.5	Compliance to LV-OIF-6G-SR	Partial	Electrical interoperability is tested but compliance is not.
4.6	Compliance to LV-OIF-11G-SR	Partial	Electrical interoperability is tested but compliance is not.
4.7	Device Clock	Partial	Limited range of Device Clock frequencies.
4.8	Frame Clock & LMF Clock	Partial	Limited range of LMF periods.

4.9	SYNC Interface	Partial	SYNC~ signal is used in interop testing but compliance not tested.
4.10	Lane-to-lane Inter-device Sync	Yes	
4.11	SYSREF Signal	Yes	
4.12	Skew Budget	No	Unable to test in interop.
4.13	Control Interfaces	Partial	Left to user in JESD204B Spec. USB used in interop.
5	Data Stream	Partial	See Interoperability Tests Table
5.1	Transport Layer	Partial	See Interoperability Tests Table
5.1.1	Overview	N/A	
5.1.2	User Data Format for and Independent Lane	No	Multi-lane devices used in interop
5.1.3	User Data Format for Multiple Lanes	Partial	Only formats supported by ADS42JB69 were tested (Table 1)
5.1.4	Tail Bits	No	Supported formats do not require tail bits
5.1.5	Idle Mode	Yes	
5.1.5.1	General	Yes	
5.1.5.2	Dummy Samples	Yes	
5.1.6	Test Modes	No	Transport Layer Test Modes not supported by the Receiver IP
5.1.6.1	General	N/A	
5.1.6.2	Short test pattern	N/A	
5.1.6.3	Long test pattern	N/A	
5.2	Scrambling	Yes	
5.2.1	Polynomial	Yes	
5.2.2	Bit Order	Yes	
5.2.3	Scrambler Type	Yes	
5.2.4	Early Sync Option	Yes	
5.2.5	Initial State	N/A	
5.2.6	Scrambling Disable	Yes	
5.3	Data Link Layer	Partial	See Interoperability Tests Table
5.3.1	8B10B	Yes	
5.3.2	Transmission Order	Yes	
5.3.3	Link Operation	Partial	See Interoperability Tests Table
5.3.3.1	Code Group Sync	Yes	
5.3.3.2	SYNC~ Signal Combining	Yes	
5.3.3.3	Initial Frame Sync	Yes	
5.3.3.4	Frame Alignment monitoring and Correction	Partial	See Interoperability Tests Table
5.3.3.4.1	Alignment Characters	Yes	

5.3.3.4.2	Character Replacement without Scrambling	Yes	
5.3.3.4.3	Character Replacement with Scrambling	Yes	
5.3.3.4.4	Frame Alignment Correction in Rx	No	Not possible to inject alignment errors
5.3.3.5	Initial Lane Synchronisation	Yes	
5.3.3.6	Lane alignment monitoring and correction	No	Not possible to inject alignment errors
5.3.3.7	Link re-initialization	Yes	
5.3.3.8	Test Modes	Yes	
5.3.3.8.1	General	Yes	
5.3.3.8.2	Test Sequences	Yes	
6	Deterministic Latency	Yes	
6.1	Introduction	N/A	
6.2	No Support (SC0)	N/A	
6.3	Using SYSREF (SC1)	Yes	
6.4	Using SYNCB (SC2)	No	
6.4.1	Principles of SYNCB sampling	No	
6.4.1.1	SYNCB Generation	No	
6.4.1.2	Adjustment Resolution & Clock	No	
6.4.1.3	Detection resolution at Tx	No	
6.4.1.4	SYNCB de-assertion	No	
6.4.2	Master & slave configurations	No	
6.4.2.1	ADC	No	
6.4.2.2	DAC	No	
6.5	Interop with JESD204A	N/A	Both devices are JESD204B in this interop
7	Receiver Operation	Partial	See Interoperability Tests Table
7.1	Code Group Synchronisation	Yes	
7.2	Initial Frame Synchronization	Yes	
7.3	Frame Alignment monitoring and correction	No	Not possible to inject alignment errors
7.4	Initial Lane Synchronisation	Yes	May not be possible to check time to align
7.5	Lane alignment monitoring and correction	No	Not possible to inject alignment errors
7.6	Error Handling	No	Not possible to inject errors
7.6.1	Error Kinds	No	Not possible to inject errors
7.6.2	Data Output on Error	No	Not possible to inject errors
7.6.3	Errors Requiring re-	No	Not possible to inject errors

	initialization		
7.6.4	Error Reporting via SYNC interface	No	Not possible to inject errors
7.6.5	Error Reporting via control interface	No	Not possible to inject errors
8	Transmitter Operation	Yes	
8.1	Synchronisation	Yes	
8.2	Initial Lane Alignment Sequence	Yes	
8.3	Link Configuration Data and Encoding	Yes	
8.4	SYNCB Signal Decoding	Yes	
8.5	SYNCB detection	N/A	Subclass 2 only
9	Device Classification	N/A	

## Document History

Revision	Date	Change Details
1.0	02 April 2014	Initial release

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