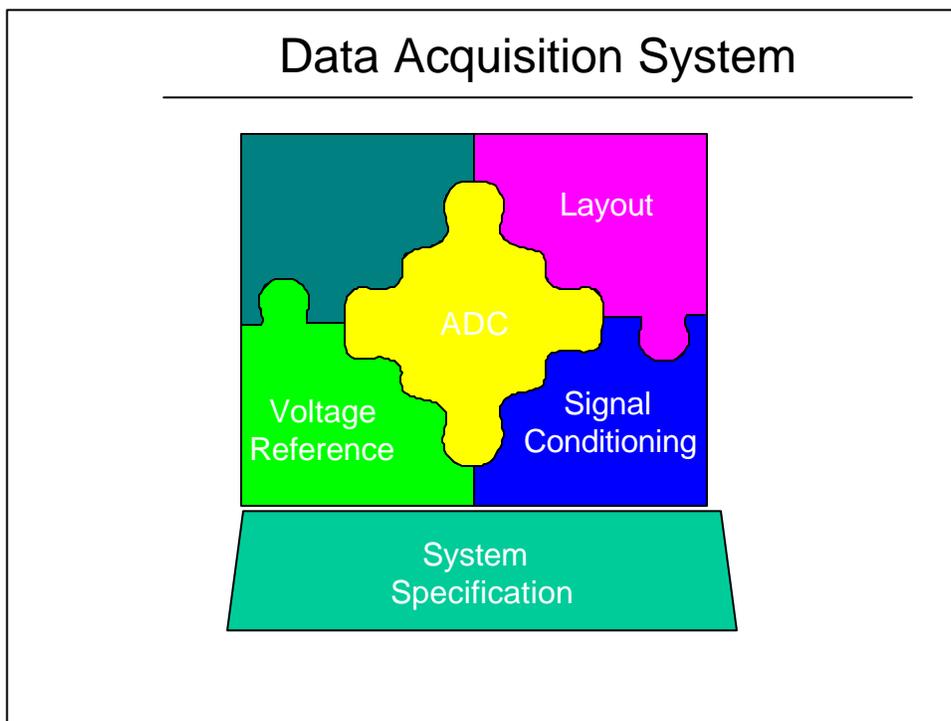# Section 2

Applying a 16-Bit SAR Converter
Considerations in the Design of a
General-Purpose Data Logger

Considerations in the design of a 16-bit data logger

How can you obtain maximum performance from an analog interface circuit? This section includes the basics and advantages of SAR converters illustrated with a design example.

- Choosing the right converter for the job.

- Understanding the significant role support circuits play in the application's success.

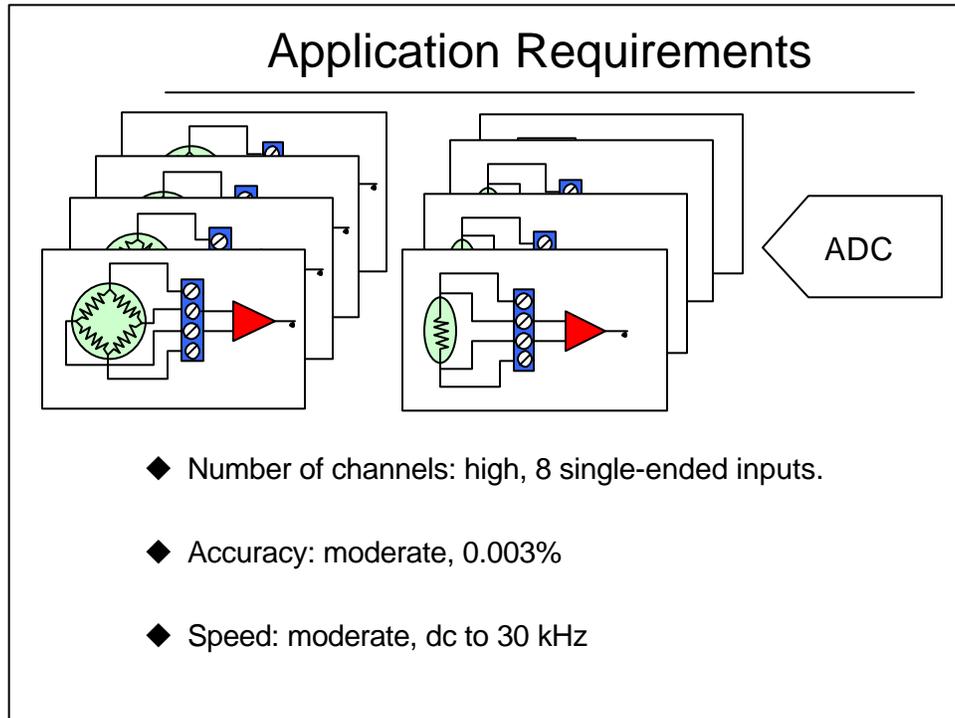- Careful layout, filtering and grounding techniques.

Discussion Topics

- ◆ Converter Technology
- ◆ Choosing the Correct ADC
- ◆ Signal Conditioning
- ◆ Reference Voltage
- ◆ Anti-aliasing Filter
- ◆ Sampling Clock
- ◆ Grounding
- ◆ Layout
- ◆ Digital Considerations

These are the topics we will discuss:

- Converter Technology
- Choosing the correct ADC
- Signal Conditioning
- Reference Voltage
- Anti-aliasing filter
- Sampling clock
- Grounding
- Layout
- Digital considerations

Application Requirements

◆ Number of channels: high, 8 single-ended inputs.

◆ Accuracy: moderate, 0.003%

◆ Speed: moderate, dc to 30 kHz

In this example, we have various transducers, which will require monitoring.

The basic system requirements are listed above.

Choosing the Correct ADC

◆ Characteristics and number of signal(s) to be
digitized.
◆ Speed of response
◆ Power: battery or mains
◆ Host system
■ Parallel interface
■ Serial interface
◆ Portability
◆ Resolution/Accuracy

There are many factors to be considered when choosing a data
converter. Here are some of the points to consider. The terms "parallel"
and "serial" data converter refer to the method used to communicate
with the device. In many cases, this decision is of primary
consideration, and is usually settled upon early in the system design
phase.

• Parallel devices tend to be faster, dissipate more power and take up
more PWB area.

• Serial devices tend to be slower, dissipate less power (modern
converters tend to have auto powerdown between samples) and
take
up less PWB area.

The choice of which type of device is right for your applications will
depend upon a number of factors.

• Characteristics of the signal(s) to be digitized.

• Speed of response for control-loop systems

• Power: battery or mains

• Host system: DSP, micro, or custom via FPGA

• Portability

Selecting ADC Topology

ADC Topology	F Conversion	Resolution	Comments
SAR	< 2 Msps	Up to 18-bit	Simple operation, low cost, low power.
Delta-Sigma	< 20 Msps	Up to 24-bit	Slow, moderate cost.
Flash	< 500 Msps	Up to 10-bit	Fast, expensive, large power requirements.
Pipeline	< 200 Msps	Up to 16-bit	Fast, expensive, large power requirements.

When selecting an Analog-to-Digital Converter (ADC) for a particular application, a good first criteria is to look at the topology of the ADC. This table shows the four main groups. Each architecture has distinct characteristics that need to be properly understood to maximize the benefits of the chosen ADC.

The most popular and versatile converter is the Successive Approximation Register (SAR) type. These converters work by comparing the analog signal voltage to known fractions of the full scale voltage and setting or clearing bits in a data register as a consequence.

SAR Converters
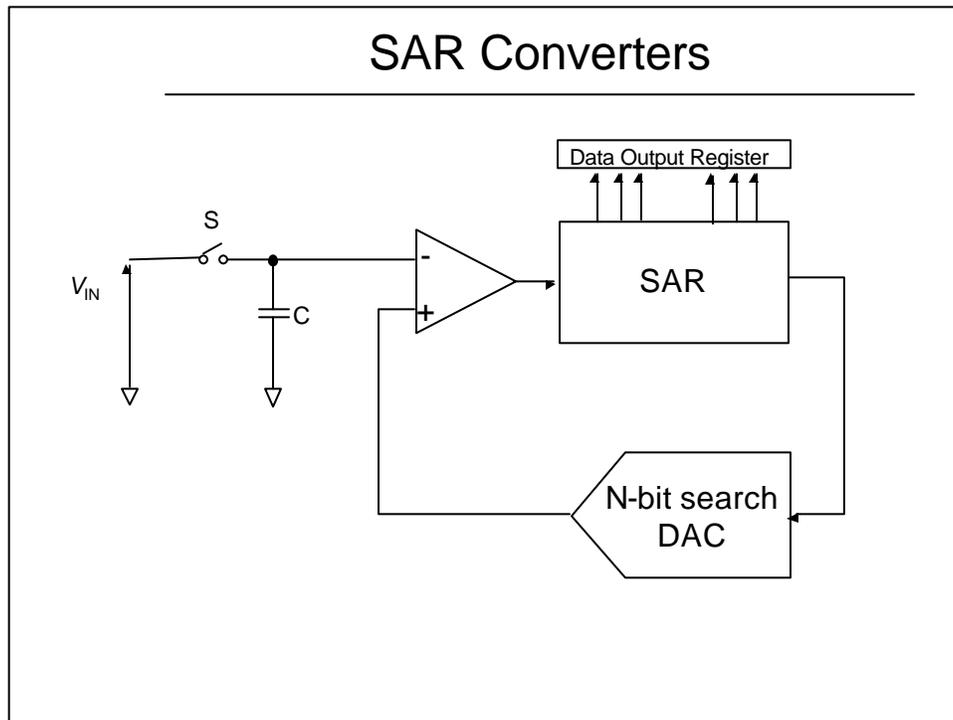
Modern SARs use a C-DAC to successively compare bit combinations, set or clear the corresponding bits in a data register, and they also tend to have an integrated sample/hold function.

A typical SAR conversion cycle has two phases; a sampling phase and a conversion phase.

During the sampling phase, the analog input signal is allowed to charge the ADC's Sample-and-Hold (S/H) capacitor to a level proportional to the analog input.

Conversion begins immediately following the sampling phase. Conversion successively compares the unknown value of the charge stored in the S/H capacitor to known fractions of charge. After each comparison, logic on the ADC determines if the unknown charge is greater or smaller than the known fractional charge.The process will be like this
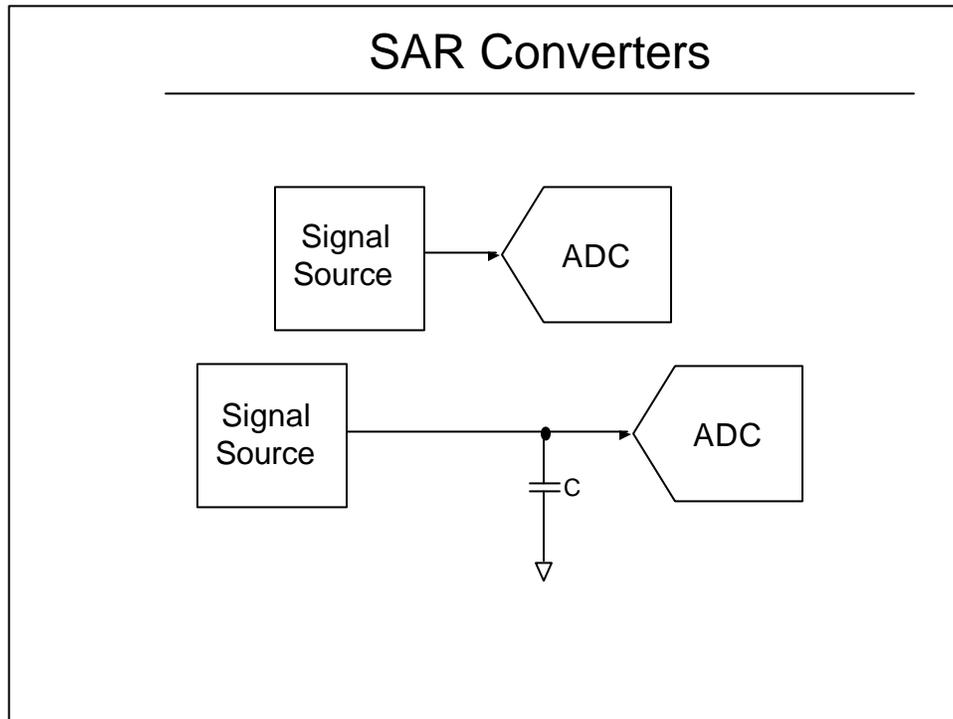
> x >1/2 FS ? - Y - set the corresponding bit
>
> x >3/4 FS ? - N - clear the corresponding bit
>
> x >5/8 FS ? - Y - set the corresponding bit
>
> etc

At the end of the process the data register will contain a binary value proportional to the value initially placed on the S/H capacitor. The user reads this value out as converted data.

SAR Converters

One word of caution: at the end of a conversion cycle there will still be a residual charge on the capacitor array. During the next sample phase, when the switch is closed, this charge will go to ground.

Depending on the output impedance of the signal source, this may be an issue especially if it is inductive.

A simple solution is to place a low-value capacitor between the channel and ground. The value of the capacitor can be small—1 pF to 33 pF is a typical range.

The capacitor ensures that after the switch (S) has closed there is a low-impedance path to ground for any residual charge enabling the signal source to begin to charge the capacitor array again.

Let's now look at some of the specifications that are important for the ADC.

Evaluating the ADC
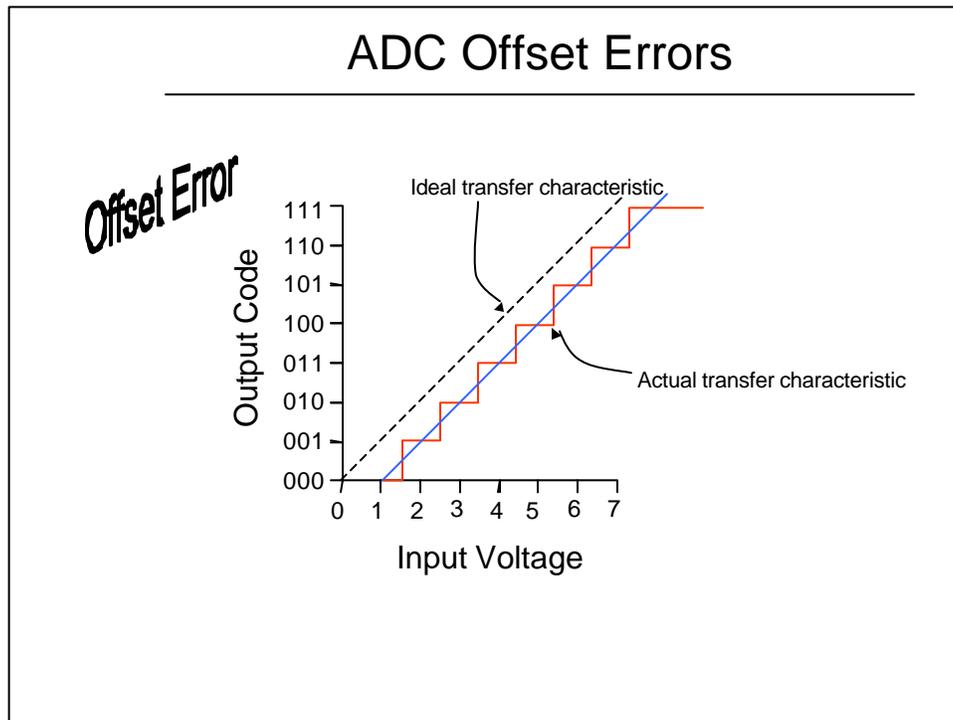
◆ Key Performance Characteristics

◆ DC
 ■ Offset error
 ■ Gain
 ■ Differential linearity
 ■ Integral linearity

◆ AC
 ■ S/N ratio and THD
 ■ Noise
 ■ Aperture errors

This section discusses the static and dynamic characteristics of the ADC.

We begin with the DC specs and look at offset error

ADC Offset Errors

The figure above illustrates the transfer function on an ideal 3-bit converter.

Offset error is defined as the difference between the nominal and actual offset points. For an ADC, the offset point is the midstep value when the digital output is zero. This error affects all codes by the same amount and can usually be compensated for by a trimming process.

If trimming is not possible, this error is referred to as the zero-scale error.

The ADS8344 is a 16-bit, 8-channel, 100-kHz converter ideal for use in battery-powered data acquisition systems.

Offset error for the ADS8344 is ±1mV

Now let's look at the Gain error.
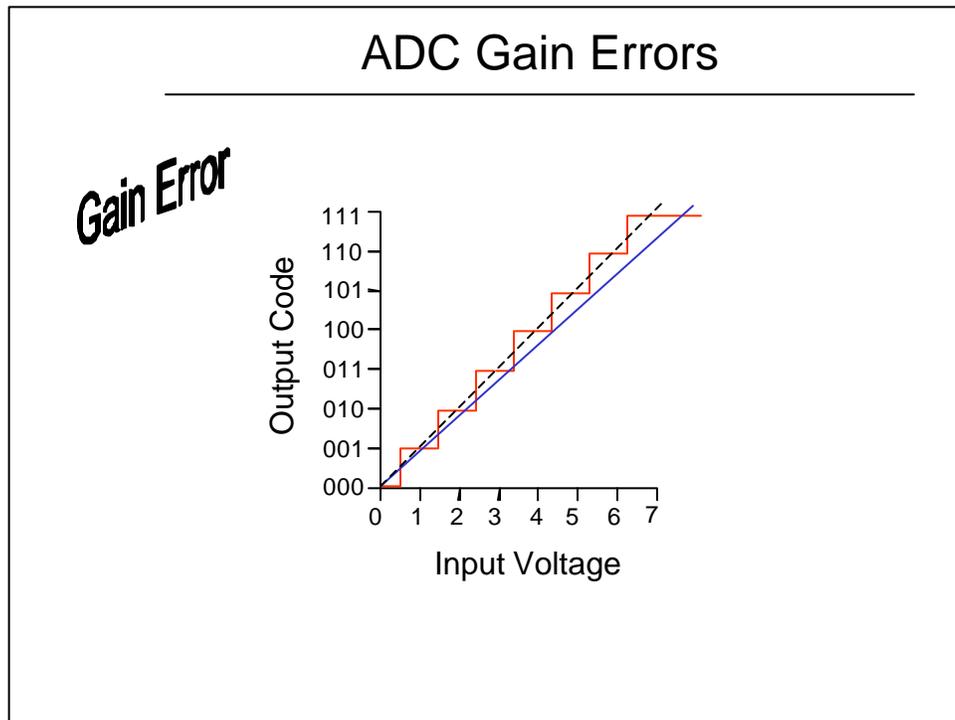
ADC Gain Errors

Gain error can be thought of as the deviation of the straight line through the transfer function at the intercept of full scale.Gain error is usually expressed as a percentage of Full-Scale Range (FSR), but can also be described in volts or LSBs.

Gain error is dominated by errors in the converter's reference voltage.

Gain error for the ADS8344 is ±0.024% -1.2mV at +5V

Now let's discuss differential nonlinearity.

ADC DNL Errors

Differential Non Linearity
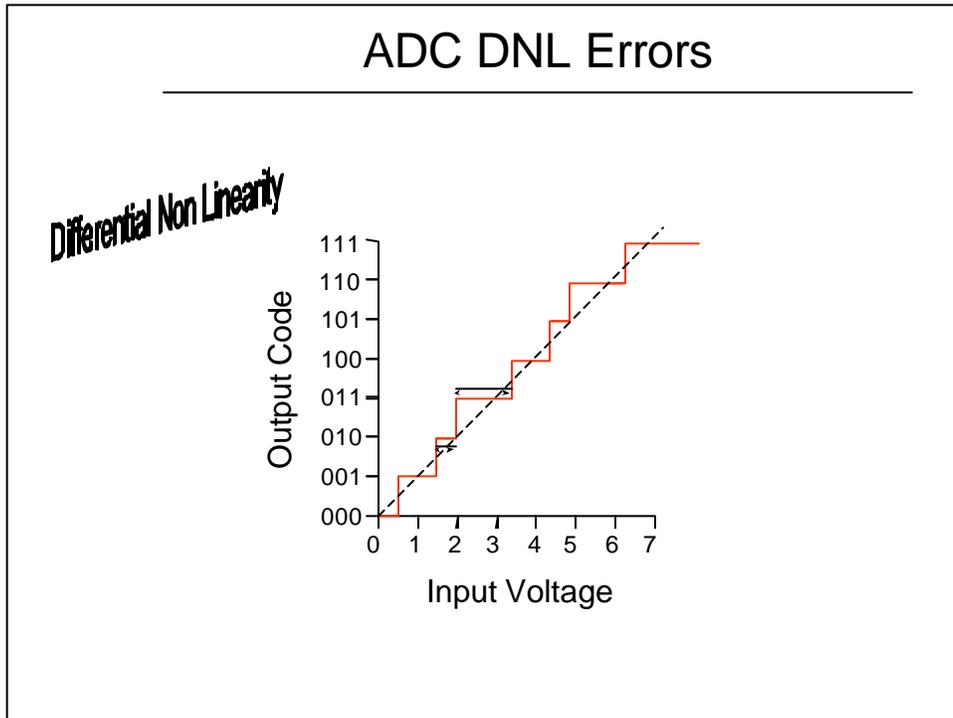
Differential nonlinearity is used to describe deviations from the ideal transition voltages in the converter's transfer function.

The figure above illustrates this.

Each code transition should occur at an interval equal to 1LSB. If the code transitions occur at intervals of more than 1LSB, or less than 1LSB, errors in the ADC's transfer function occur.

Many 16-bit ADCs are specified to have no missing codes at some resolution below 16-bits.

The ADS8344EB is guaranteed to have no missing codes to 15 bits.

In this case, the output is only guaranteed to have 15 bits of information at any given output state.

Finally, for the DC specification, let's look at integral nonlinearity

ADC INL Errors

Integral Linearity

Output Code vs Input Voltage
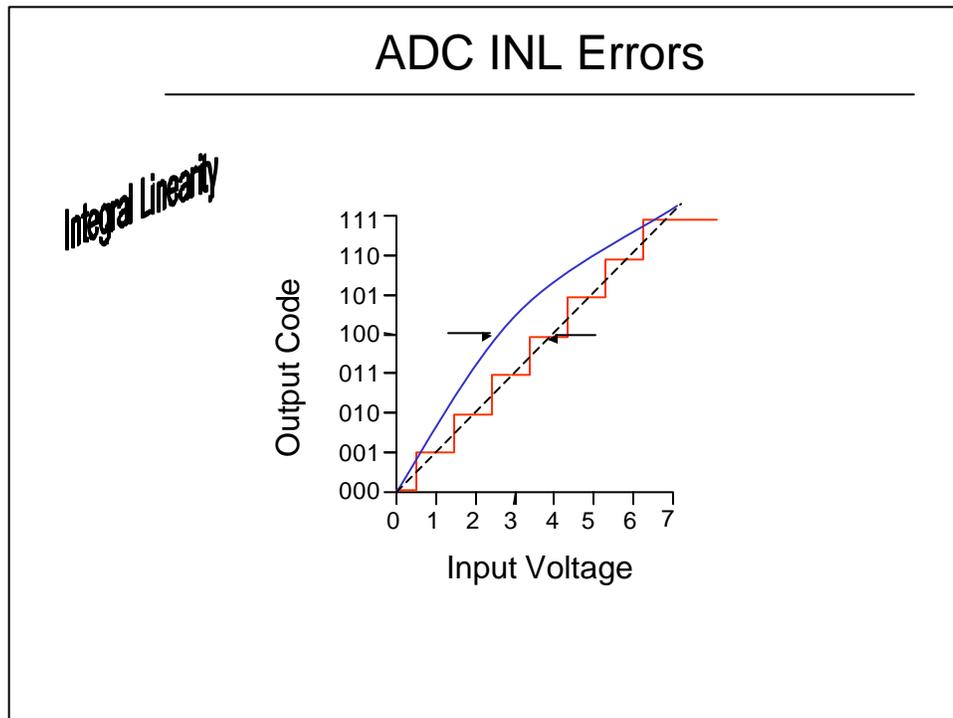
Integral linearity is used to describe the overall shape of the transfer function of the ADC. It is the deviation of code midpoints from their ideal location.

The maximum deviation from the ideal transfer function is the worst-case integral linearity error. There are two ways to describe this.
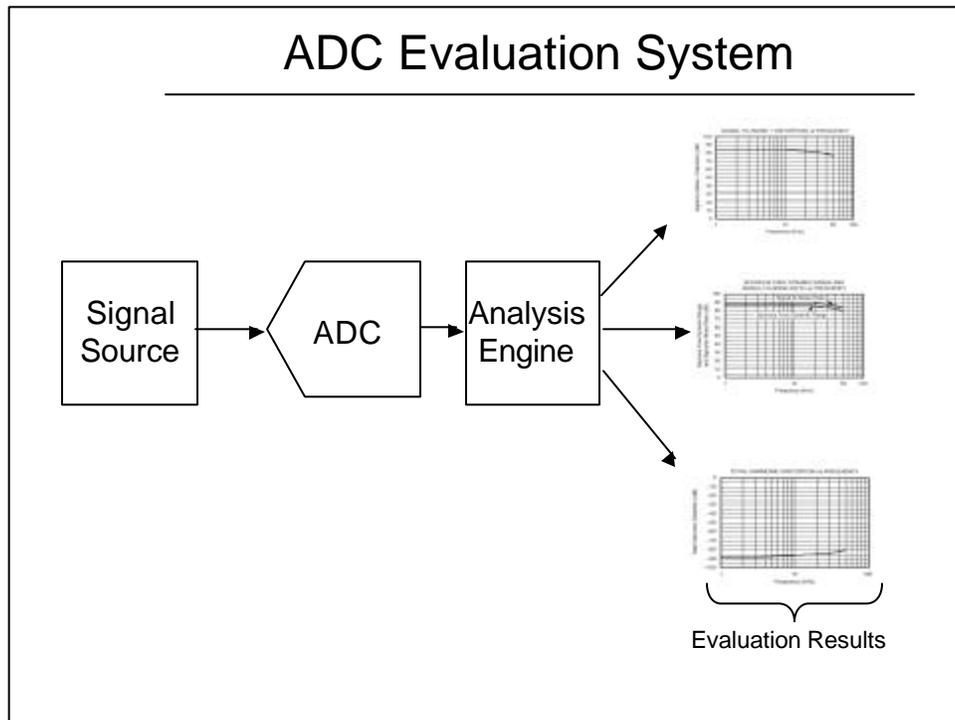
Either:

- Best fit
- End point

The figure above shows the end-point linearity. For an ADC, the deviations are measured at the transitions from one step to the next.

The ADS8344 has less than 6LSBs of INL

Now, let's examine some of the AC specifications that are important and how we derive them.

Dynamic Measurements

Although sampling ADCs can usually handle ac input signals as high as the Nyquist frequency, they will exhibit some degraded dynamic performance as the input signal slew rate is increased.

For example, the ADC's linearity tends to degrade, bandwidth rolls off and aperture jitter begins to play a significant role in the ADC's performance.

The most common method for quantifying these dynamic errors is by applying a pure sine-wave signal to the ADC and performing an FFT on the output data.

These tests yield spectral outputs from which we can calculate the S/N ratio, harmonic distortion and SINAD.

First, we need to review some of the equations that form the core of any analysis.

ADC Calculated Resolution

$$V_n = \frac{q}{\sqrt{12}}$$

$$SINAD = 6.02n + 1.76 \text{ dB}$$

$$ENOB = \frac{SINAD_{ACTUAL} - 1.76 \text{ dB}}{6.02}$$

Note: Analysis engine uses these equations to generate graphs.

It's not the intention of this seminar to derive the mathematical formulae we use--a good starting point is the application report:

"Understanding Data Converters, SLAA013"

http://www-s.ti.com/sc/psheets/slaa013/slaa013.pdf

We will merely restate the results, which are the engine of the analysis carried out. These are:

- A perfect n-bit ADC with no errors will yield a theoretical quantization noise of q/sqrt(12), where q is the value of the LSB.

This relationship leads to the well-known equation for SINAD (signal-to-noise and distortion) shown above.

- However, in practice, the ADC will yield a measured SINAD less than the theoretical value. Solving this equation for n using the measured SINAD value yields a figure of merit called the Effective Number of Bits (ENOB).

- The results of these equations and calculations on actual ADCs yields graphs which can express the converter's typical performance over a range of frequencies.

ADC Noise Histograms

Typical Histogram

ADS8344

Figure 1

Figure 2
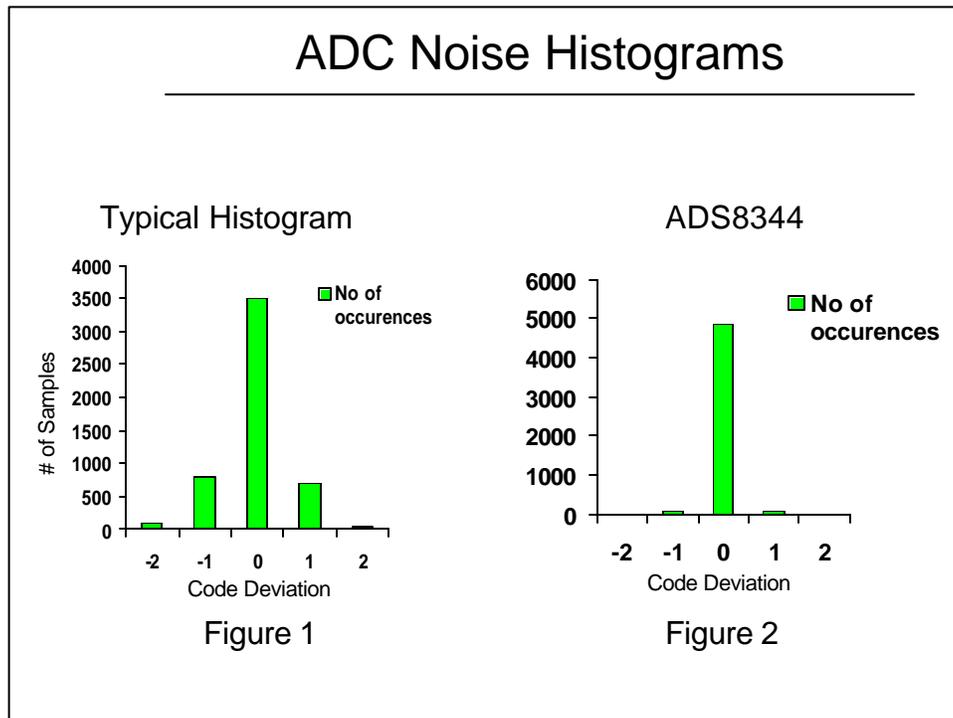
Ideally, a fixed DC input to an ADC should result in the same output code for for every conversion.

Even with a precision ADC like the ADS8344, for a given input voltage you should expect to see a range of output codes. This is caused by circuit noise within the ADC. The noise is equivalent to summing the broadband noise with the input of a noiseless ADC.

If you apply a dc signal to the ADC and record several thousand readings, the result will be a distribution of codes such as is shown here in Figure 1.

A typical histogram for the ADS8344 is shown above, Figure 2.

Noise Sources

◆ Interference noise
  ■ External sources, not easily controlled
◆ Inherent noise
  ■ Many sources

Noise depends on the bandwidth you're working with.

Resistance noise $E_{rms} = \sqrt{0.13 \quad [R(f_2-f_1)]}$ μV @ room temp

R in MΩ
(f_2-f_1) in Hz

To illustrate this over a 50-kHz range, the noise generated by a 10-kΩ resistor is around 2.9 μV.

	Reference voltage		
	2.7v	3.6v	5v
1LSB	41.2μV	54.9μV	76.3μV

16- bit LSB resolution

There are two basic sources of noise:

- Interference noise—noise picked up from outside the circuit.
- Inherent noise—noise arising within the circuit itself.

There are usually steps that we can take to reduce or eliminate interference noise such as physical shielding and careful layout around sensitive areas.

Inherent noise, however, is a function of the ADC and the circuit in which it is used. The only way in which a designer can influence inherent noise is through an awareness of the sources of noise and a careful choice of components.

For example, a 10-kΩ resistor generates almost 3 μV of Johnson (or thermal) noise at room temperature.

Comparing this 3 μV of noise with the resolution of an LSB for the ADS8344, at different reference voltages, shows the importance of understanding the noise sources involved.

## Total Noise

$$E_{total} = \sqrt{(E_1^2 + E_2^2 + E_3^2 + ...)}$$

The largest noise sources are dominant.

The combined effect of several random noise sources is found by root sum of the squares addition of the rms values of the separate noise sources.

Don't get too caught-up in the math. The technique emphasizes the larger quantities, so you can estimate total noise contribution easily.

Sample-and-Hold Errors
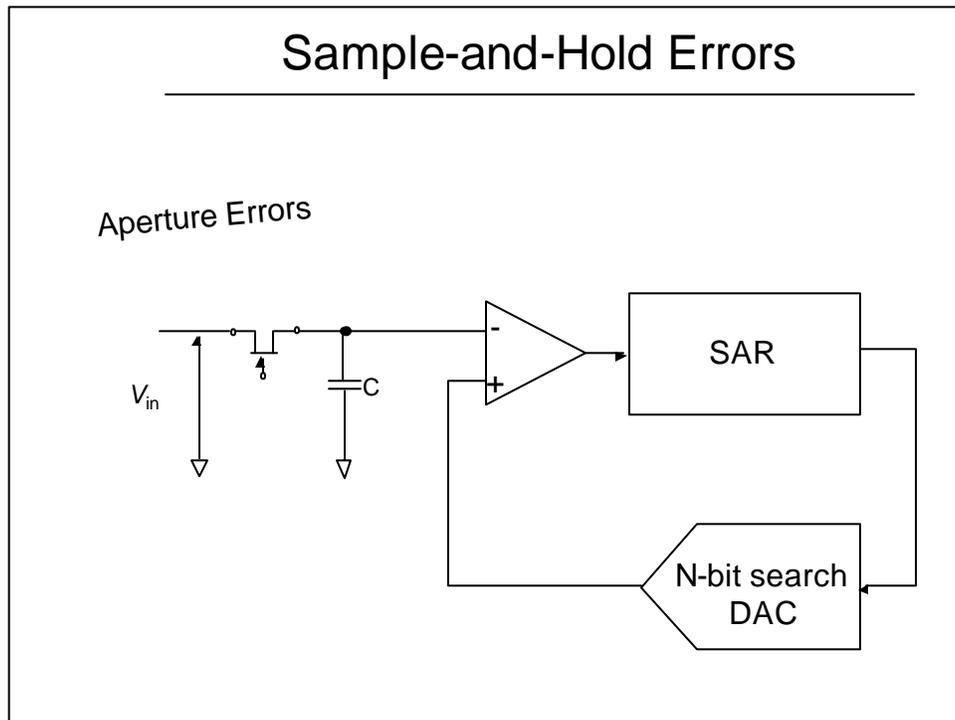
Aperture Errors

There are basically two errors caused by the process of switching over from sample mode to hold mode, these are:

- Aperture delay
- Aperture uncertainty

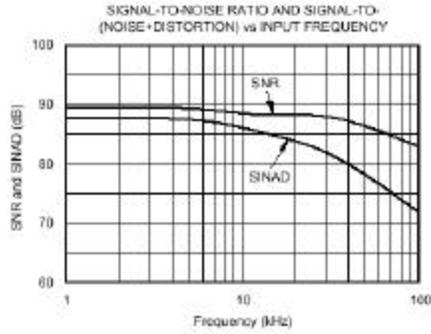Aperture delay is the elapsed time from the activation of the sample-to-hold command to the opening of the switch in hold mode. It's normally a very small number, in the order of 20 — 40 ns.

Aperture uncertainty is the variation in the time required between successive sample-to-hold commands. As you would expect, this is an order of magnitude less than aperture delay, in the order of 100 ps — 200 ps.

Frequency Dependent Errors

S/N & THD

SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY

ADS8344
A/D Converter

EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY

16-bit resolution requires 98 dB
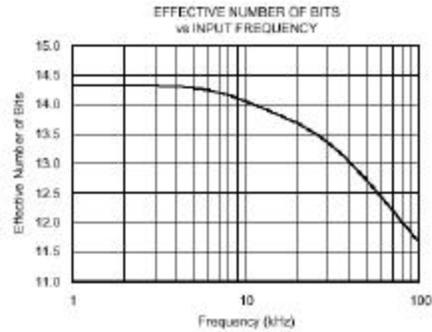
These graphs show some of the typical characteristics of the ADS8344.

You can see the effect that increasing the input signal frequency has on the effectiveness of the converter.

Protecting the ADC

◆ Large input overvoltages are expected frequently.

◆ ADCs are static sensitive.

◆ Protection usually requires PWB area.

◆ Cost / serviceability is an issue.

Most ADCs will tolerate moderate out-of-range signals without damage to the input circuit.

However, there are a few reasons why you may want to consider clamping the input.

• If large overvoltages are expected frequently.

• Whether or not the data converter will be remote and difficult to access if it fails.

• Is the data converter expensive?

Summary

DC specifications are most important
for this low-speed data logging application.

These are the important points that we must decide upon for the ADC.

In real-time signal processing applications, dynamic specifications such
as THD and S/N ratio are the most critical. This is because the signal is
changing constantly.

In measurement and control systems, where measurement accuracy
and repeatability are important, the static specifications must also be
considered carefully.

Support Circuits

Signal Conditioning

Reference

Top diffusion

Breakdown region

Zener diffusion

Jitter

Filtering
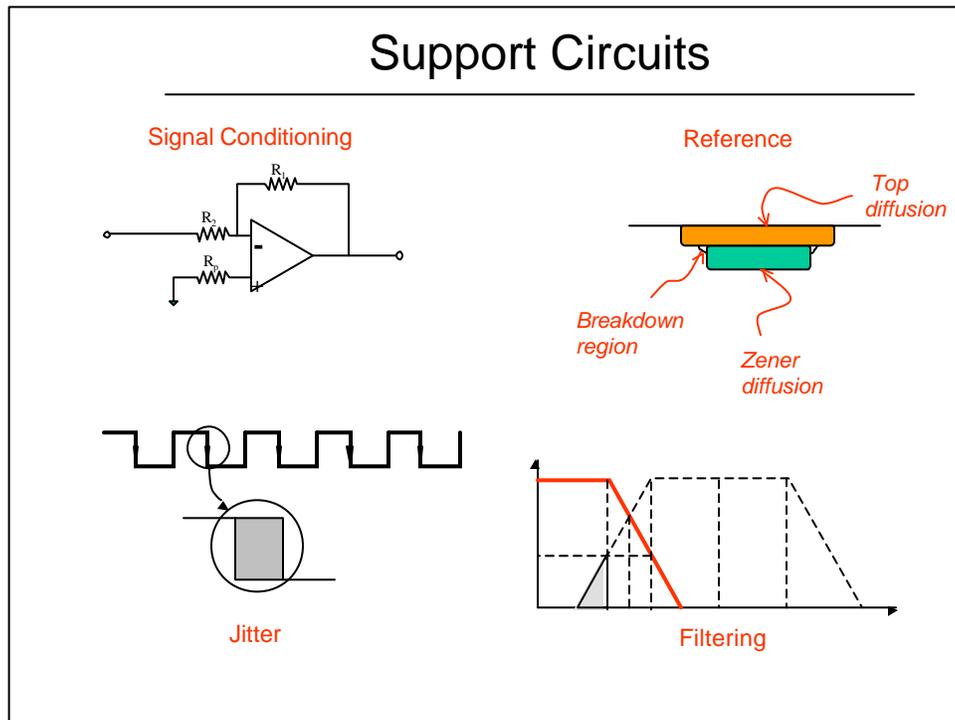
There are four support circuits that we will now consider. They play a significant role in the success of your application. They are:

- Signal conditioning circuitry
- Reference voltage circuitry
- Sampling clock
- Anti-aliasing filter

Some of these solutions may not be required; however, a knowledge of their role will help you to determine this for yourself.
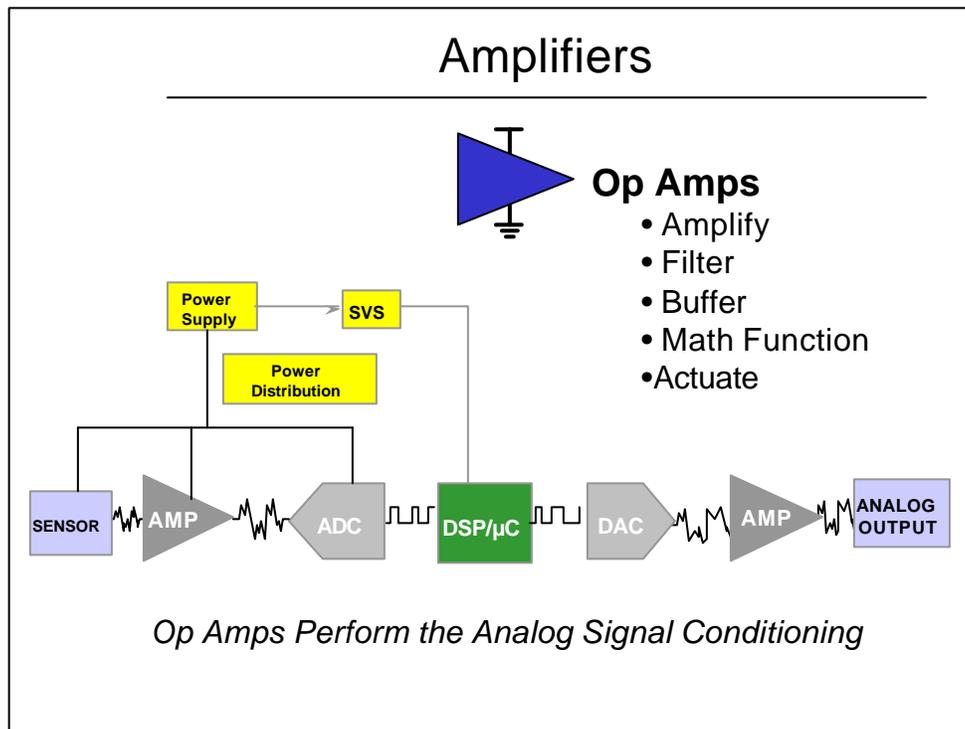
Amplifiers

Op Amps
- Amplify
- Filter
- Buffer
- Math Function
- Actuate

SENSOR — **AMP** — **ADC** — **DSP/μC** — **DAC** — **AMP** — **ANALOG OUTPUT**

Power Supply
SVS
Power Distribution

Op Amps Perform the Analog Signal Conditioning

Amplifiers are used in most data acquisition systems found in the industrial world today. They are commonly found at the beginning and end of the signal chain.

They are used as an interface between the sensors that measure or monitor physical parameters. They are also sometimes used to take that measured parameter, once it has been digitized and analyzed, and force an analog response.

For example, one might be monitoring flow rate in a system. If the rate is determined to be high, a valve could be caused to move to slow down the rate.

The Need for Signal Conditioning

◆ (Q) Why do we need amplifiers in the first place?

◆ (A) Because most Industrial Analog Signals do not work well directly with SAR based ADC's such as:

- Very tiny signals from RTD's or Bridges,

- Signals that have high common mode voltages,

- Very wide dynamic range signals,

- Or signals that need to be converted into an input the ADC can recognize, i.e. light or charge.

◆ The goal is to take all of these "hostile" signals and convert them into a voltage which equals the input voltage range of the converter.

In the real world the need for amplifiers is driven by the fact that the world is analog and in general unfriendly to many data converter designs.

Throughout this section it will be assumed that you have some type of analog signal that needs to be conditioned for the input of a data converter which has, for example, a 0 to 5 volt full scale input range.

Some signals, such as those from an RTD, bridge, or human body are so tiny, μV's to mV's, that they need to be amplified heavily. In many cases these signals are differential in nature.

Another real world situation is that the signal to be analyzed is in the presence of external noise or interference. The signal might be "riding" on top of a common mode voltages that the data converter can not accommodate.

Finally, the signal might not be a voltage at all. It may be light / photons, current or even charge. Fortunately, there are amplifier devices that are designed specifically for dealing with all of these scenarios.

Selecting the Correct Type of Amplifier

◆ What type of amplifier is required ?
- Operational Amplifiers
  - Ideal for tiny single ended signals.
  - Also used where common mode voltages are NOT an issue.
- Differential Amplifiers
  - Best for low (< 100) gain differential signals.
  - Found where high levels of common mode voltage are present.
  - Current (shunt) measurement.
- Instrumentation Amplifiers
  - Where high gain, high common mode rejection, and high input impedance are required.
- Analog Circuit Function
  - Wide dynamic range (> 60dB) signals.

The first step in the design cycle when choosing an amplifier for a data acquisition system is to determine what type of amplifier is needed.

If the signal is single ended in nature, i.e. it is referred to a common voltage like ground, then a simple operational amplifier may be best.

Not that operational amplifiers, being differential in nature, are not suited for differential signals, but there is a different class of amplifiers that are designed for these types of signals. These are called differential or instrumentation amplifiers. Rejection is what these types of amplifiers are all about. Among other considerations these devices are designed specifically to REJECT common mode signals, such as noise.

A differential amplifier (diff-amp) is a fixed gain device with relatively low input impedance. In general, diff-amps are not designed to be connected directly to a sensor. They are used most commonly to translate a differential voltage into a single ended one.

Instrumentation amplifiers (INA's) are designed to connect directly to a sensor and amplify the resulting voltage by a large (1000V/V+) factor. An INA brings together the best qualities of operational and differential amplifiers.

Finally, analog circuit function amplifiers are useful for either non-electrical or very wide dynamic range signals.

Op-Amp Technologies

◆ The process used to build an Op-Amp has a significant impact on performance
◆ Four types are used
  ■ Bipolar
  ■ JFET
  ■ CMOS
  ■ Difet
◆ These technologies are sometimes combined
  ■ BiFET or Bipolar and JFET combination
◆ Process description is usually associated with input stage of the Op-Amp

The op-amps used primarily in industrial data acquisition systems are fabricated on either Bipolar, JFET, CMOS, or *Difet* semiconductor processes.

Each of these processes have unique electrical properties that in turn impacts the overall performance of the system. Hence the type of application and nature of the signal to be conditioned directs the choice of process and amplifier.

The pros and cons of each process will be covered next.

Bipolar Operational Amplifiers

◆ Bipolar Op-Amps are characterized by
- Low input impedance, I $_{bias}$ of 1 to 100 nA,
- Low offset voltage , Vos as low as 10 μV,
- Temperature Stability, Drift as low as 0.1 μV / °C,
- Low Voltage Noise, Low as 1 nV√Hz.

◆ Small signal, low impedance high gain applications
- Weigh Scales, Geophysical Analysis , High Precision Temperature Measurement.

◆ Example device OPA277
- 2.5nA, 10 μV, 0.1 μV / °C, 3 nV√Hz
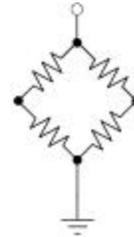
When the utmost in DC precision is required in a system, usually a bipolar based operational amplifier is best. These devices offer the highest level of common mode rejection (CMRR), open loop gain (A$_{OL}$),

offset voltage (V$_{OS}$), and associated drift (ΔV$_{OS}$/T). In addition, the voltage noise of a bipolar amplifier is very low. This is important because this noise source will be amplified by the closed loop gain of the amplifier, which is set very high for small signal sources like RTD's and bridges.

On the down side, the current noise of a bipolar op-amp is very high and the input impedance is low, as compared to other amplifiers. These two characteristics make bipolar amplifiers poor choices for high impedance signal sources, such as those found in many medical applications.

JFET Operational Amplifiers

◆ JFET Op-Amps are characterized as having

- Moderately High Input Impedance, I_{bias} of 10 to 100pA,
- Moderate Offset Voltage, V_{os} of 0.1 to 5 mV,
- Large bias current changes with temp., I_{bias} doubles every 10 °C,
- Lowest I_{bias} noise, As low as 4 fA/$\sqrt{Hz}$.

◆ High source impedance, moderate gain applications
- Blood Analysis, CT Scanner, and Audio applications

◆ Example device OPA130
- 20 pA, 1mV, 5 pA, 4 fA/ $\sqrt{Hz}$
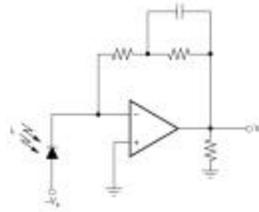
JFET input amplifiers are an excellent choice for high impedance signal sources. This type of amplifier is an ideal choice for transimpedance applications. Low current noise and distortion also make it a good choice for audio and other high frequency applications.

DC performance, voltage noise, and a change in input impedance with temperature limit the choice of applications that the JFET amplifier is suitable for. In general the JFET op-amp is the best choice when AC performance is paramount.

Difet Operational Amplifiers

- ◆ Difet Operational Amplifiers are characterized by
  - Ultimate in low current and voltage noise, 4 nV/√Hz;2 fA/√Hz,
  - Highest Input Impedance, I_{bias} as low as 3 fA ,
  - Best DC Specifications, Process allows designs that have best CMRR and AOL,
  - Highest cost, Each active device is individually isolated in glass tub , i.e. large die size.
- ◆ High Speed / Resolution Data Acquisition
  - Base Station Quantization, High End Medical, ATE
- ◆ Example device OPA627
  - 4.5 nV/√Hz, 1.6fA/ √Hz, 1pA, 106dB, 120dB

Difet, or dielectrically isolated FET op-amps offer the best of both bipolar and JFET devices. At the same time is possible to garner both DC precision and JFET AC performance. In fact with this type of fabrication technology it is sometimes possible to exceed the performance of any other process technology.

In a conventional integrated circuit process the individual components, transistors etc. , are kept electrically isolated from each other by reverse biasing the substrate based diode common in this process. In a *Difet* design the isolation process is accomplished by placing the individual components in glass or dielectric tubs. While this technique results is superior performance it also dramatically increases both the fabrication process and resulting die size. The cost of a *Difet* device is always higher than an equivalent Bipolar, JFET, or CMOS device.

This added cost and higher performance in general makes the *Difet* device suitable for only very high performance data acquisition systems.

CMOS Operational Amplifiers

◆ CMOS devices are characterized as having
  - Large Input Voltage Range, Input can often exceed both supplies,
  - Excellent Output Drive Capability, Output swings to within 1mV,
  - Excellent V_{OS}, 125µV
  - Very Low Power Requirements, Iq < 1 µA,
  - High Input Impedance, I_{bias} of 10 pA,
  - Low Cost, Built using small geometry "Digital" processes,
  - Wide variety of bandwidth and accuracy offerings.
  - Wide temperature range, -65 to +150 ° C
◆ Battery powered, low to moderate performance systems
  - Glucometer, CDAC ADC driver, CO and Smoke detectors
◆ Example device OPA336
  - ± 300mV, 3mV,125uV, 125µV, 1pA, 100kHz

When the CMOS process was first used to build amplifier products the resulting devices were generally of very low performance. They were slow, noisy, and had poor DC performance. A lot has changed since then and you can now obtain CMOS amplifiers with levels of DC precision approaching Bipolar products and AC performance that in some cases exceeds JFET ones.

As is widely known, CMOS devices are known for rail-to-rail operation, small size, low power, and cost. TI has CMOS amplifiers that can accept input signals in excess of both supply rails, whose output stages can swing to within 1mV of each supply rail, and that have bandwidths of almost 500MHz. In terms of DC performance there are devices with offset ratings of less than 100µV and A_{OL} and CMRR specifications in excess of 100dB. Also, these devices are very quiet with voltage noise floors of less than 5 nV/√Hz.

The CMOS process used at TI is very amenable to optimization. There are devices that are optimized for the following characteristics

- Speed / Power or MHz per µA. OPA348 has 1MHz BW while using only
  45mA of I_Q.

- Output drive – a very important parameter for driving CDAC based converters. OPA353 can drive a 10KΩ load to ± 1mV of each supply rail.

- Over temperature performance. -65 to 150 °C operation makes these devices very suitable for automotive and industrial applications.

- Building blocks for other amplifier applications. TI builds a wide variety of other amplifier devices using the CMOS op-amp as the central element.
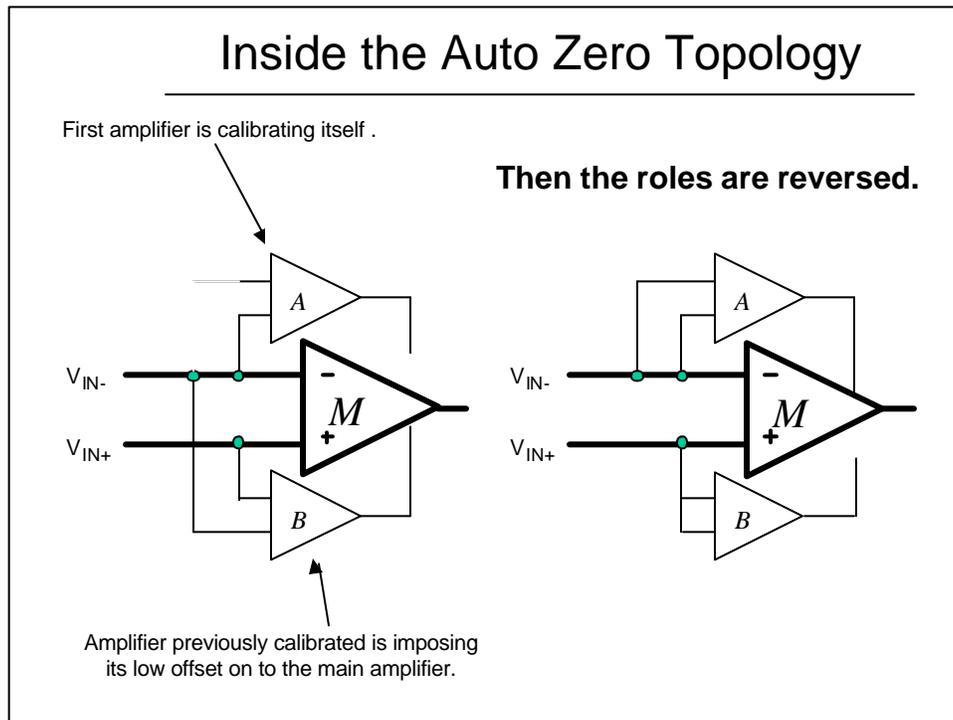
CMOS Auto Zero Amplifier

OPA335

◆ Most precise CMOS architecture
◆ Bipolar Precision + CMOS Advantages
- Rail-to-Rail input and output
- Low Power
◆ Achieves chopper type precision and drift without the chopper drawbacks
- V_{OS} and Drift – 5 μV / 0.05 μV/°C
- Noise – 1.4 μV pp
- Bandwidth – 2MHz
◆ Uses an auto-zero topology in series with a time continuous operational amplifier

The latest "version" of amplifier to take advantage of the CMOS process is the auto zero op-amp. This new topology is sometimes compared with the "chopper stabilized" type of amplifier. The reason for this is that both approaches offer the best performance in terms of offset voltage and drift.

However, the auto-zero amplifier does not suffer from the pitfalls of the chopper type. The chopper amp is known for high levels of noise and low bandwidth.

The auto-zero amplifier uses a time continuous amplifier in the signal chain that is constantly corrected for its offset voltage. This approach yields a precise, fast, low noise op-amp.
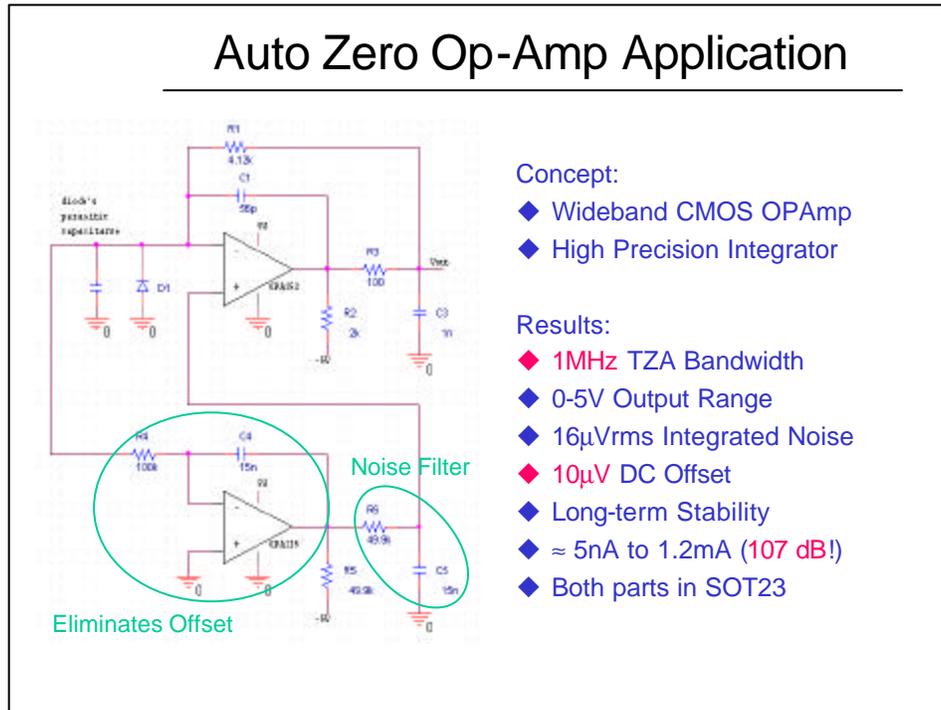
The auto zero amplifier, being a CMOS device, is ideal for single supply data acquisition systems. Due to its high levels of precision and excellent drive capability it is ideal for driving high resolution (16+ bits) data converters. A typical application would be a commercial weigh scale.

Inside the Auto Zero Topology

First amplifier is calibrating itself .

Then the roles are reversed.

Amplifier previously calibrated is imposing
its low offset on to the main amplifier.

The diagram above illustrates the action of the auto zero amplifier. At first calibrating amplifier B is imposing its previously calibrated output of the main amplifier M. During this cycle amplifier A is sampling the offset voltage present on the inverting input.

During the next cycle the main amplifier is calibrated by amplifier A to eliminate that offset voltage. So the main amplifier is continuo usly calibrated for input offset voltage. Because this action occurs over temperature as well, offset voltage drift is also eliminated.

Auto Zero Op-Amp Application

Concept:
◆ Wideband CMOS OPAmp
◆ High Precision Integrator

Results:
◆ 1MHz TZA Bandwidth
◆ 0-5V Output Range
◆ 16µVrms Integrated Noise
◆ 10µV DC Offset
◆ Long-term Stability
◆ ≈ 5nA to 1.2mA (107 dB!)
◆ Both parts in SOT23

Noise Filter

Eliminates Offset

The auto zero amplifier, OPA335, can also be used to calibrate other linear systems. In particular the above concept can be used on any inverting input amplifier system that employs negative feedback. An example of such a system is the classic transimpedance amplifier (TZA). In this case it is assumed that the input is a photodiode.

One of the limitations of the conventional TZA is that the offset voltage of the op-amp limits the dynamic range (i.e. size of the feedback resistor) available. This limitation tends to restrict its use to input current ranges of less than 60dB. In many TZA applications the input range is far higher, up to 160 dB.

In the example shown the OPA335 auto zero amplifier continuously compensates for the offset voltage of the TZA amplifier, the OPA353. The resulting circuit results in a TZA application that offers large dynamic range, low noise, and excellent DC precision.

With the addition of a negative supply and pull down resistors the output of the OPA335 and OPA353 can go from 0 to +4.999 volts, which is within 1mV of the full scale range of many data converters. This is another unique feature of the CMOS op-amp offering from TI. The outputs can actually be pulled down below the negative rail without damaging the device.

Recommended Op-Amps

Device	Offset Voltage (µV)	Input Bias Current (pA)	GBW Product (MHz)	Voltage Noise (nV√Hz)	Current Noise (fA/√Hz)
OPA131	±750	±50	4	15	3
OPA227	±75	±10	8	3	400
OPA277	±20	±50	1	8	200
OPA344	±500	±50	2	30	0.5
OPA335	±5	±50	2	50	20
OPA627	±100	±50	16	4.5	2.5

Instrumentation Devices

◆ Many types of Instrumentation Devices
  ■ Difference Amplifiers
  ■ Current Shunt Amplifiers
  ■ Instrumentation Amplifiers
  ■ Programmable Gain Amplifiers
  ■ 4-20 mA Transmitters
◆ All of these devices share similar characteristics
  ■ Combination of precision op-amp and trimmed resistors
  ■ Accept a differential voltage
  ■ Are easily programmed for a fixed gain
  ■ Used for a variety of input signal conditions

Instrumentation devices are designed to interface with specific types of sensors used to monitor physical parameters in the real world. There are devices designed to measure current, temperature, pressure and reject very high levels of common mode voltage.

Difference Amplifiers (Diff Amps)

◆ A Diff-Amp is an Op-Amp + 4 or 5 Resistors.
◆ Characterized by
  ■ Low Input Impedance , 10KΩ ~ 1MΩ
  ■ Moderate CMRR, 70 ~ 80 dB
  ■ Bandwidth, 100KHz ~ 5MHz
◆ Function is to accept differential input voltage and output a single ended voltage.
◆ Diff Amps are designed for specific functions.
  ■ Unity gain devices $V_{IN} = V_{OUT}$
  ■ Devices with gain $V_{IN} < V_{OUT}$
  ■ Devices with attenuation $V_{IN} > V_{OUT}$
  ■ Devices which support large common mode voltages:

$$V_{IN} + \quad \lightning \quad V_{OUT}$$

Difference amplifiers, as the name implies, measure the magnitude of a differential voltage and deliver an output that is proportional to it. This output is referenced to a reference voltage, V_{REF}.

The diff-amp can buffer, amplify or attenuate the input signal. A conventional diff-amp uses four precision resistors and one op-amp.

With the addition of other resistors the diff-amp can be used to hold off or interface with very high levels of common mode voltage. In fact there are devices available that allow systems that are powered from conventional analog power supplies (± 15 volts) to monitor signals that are in the presence of up to ± 200 Volts!

Difference Amplifier Topology
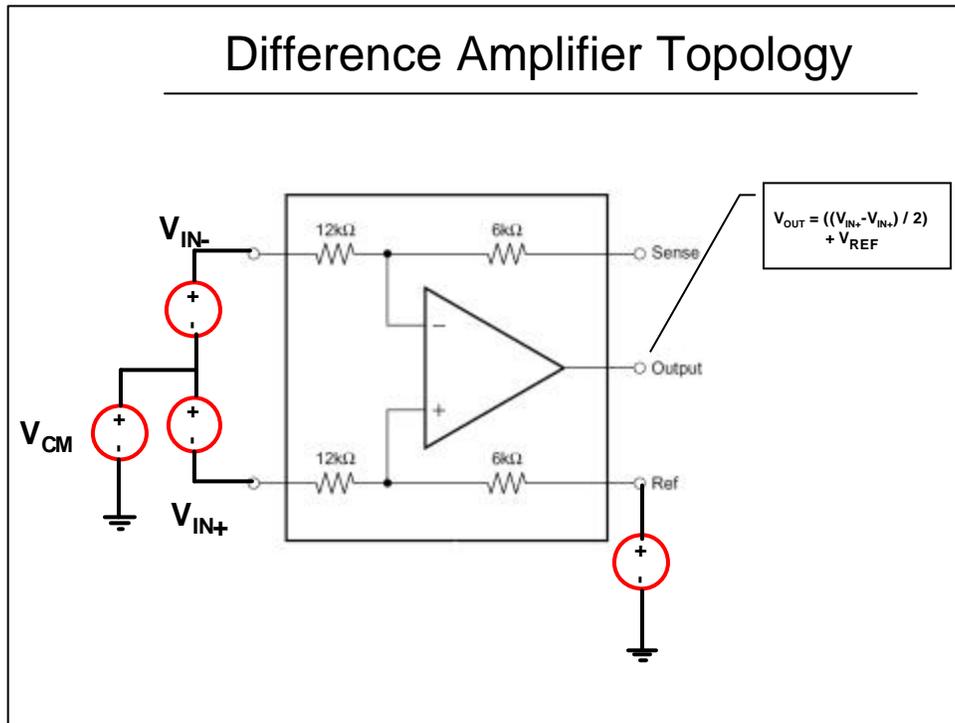
The figure above shows the topology of the conventional diff-amp. In the example the input resistors (12KΩ) are twice the value of the feedback resistors (6KΩ). This results in a design that actually attenuates the input voltage.

Why is this useful for a data acquisition system?

Suppose for example we have a data converter that is run from a single +5 volt supply whose full scale input voltage is somewhere between 0 and +5 volts. If an input voltage of –5V to +5V is be monitored then a way is needed to accurately translate this input signal to the data converter. Using a diff-amp, like the one shown above, would divide down the 10 volt input span to 5 volts (+2.5 to – 2.5). We then apply +2.5 volts to the V_{REF} pin and the input signal is now 0 to +5. In the process we have not lost any accuracy and have preserved the differential nature of the signal, thus improving noise immunity.

A final word about the nature of resistors used in instrumentation products is in order. The absolute value of these resistors is on the order of 30%. Also the match between the pairs of input or output resistors is not in general precise. Instrumentation devices achieve their high levels of performance due to the precise ratio between a feedback and corresponding input resistor. They are laser trimmed to ratios of 0.001% or better.

It is for this reason and the low, sub 1MΩ value of these resistors, that differential amplifiers are suitable for signal sources with low impedance.

High-Common Voltage Diff Amp
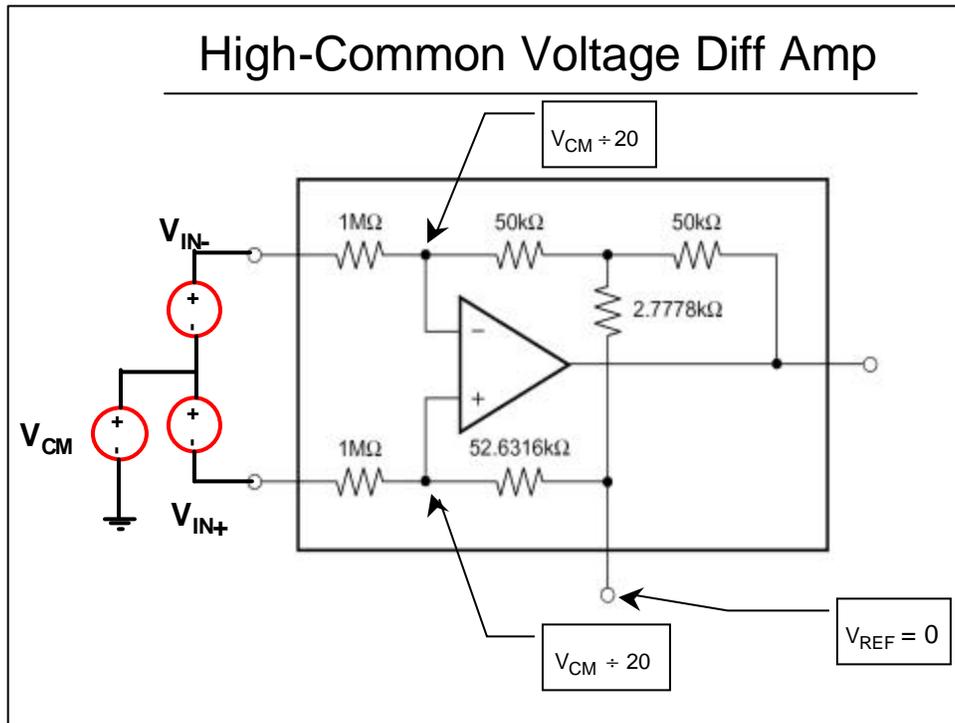
Another type of differential amplifier is a device that is designed to interface with high levels of common mode voltage. Like the conventional diff-amp we have a differential input stage whose value is compared by an op-amp and then made relative to a reference pin.

This device has an additional set of resistors that divide down the common mode voltage, in this example by 20. This type of amplifier will work with common mode voltages of up to ± 200 volts continuously ± 500 volts for up to 10 seconds. This makes it very useful for a wide variety of industrial and telecommunications applications.

An obvious question at this point is why bother with an integrated difference amplifier in the first place? Would not it be less expensive to use a combination of a discrete op-amp and resistors?

The answer is yes it would be less expensive but performance would suffer. In general, if the desire is to achieve CMRR performance of better than 60 dB and linearity of better than 12 bits, a purpose-built diff-amp is needed.
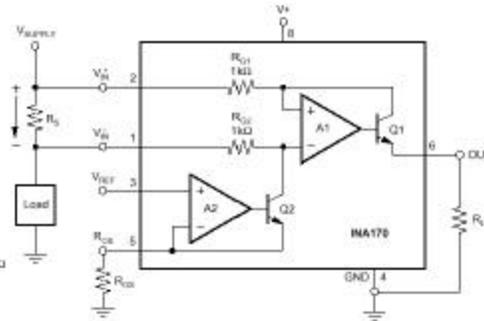
Current Shunt Monitors

INA138

High-Side, *uni-polar*
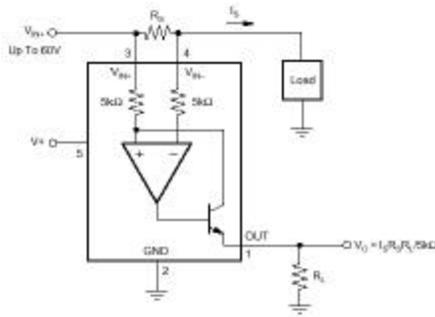
INA170

High-Side, *bi-directional*

The last type of diff-amp to be discussed is the current shunt amplifier. These devices are designed to monitor currents of up to 25 amps and can monitor supply voltages of up to 60 volts while drawing only 25mA and running on supplies as low as 2.7 volts.

There are two types of current shunt amplifiers currently available. The first uses a single op-amp and is suitable for measuring currents flowing into a load. This device is programmed by a single resistor such that the output is proportional to the current flowing into the load.

The second type is useful when it is necessary to monitor currents flowing either into or out of the load. This device has a second element in the transfer function, namely the output voltage that is desired when the load is drawing no current. This is also set with an external resistor.

Instrumentation Amplifiers

◆ Instrumentation Amplifiers (INA's) feature
- Differential Inputs
- Gain setting via a standard resistor
- Superior noise immunity, better CMRR vs frequency than standard op-amp designs

◆ There are specific INA devices for
- Single Supply Applications
- Low Noise Applications
- High Impedance Sources
- Programmable Gain

The last type of instrumentation devices to be discussed are the true instrumentation amplifiers, INAs. Like diff-amps these devices have a differential input. Unlike diff-amps they have high input impedance inputs and feature adjustable gain. The gain is set with an external resistor.

There are also devices, programmable gain amplifiers or PGAs, that have gain setting resistors built in. The gain can be set "digitally" via internal switches.

"Two" Op-Amp INA

$$Gain = \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{2 \bullet R_1}{R_G}\right)$$
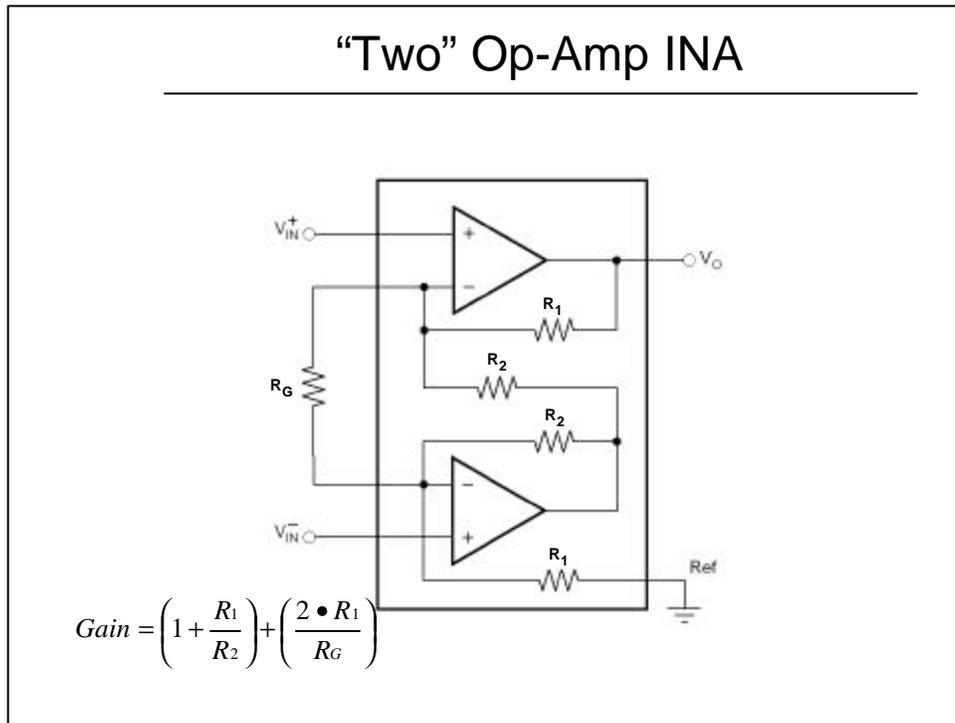
Like the op-amps that are used to construct them, there are a number of configurations and performance options available for INAs.

The most basic INA uses two op-amps and four resistors in its construction. This topology, as one might imagine, is the smallest, lowest power, and lowest cost choice available.

There are two big limitations with this type of design. First there is a minimum gain that can be had from this design. The second and more important limitation is that the CMRR ratio changes dramatically with frequency as compared with other types of INAs. This response is caused by the asymmetrical path from input to output with regard to the inputs.

As can be seen from the diagram, the negative input goes through both op-amps whereas the positive signal path only goes through one. This results in different phase response between the positive and negative inputs and results in lower CMRR as frequency increases.

This type of instrumentation amplifier is usually used in lower performance systems. Most of the new product development for this type of device is being done on the CMOS process.

"Three" Op-Amp INA
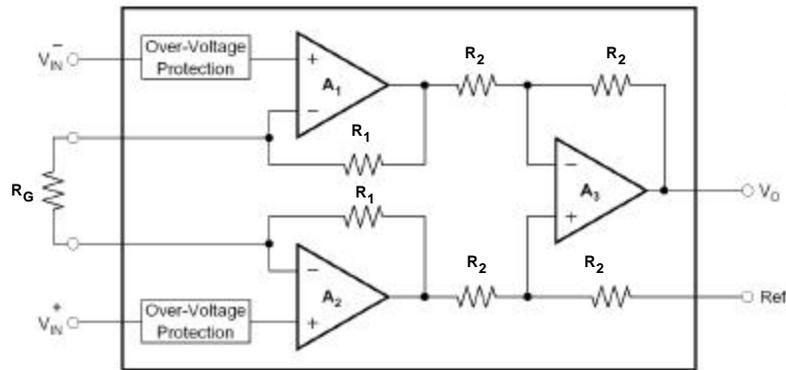
$$Gain = 1 + \left(\frac{2R_1}{R_G} \right)$$

The three op-amp INA has the highest levels of overall performance available today. Voltage gains of 1 to 10,000 V/V are achievable. It does not suffer from the CMRR vs. frequency limitations of the two op-amp approach. In fact, the three op-amp INA rejects 60Hz common mode noise 10 to 20 times better than does the two op-amp version.

Finally, since this device is intended for high end signal acquisition it is common for additional features to be included in its design, such as over voltage protection.

The three op-amp INA is currently offered on the Bipolar, JFET, and *Difet* semiconductor processes. Hence there exist a wide choice in terms of DC and AC performance parameters.

The "Current Mirror" INA

$$Gain = \left(\frac{2R_2}{R_1}\right)$$
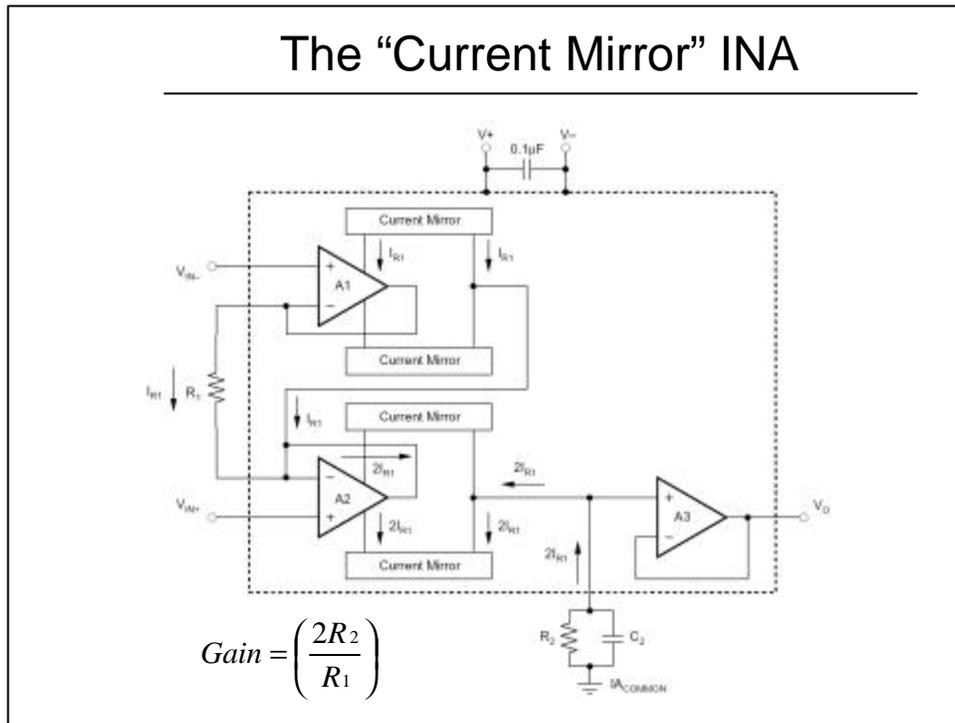
The current mirror INA, the INA326, is the latest innovation in instrumentation amplifier design. While all previous INA topologies were based on voltage gain and feedback, this device uses the current that is generated as a result of the input differential voltage divided across the gain setting resistor R_1 as the main feedback signal.

The principal of operation is fairly straightforward. First of all, the front end of the amplifier is internally powered by a pair of charge pumps. This allows input voltages to actually exceed the rails by 20mV. The input voltage impressed across R_1 generates current I_{R1}.

I_{R1} is mirrored and ultimately multiplied by a factor of two. The resulting current is drawn across R_2 resulting in the gain equation shown above.

Another feature of this type of INA design is the ability to easily implement low-pass filtering. A capacitor can be placed in parallel with R2, causing the gain of the INA to decrease with frequency. This is particularly useful when anti-aliasing or noise reduction is desirable in the application.
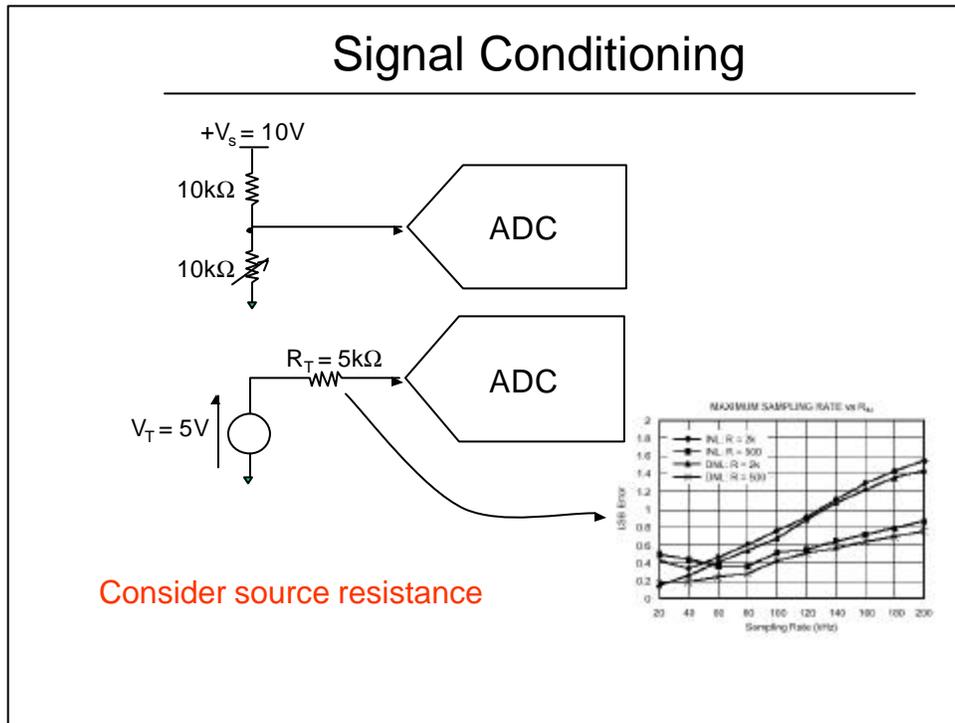
Like the CMOS op-amps that the INA326 is based on, rail-to-rail performance is excellent. This makes it an excellent choice for driving single supply CDAC data converters. Also since the input is very high impedance almost any signal source can be interfaced to it.

Instrumentation Devices

Device	CMRR (dB)	Bandwidth (MHz)	Non-Linearity (%)	Offset Voltage (μV)	Gain Range (V/V)
INA129	120 (G = 100)	0.2 (G = 100)	0.002	50	1-10,000
INA148	70	0.1	0.001	5,000	1
INA154	80	3.1	0.001	750	1
INA169	100	4.4	0.1	1,000	200μA/V
INA170	100	0.4	0.1	1,000	200μA/V
INA326	100 (G = 100)	1 (kHz) (G = 100)	0.5	0.125	0.1-10,000

Signal Conditioning

$+V_s = 10V$

$10k\Omega$

$10k\Omega$

ADC

$R_T = 5k\Omega$

ADC

$V_T = 5V$

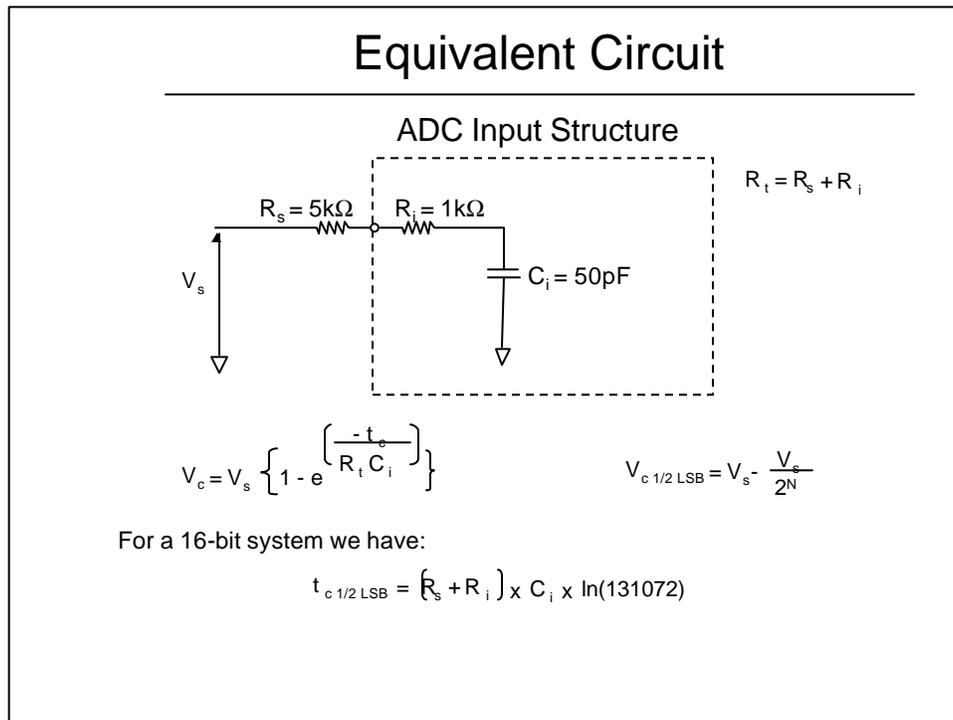MAXIMUM SAMPLING RATE vs R_{AJ}

Consider source resistance

Now that we've considered using an amplifier to bring the signal from our sensor into the optimal voltage range for our converter, let's consider what the ADC really wants to see in an input op amp.

Consider the case above. We're measuring a variable (e.g. temperature, pressure) whose value is directly proportional to a resistance.

We model this system by taking the Thevenin equivalent voltage and resistance as shown. You can see from the diagram (although it is obvious), that a higher source resistance will equate to a longer time constant.

Therefore, the time it takes for the input signal to charge the capacitor array inside the ADC to an acceptable level (< 1/2 LSB) will increase.

Equivalent Circuit

ADC Input Structure

$R_t = R_s + R_i$

$R_s = 5k\Omega$ $R_i = 1k\Omega$

V_s

$C_i = 50pF$

$$V_c = V_s \left\{ 1 - e^{\left(\frac{-t_c}{R_t C_i} \right)} \right\}$$

$$V_{c\,1/2\,LSB} = V_s - \frac{V_s}{2^N}$$

For a 16-bit system we have:

$$t_{c\,1/2\,LSB} = \left(R_s + R_i \right) \times C_i \times \ln(131072)$$

Using this equivalent circuit, we can write down an expression for the time required to charge the analog input capacitance from 0v to V_s, to within 1/2 LSB.

We can equate both these expressions and solve for t_c for a 16-bit system.

In this example, it would take around 3.5 μs for the analog input to charge to within 1/2 an LSB.

Now, consider the case if the source resistance were very small, due to an op amp driving the ADC. Say R_s was 100Ω. In this case the time taken for the analog input to charge to within 1/2 LSB is now 0.65 μs. A five-fold improvement.

The point of this analysis is to demonstrate that the source resistance the ADC "sees" is one of the few variables that you can influence.
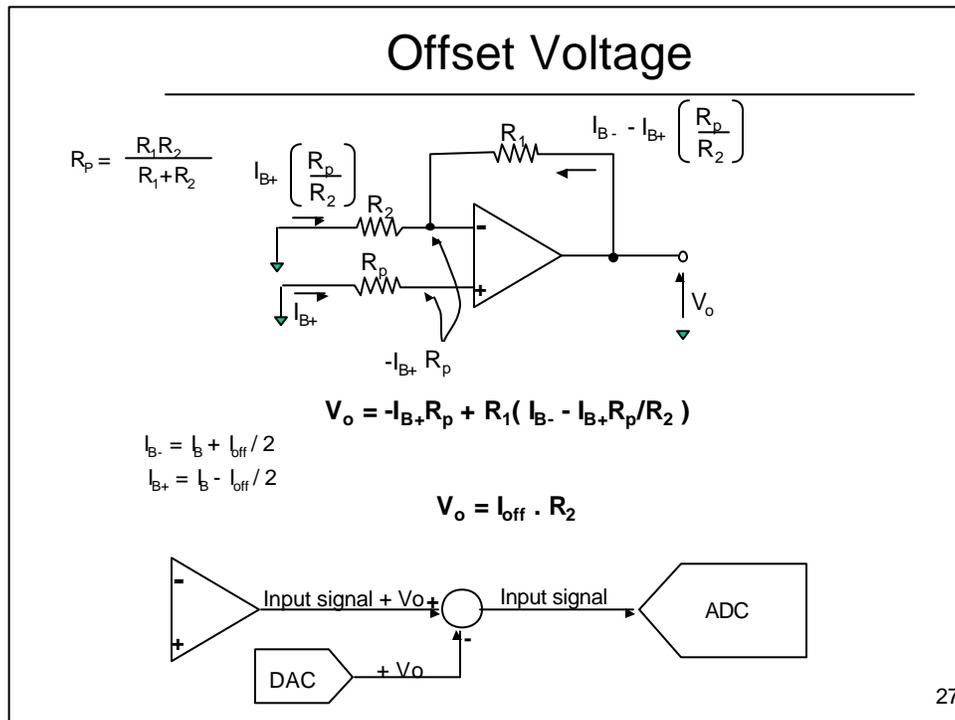
All systems should include a signal-conditioning amplifier to ensure best performance possible.

Selecting the Right Amplifier

◆ Calculate the DC error budget.
- Output error voltage
- Gain accuracy

◆ Is noise at an acceptable level?

◆ Ensure that the harmonic distortion of the amplifier does not limit the system's dynamic range.

◆ Make sure the amplifier's settling time is compatible with the ADC's sampling time.

When selecting an amplifier to drive an ADC, there are a number of points that should be considered:

- Calculate the DC error budget
    - Output error voltage
    - Gain accuracy
- Is noise at an acceptable level?
- Ensure that the harmonic distortion of the amplifier does not limit the system's dynamic range.
- Make sure the amplifier's settling time is compatible with the ADC's sampling time.

Offset Voltage

$$R_p = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_o = -I_{B+}R_p + R_1(\ I_{B-} - I_{B+}R_p/R_2\ )$$

$$I_{B-} = I_B + I_{off}/2$$
$$I_{B+} = I_B - I_{off}/2$$

$$V_o = I_{off} \cdot R_2$$

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The offset voltage is the voltage that an amplifier will output even if the input is grounded. It is small, but can be significant if the absolute error is important in your application. To minimize the effect of input bias currents a resistance (R_p) equal to the dc resistance seen by the inverting terminal can be placed at the non-inverting terminal. If there are offset currents for I_{B+} and I_{B-} as shown in the slide, the output voltage (offset voltage) can be shown as a function of the offset current.

The offset voltage becomes significant in a 16-bit system at +5 V when 1/2 LSB error is only 38 μV.

Using a chopper-stabilized instrumentation amplifier or a CMOS auto-zero amplifier, as discussed previously, can also minimize input offset voltage.

If you must consider removing an input offset voltage, there are two commonly accepted ways.

• Use a summing configuration and trim-pot (or DAC) to remove the unwanted offset voltage.

This is acceptable if the voltage drift versus temperature is small.

OR

• A software routine can make a measurement, assuming 0-V input, and use the converted value as a digital offset which can be applied to every reading

Gain Accuracy—16-Bit Resolution

$$E_{DC} = \frac{1}{|A_o b|}$$

$$E_{DC} = 1 \text{ LSB} = \frac{1}{2^{16}} = 0.000015$$

$$A_o = \frac{1}{0.000015 \times 0.5}$$

$$A_o = 133,333 = 102.5 \text{dB}$$
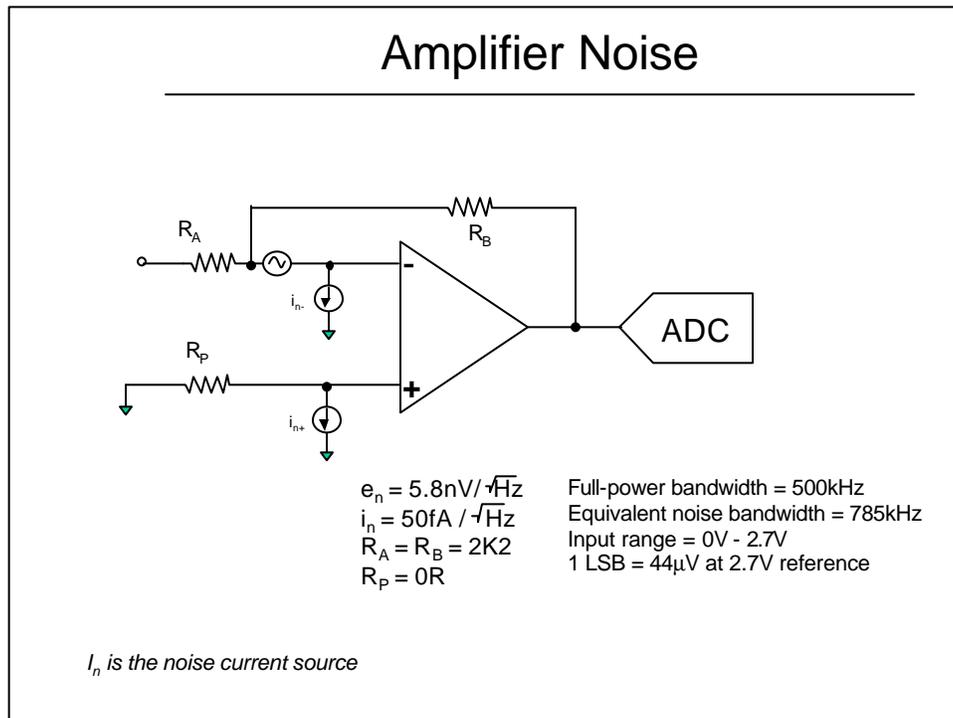
16-bit resolution requires 102.5 dB loop gain

Next, we must consider the gain accuracy of the amplifier.

In some applications gain accuracy is important. You can use the finite dc open-loop gain specification, A_o, and the feedback factor, β, to calculate the closed-loop dc gain error (e_{DC}) of a voltage-feedback amplifier from the above approximation.

In the case of a 16-bit system, $e_{DC} = 0.000015 - (0.0015\%)$

In a unity gain configuration, such as the configuration on the previous page, $\beta = 0.5$; therefore, the dc open loop gain must be at least 133,333 (102.5dB).

Amplifier Noise

$e_n = 5.8nV/\sqrt{Hz}$
$i_n = 50fA/\sqrt{Hz}$
$R_A = R_B = 2K2$
$R_P = 0R$

Full-power bandwidth = 500kHz
Equivalent noise bandwidth = 785kHz
Input range = 0V - 2.7V
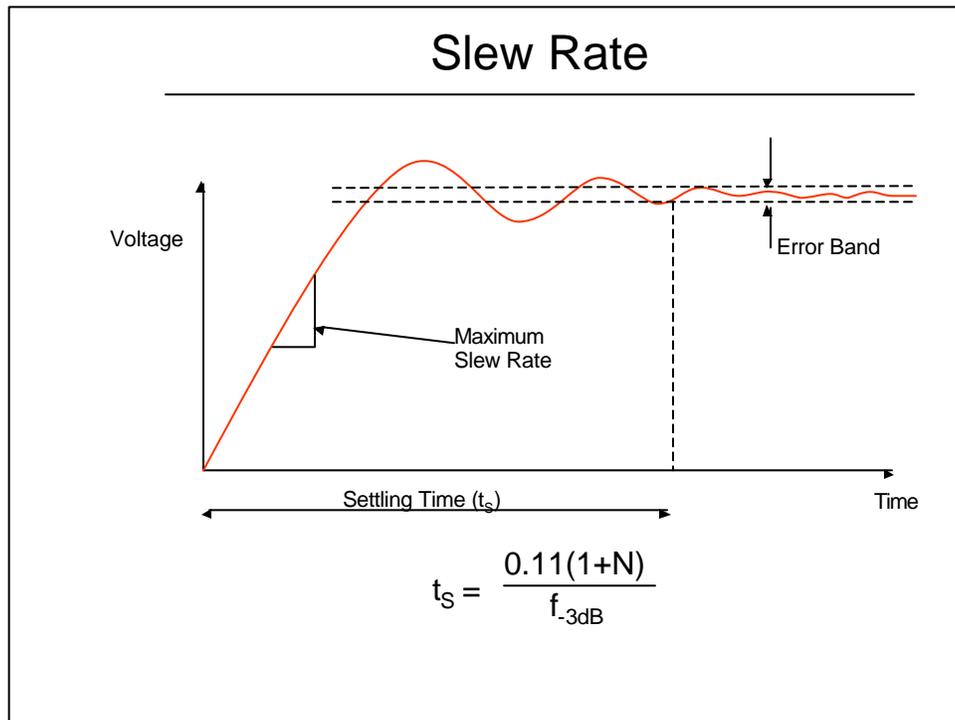1 LSB = 44µV at 2.7V reference

I_n is the noise current source

We can now discuss some of the important AC parameters. This amplifier is shown in a unity-gain configuration. For voltage-feedback amplifiers we can make the assumption that $i_{n+} = i_{n-} = i_n$.

A good rule of thumb is to try to keep the op amp's rms noise at the ADC's input to less than the theoretical rms quantization noise of the ADC. We've already discussed this value--it's q / sqrt(12). For a 16-bit ADC working at 2.7 V, q = 41 µV and the theoretical rms quantization noise is 11.9 µV.

Plugging these numbers into the equation we arrive at a value for the total rms noise contributed by the op amp of 10.3 µV.

Slew Rate

Voltage

Maximum
Slew Rate

Error Band

Settling Time (t_s)
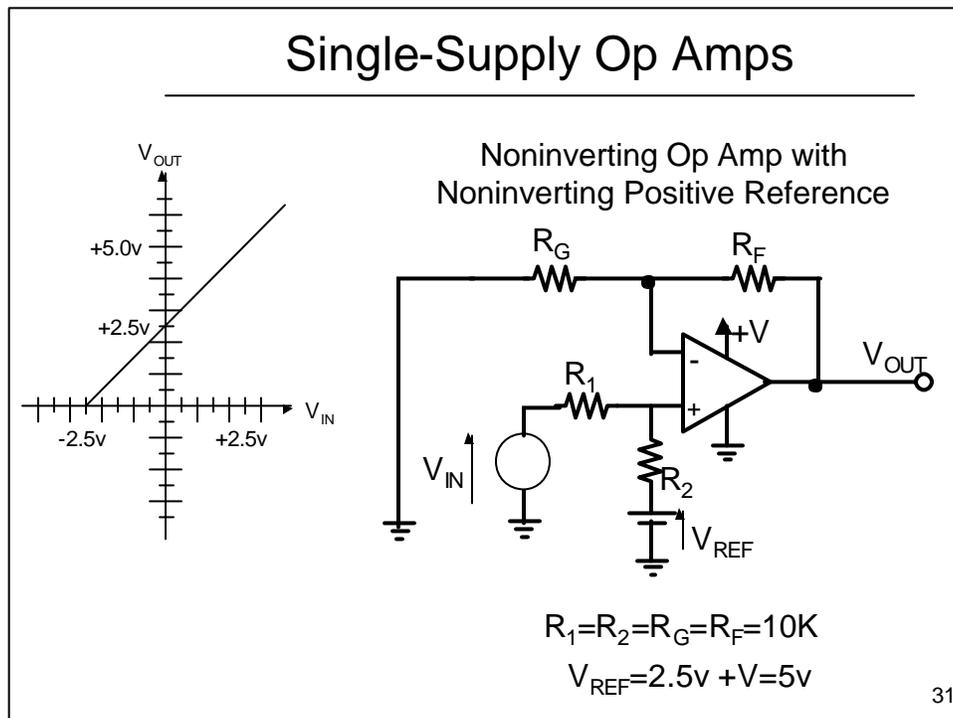
Time

$$t_S = \frac{0.11(1+N)}{f_{-3dB}}$$

There is a limit to the rate at which the output voltage of an operational amplifier can change; the slew rate is the parameter used to quantify this effect. Slew rate is the maximum rate of change of output produced in response to a large input.

The basic mechanism governing slew rate is capacitor charging. The rate of change of voltage at any point in a circuit being limited by the maximum current available to charge the capacitance at that point.

Slew rate will be important to you if the amplifier's output signal cannot settle to within an accepted error band (usually 1/2 LSB) before the next ADC sampling period.

We can use the formula above to make a first-order approximation of settling time, if we know the amplifier's 3-dB corner frequency, and assuming that the input signal doesn't cause the amplifier to be slew-rate limited.

Single-Supply Op Amps

Noninverting Op Amp with Noninverting Positive Reference

$R_1 = R_2 = R_G = R_F = 10K$

$V_{REF} = 2.5v \quad +V = 5v$

31

Portable equipment tends to operate from a single-supply. The drive toward single-supply op amps is fuelled by the available power sources; which, in portable applications, is typically a battery.

The above shows an example of how to arrange a single supply system to turn an input signal of ± 2.5v into a 0 - 5v signal which feeds an ADC.

Care must be taken when applying a negative input voltage to an op amp powered from a positive supply, since op amp inputs are susceptible to reverse-voltage breakdown - some sort of input protection (typically a diode) should be used to ensure no fault condition.

Details regarding single-supply op amp circuits can be found in the application report *Single-Supply Op Amp Design Techniques*.

http://www-s.ti.com/sc/psheets/sloa030a/sloa030a.pdf

Potential problems that should be considered are:

• Output voltage is limited

• Potential common-mode issues

Voltage Reference

◆ Stable

◆ Two different technologies
- Bandgap
- Buried zener

If you're going to use a SAR ADC, then you will also have to plan for a voltage reference circuit. There's really only one main characteristic that a voltage reference should possess--it should be very, very STABLE!!

The ideal reference will be stable to the required accuracy, with time, temperature, input voltage and load current.

The reference establishes the full-scale range of the ADC; the overall dc accuracy and stability can be no better than that of the voltage reference.
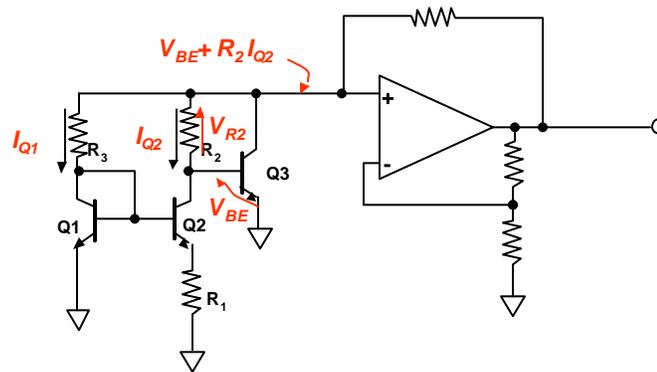
There are two types of reference available. These are:

- Bandgap Reference

- Buried-Zener Reference

The choice of which reference to use is very important.

We will give a brief overview of both the bandgap and buried zener, comparing their strengths and weaknesses, and completing References with a proposed circuit.

Bandgap Voltage Reference

Stable over temperature (2-3 ppm/ºC)

In this basic example, the current mirror provides a constant current through R_3. Since this is a current mirror, a proportional current will also be generated through Q_2.

The voltage generated due to the current flowing in Q_2 is proportional to the value of R_2. If the voltage generated by R_2, V_{R2}, has a positive temperature coefficient, we can compensate for temperature variations due to the negative temperature coefficient of Q_3's V_{BE} .

This leads to a voltage reference that is very stable over temperature around 2-3ppm/ºC. However, devices based on this technique are not as accurate nor stable as the best buried-Zener references.

Buried Zener Voltage Reference
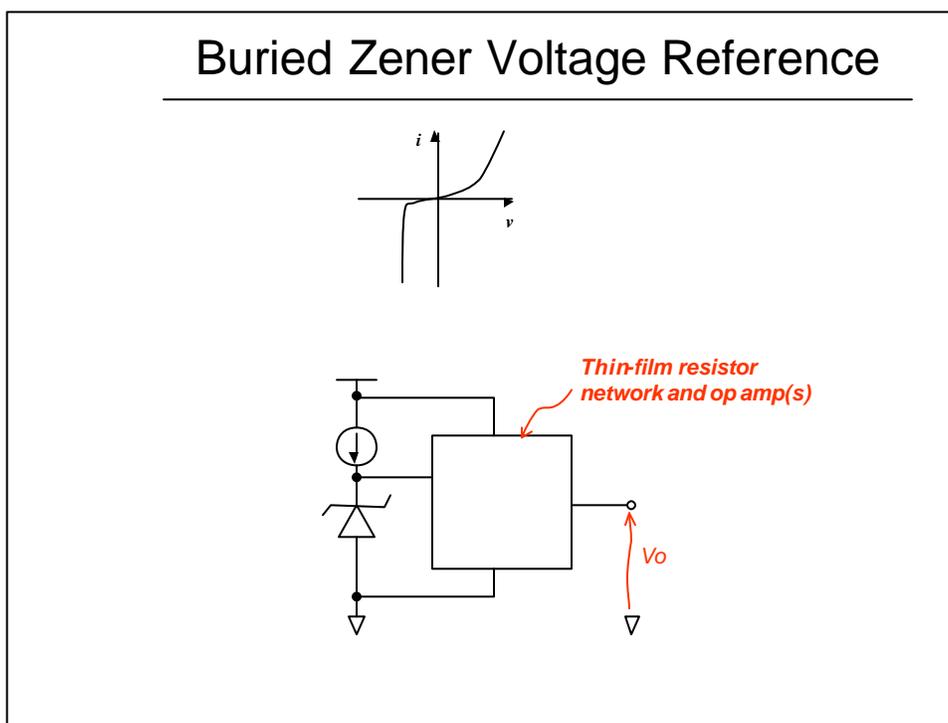
Zener diodes operate in the breakdown region. The breakdown region is entered when the reverse voltage exceeds a threshold value specific for that particular diode. The breakdown is not destructive if the power dissipated in the diode is limited by external circuitry. The voltage is set during manufacture by controlling the density of the doping of the two regions of the junction; the heavier the doping the lower the breakdown voltage.

In order to produce a stable voltage the device must draw a steady current (1.4 mA in the the case of the REF02)—bearing in mind the portable nature of a data logger, it's a factor to be aware of during the component selection phase.

Surface zeners are subject to mechanical stresses and impurities which tend to make their outputs noisy, so to enhance their performance we take the simple step of covering the devices with a passivation layer. These are called buried (or subsurface) zeners.

To these basic zeners, manufacturers will add active devices (op amps) and compensation networks (resistors), which can be laser-trimmed to yield a high degree of accuracy.Typically they will have an initial error of 0.01% — 0.04% and TC of 1-10ppm/^{0}C and less than 10mV$_{pk-pk}$ of noise.

A final note worth making is that these references must have a minimum supply voltage significantly larger than the output - at least 8 V for the REF02. This is an important consideration to keep in mind for portable applications, since to generate 8 V from a 5-V supply will require a converter, adding to your power budget.

Buffered Voltage Reference
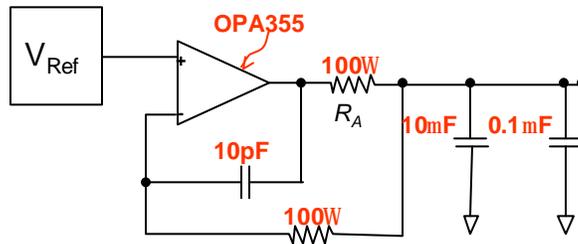
Because noise from the reference causes its output voltage to appear "non-stable" (not perfectly DC), regardless of the type of voltage reference, it's good practice to filter the output before presenting it to the ADC.

Select a precision, low-noise amplifier - like the OPA355 to provide the active filter. The large load capacitor (10 μF) serves two purposes.

- Forms a lowpass filter with R_A to create a corner frequency of around 160 Hz. This filtering reduces the op amp's output noise to a negligible value.

- Provides additional reference voltage stability by acting as a charge reservoir to any transient load current.

The 0.1-μF capacitor in parallel with the 10-μF capacitor keeps the output impedance low at high frequencies, where the 10-μF capacitor becomes less effective.
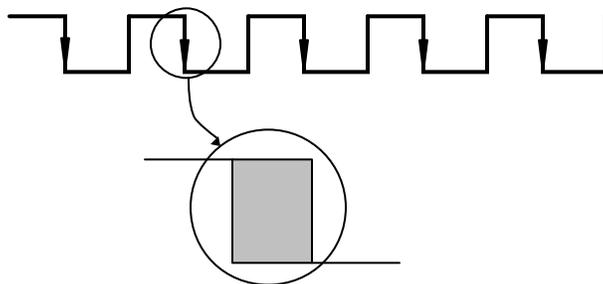
The 10-pF capacitor assures stability of the op amp.

Check-out the application note "*Voltage Reference Filters*" AB-003A for more details.

http://www-s.ti.com/sc/psheets/sbva002/sbva002.pdf

Sample Clock Generator

Sampling jitter is the error in the placement
of each clock edge controlling the point
when sampling begins.

Sampling jitter is also an important point that should be considered
during the design phase – although there may be little that you can do to
influence it.

The effect of jitter is to set a limitation on the maximum frequency of
input sine wave, because it defines the maximum slew rate of that
signal.

Sample Clock Generator

$$\text{S/N ratio} = 20 \log_{10} \left\{ \frac{1}{2\pi f\, t_A} \right\}$$

S/N ratio at 100KHz

S/N ratio at 500KHz
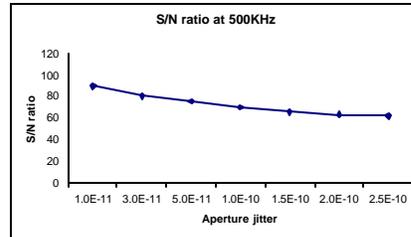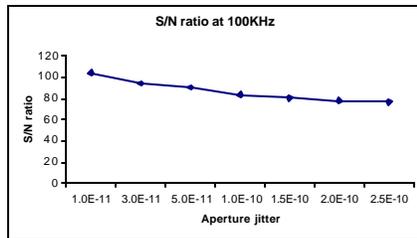
Sampling jitter is the rms value of the sample-to-sample variation in the time the ADC samples the input signal.

This rms time jitter produces a corresponding rms voltage error that's proportional to the slew rate of the ADC's input signal. You can approximate the rms S/N ratio of the jitter by the formula above.

The consequences of jitter are illustrated in the diagrams for the S/N ratio at two different frequencies. For a given input frequency, if the jitter increases the S/N ratio decreases.

In most real-world cases, unwanted external sources often modulate the phase or amplitude of the sampling clock. These sources can be wideband random noise, oscillator phase noise, power-line noise, or digital noise due to poor layout, bypassing or grounding techniques.

For most people the sampling clock used will come from either a crystal oscillator or be derived from a host processor.

Consider providing a low-pass (RC) filter after the oscillator to remove any harmonics present in the signal. In some cases, a small valued resistor is good enough. This reduces overshoot and makes the signal less prone to radiate noise.

Layout at this point is important too. Don't let the digital outputs of the ADC couple into the sampling-clock signal. Coupling may cause an increase in the harmonic distortion of the ADC by allowing digital transients into the sampling clock. Conversely, the sampling clock is itself a digital signal, therefore it has the potential for causing noise in the analog portion of the system.

Take steps to isolate the sampling clock and consider its routing very carefully. Perhaps even making sure you have a Faraday shield around the trace.
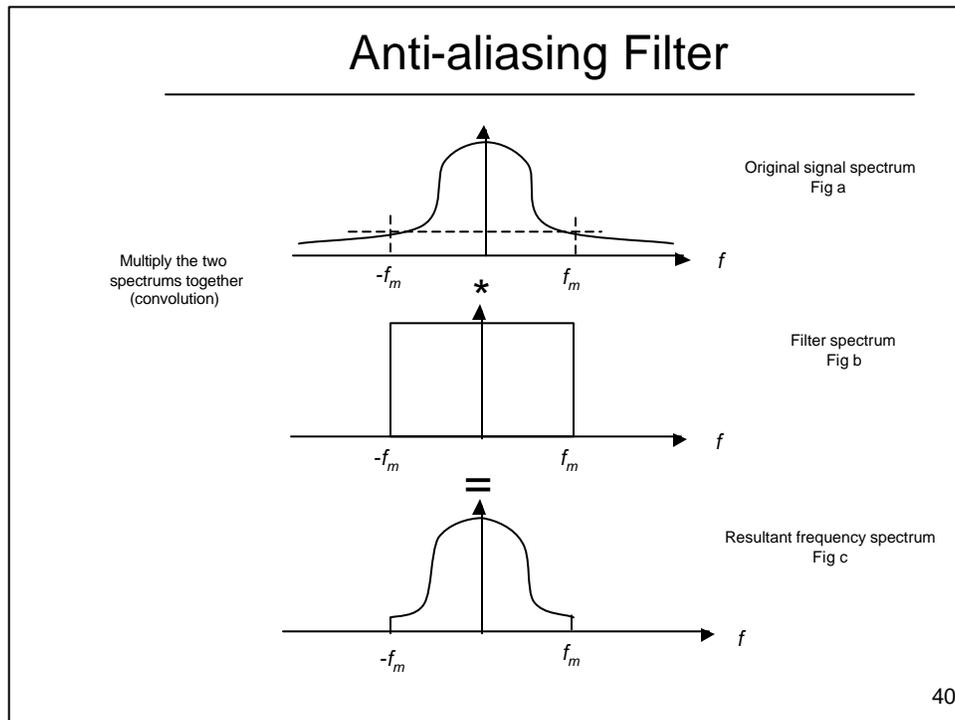
Aliasing

Figure a

Figure b
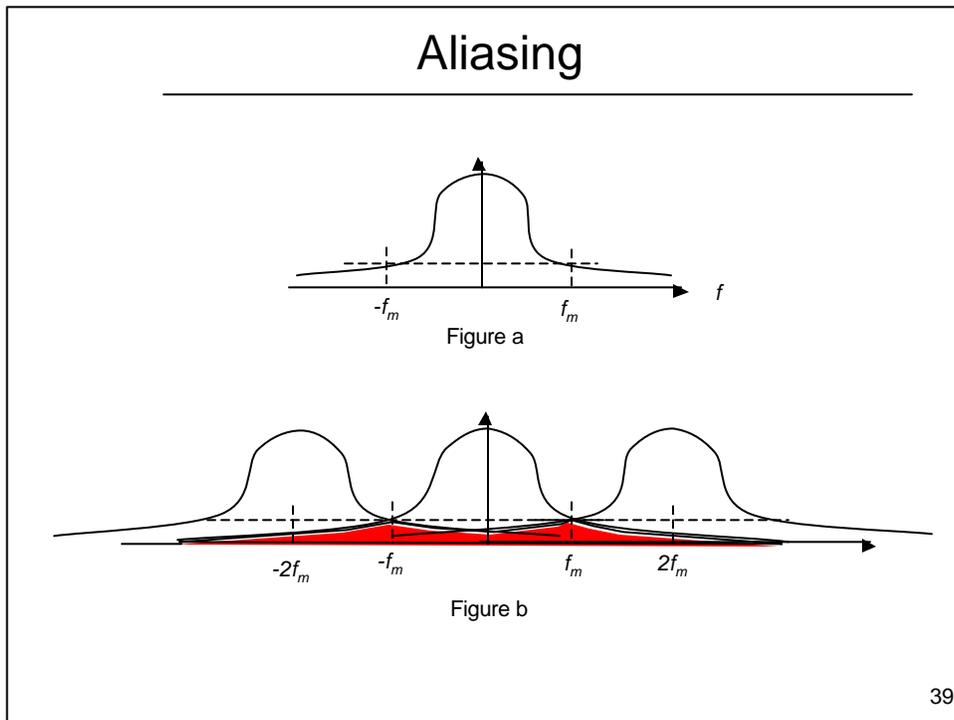
39

The final circuit we discuss is the anti-aliasing filter.

In the real world we rarely come across a pure sine wave. Typical signals have a wide spectrum of components, which we can show above - fig. a. Information above or below a certain frequency, is usually considered surplus. Assuming that f_m is the maximum frequency of interest, we would like to sample at a rate of f_s, where $f_s = 2f_m$.

If we do this, and look at the frequency spectrum, as shown in figure b, we can see that the bands will overlap and produce aliasing in the output signal. To avoid this we must first use a low-pass filter to remove any frequency components above f_m.

Anti-aliasing Filter

Original signal spectrum
Fig a

Multiply the two
spectrums together
(convolution)

Filter spectrum
Fig b

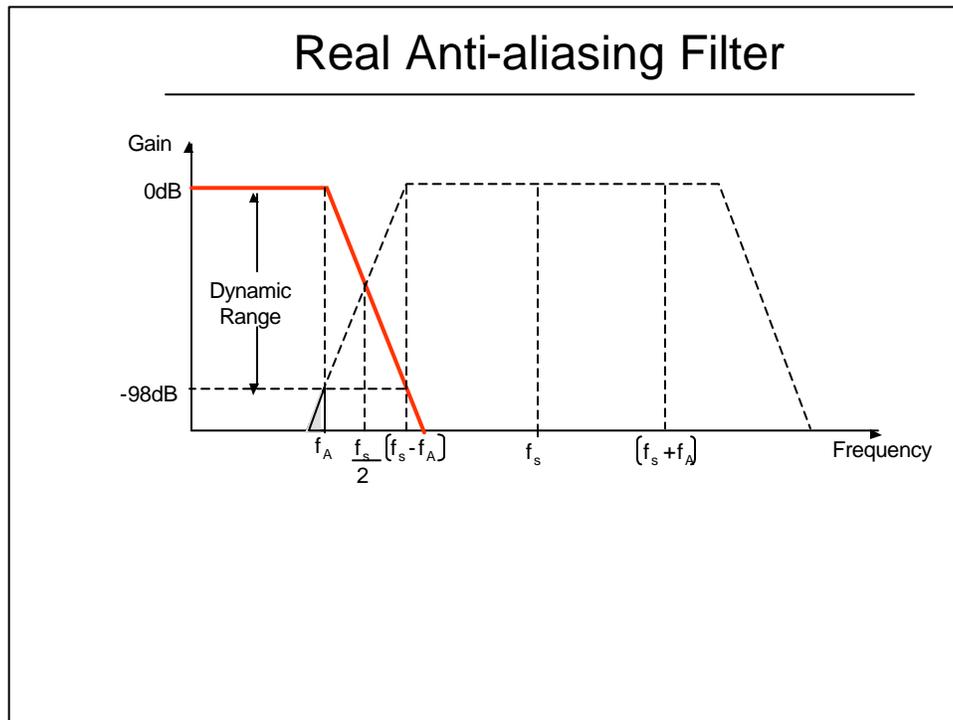Resultant frequency spectrum
Fig c

40

In applications such as would require an anti-aliasing filter, the signal's spectral characteristics and the system's dynamic-range requirements must be completely understood before beginning.

The characteristics of an ideal anti-aliasing filter are shown above fig b. It should be flat over the pass-band and zero at all other points in addition to having a linear phase response.

For example, in a control system, if the filter is not designed properly, there will be frequency components that get through to the ADC. Since the ADC's sampling rate is fixed, the frequency components above 2xNyquist show-up and are digitised by the ADC. The control system will spend more time compensating for the poorly designed filter than actually performing the control task.

Real Anti-aliasing Filter

Gain

0dB

Dynamic
Range

-98dB

f_A $\dfrac{f_s}{2}$ $\left(f_s\text{-}f_A\right)$ f_s $\left(f_s\text{+}f_A\right)$ Frequency

A real-world anti-aliasing filter will have some rolloff characteristic, and some aliasing may still occur. The filter used then must sufficiently attenuate the out-of-band signals so that their aliased components are below the noise floor of the ADC. Not doing so will degrade the dynamic range in the frequency range of interest available from the ADC.

For a 16-bit system, remembering that SNR = 6.02n + 1.76 dB, we arrive at an SNR of around 98 dB.

In applications that require an anti-aliasing filter, the signal's spectral characteristics and the system's dynamic-range requirements must be completely understood before beginning.

Support Circuit Summary

◆ Signal conditioning circuitry

◆ Reference voltage generation

◆ Sampling clock

◆ Anti-aliasing filter

These are the four areas we considered important to support the ADC and ensure that you will achieve your design goals.

Signal conditioning amplifier
Useful for matching the dynamic range of the sensor to the maximum range of the ADC. This will enable a larger voltage reference to be used and a bigger step-size. Other benefits include low-output impedance - important for SAR converters.

Voltage Reference

The system cannot be any more stable than the reference voltage allows. There are two main types in use—the Buried Zener and the Bandgap. Buried Zeners are more stable, but require a higher voltage to operate properly. Bandgaps don't require a higher voltage source and have excellent temperature compensation schemes.
Due to the dynamic nature of a CDAC in any SAR converter, an active device (operational amplifier) in the circuit maintains a constant voltage to the reference. The topology presented represents the recommended circuit for a SAR.

Sampling clock
Use a series resistor to tune edges – be careful with the layout.

Anti-aliasing filter

An anti-aliasing filter may be necessary to achieve full bandwidth.

Converter Interfaces

◆ Serial Interface
  ■ Microcontrollers
  ■ Digital signal processors
◆ Parallel Interface
  ■ Digital signal processors
  ■ Microcontrollers
◆ I^2C Interface
  ■ Digital signal processors
  ■ Microcontrollers

Converter Interfaces

Now let's consider your interface options.

Analog-to-digital and digital-to-analog converters support the glueless interface to digital signal processors, microcontrollers and FPGAs.
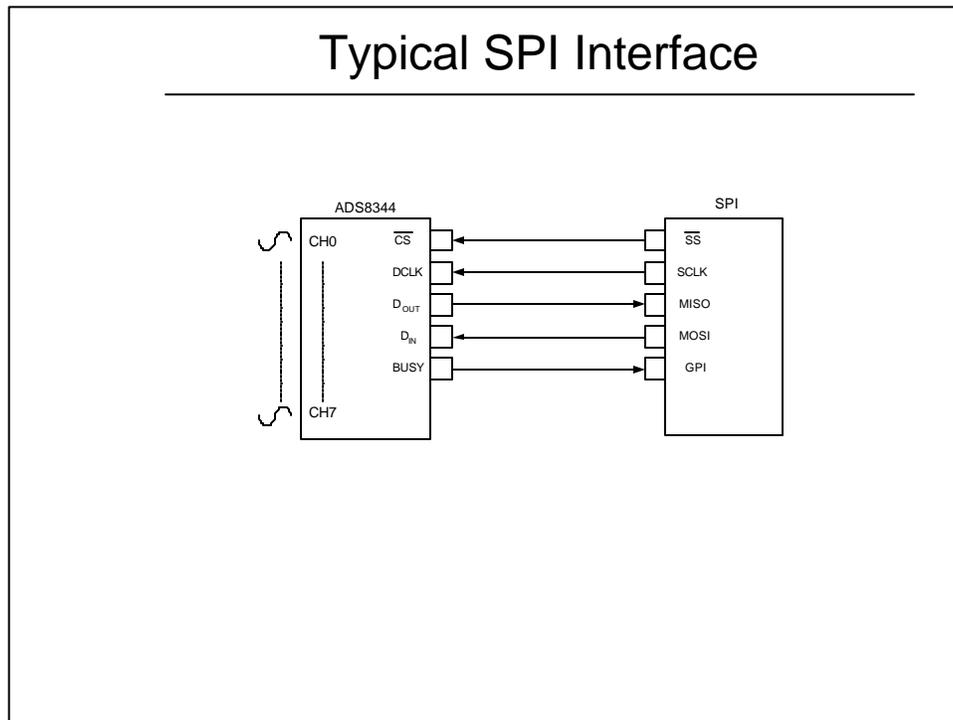
We'll take a look at serial, parallel and I^2C types of interfaces.

Many people are familiar with SPI interface, so that's what we'll focus on first.

We'll then briefly mention the serial port you'll encounter with TI's DSP the Multi-channel Buffered Serial Port (McBSP).

Next we'll look at interfacing parallel A/Ds to DSPs and Microcontrollers. Finally, we'll end this section a with quick look at the I^2C interface.

Typical SPI Interface

ADS8344		SPI	
CH0	$\overline{CS}$	$\overline{SS}$	
	DCLK	SCLK	
	D_{OUT}	MISO	
	D_{IN}	MOSI	
	BUSY	GPI	
CH7			

This is the simplest way to connect your ADC and host system together. In this case Chip Select is connected to the Slave Select pin of the processor. DCLK is connected to serial clock (SCLK) pin. Data out (Dout) pin is wired to Slave out Master In (SOMI) pin. Likewise, Data In is connected to Slave In Master Out (SIMO) pin. The Busy pin is shown tied to a general-purpose input here because not all processors have programmable edge-sensitive interrupt circuits. The MSP430F1149, 68HC11 microcontrollers and F2407 and C6000 family of DSPs posses these edge-triggered interrupt circuits.

What is the McBSP?

◆ Based on standard serial port of TMS320 DSPs

◆ Direct interface to ADCs, DACs, CODECs, AICs.

◆ Full-duplex communication. Double-buffered transmit and triple-buffered receive data registers

◆ Direct interface to T1/E1 framers, IOM-2, AC97, MVIP switching, ST-BUS, IIS and SPI-compliant devices.

◆ Multichannel transmit and receiver up to 128 channels

◆ Data sizes 8-, 12-,16-, 20-, 24- and 32-bits

◆ µ-Law and A-Law companding

The multi-channel buffered serial port (McBSP) is a superset of the standard serial ports found on Texas Instruments' digital signal processors (DSP). It enables the DSP to interface to many of the popular serial interfaces, including SPI-compatible devices.

In addition to features found on the previous serial-port interfaces, the McBSP is able to directly interface to TI/E1 framers, IOM-2-compliant devices, MVIP switching-compatible, ST-BUS-compliant devices, AC97-compliant devices, IIS -compliant devices, and SPI devices.

It provides a wide selection of transmit/receive data sizes, µ-Law and A-Law companding, programmable polarity for both frame synchronization and data clocks, and highly programmable internal clock and frame generation.

This serial port enables engineers to directly interface TI DSPs to most ADCs, DACs and CODECs on the market.

It provides full duplex communication.

It allows the transmitter and receiver sections to be used independently of the other.

Data sizes are programmable from 8-bits up to 32-bits.

Serial Interface to McBSP
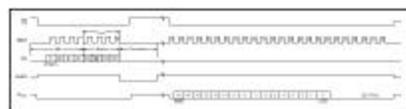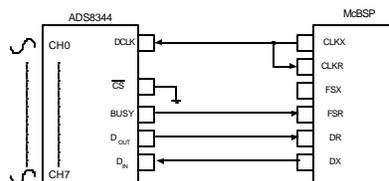

Figure 1

Figure 2

Figure 3

The ADS8344 is a 16-bit 100-kSPS analog-to-digital converter.

Because McBSP is so flexible, there are a couple of ways to interface this part to TI's DSP. The easier and more frequently used interface is shown here. We'll assume that there's only one device on the serial bus.

The device's chip select pin can therefore be tied low.

Data clock is tied to CLKX and CLKR of the McBSP. BUSY signal is tied to receiver frame sync pin (FSR). Data Out and Data In pins are tied to Data Receive (DR) and Transmit (DX) pins, respectively.

Normally in this type of DSP interface FSX is connected to some kind of frame sync pin on the converter. We can leave that pin not connected, because the converter uses the start bit in the command word in place of the frame sync signal. The busy signal, in external clock mode, acts like a frame sync signal. Therefore, we tie that to FSR.

If your application requires the use of the internal clock mode, you can see from Figure 2 that it doesn't look like a typical frame sync signal anymore. However, since McBSP is flexible, you may continue to use the BUSY as your FSR.
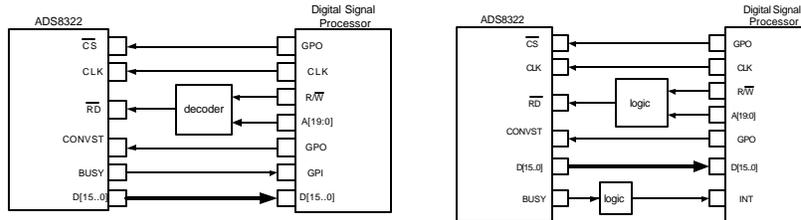
Parallel—Digital Signal Processor


Figure 1

Figure 2

Next let's take a look at the general requirements for parallel converters. In this example, the device is memory mapped in data or I/O space. Some combinational logic is required to decode the address and select the device on the bus.

In this case, there are approximately 21 wires from the converter and possibly up to 37 signals and some discrete logic involved from the processor side.

The figure above shows a typical memory-mapped device. Some address decoding logic is needed to create the read signal for the converter. In some cases additional logic is required to transform a signal like the BUSY signal into an interrupt pulse that the processor can use.
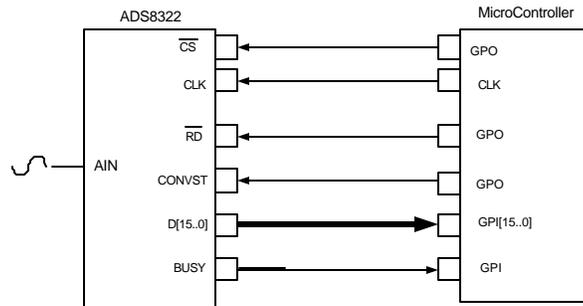
Here's an example showing the ADS8322 a 16-bit, 500-kSPS ADC.

General purpose I/O pins are programmed as outputs and can then be used to toggle the Chip-Select, Read and Convert-start signals.

General purpose I/O is programmed as input and connected to BUSY pin. Polling the BUSY pin will indicate the state of the converter in the conversion cycle.

The clock for the converter is sourced from the micro's CLK pin.

The data bus is tied to input port pins.

I2C Interface — DSPs
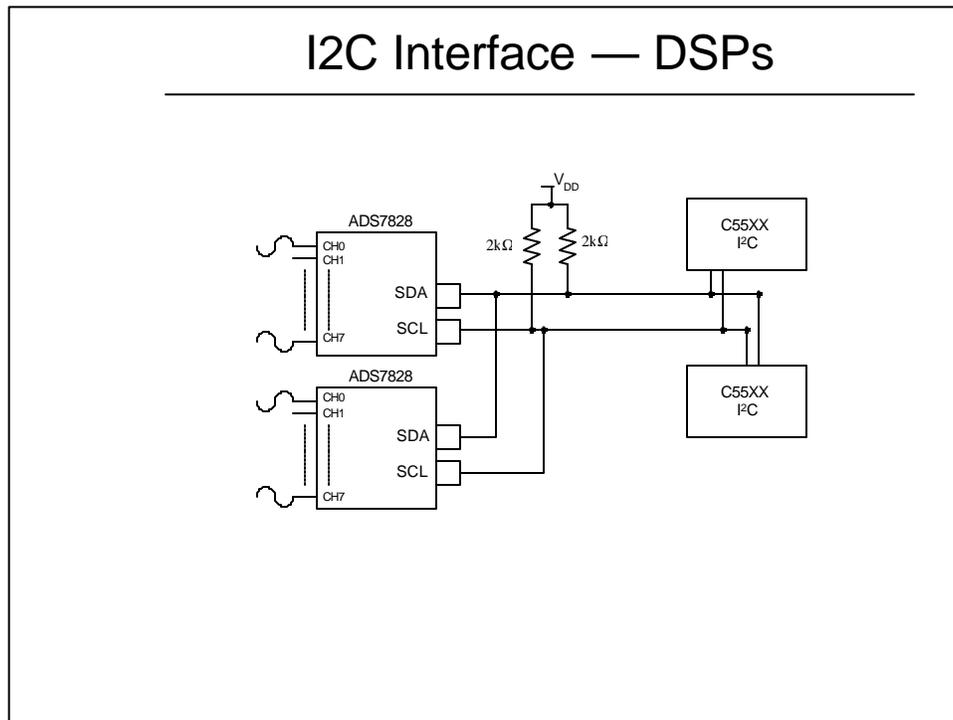
In electronic systems there are peripheral devices that must communicate with both each other and the outside world. To maximize hardware efficiency and simplify circuit design, Philips developed a simple bi-directional 2-wire, serial data (SDA) and serial clock (SCL) bus for **I**nter-**I**ntegrated **C**ircuit control, simply called I²C.

This I²C-bus supports any I²C fabrication process and, with the extremely broad range of I²C—compatible chips from Philips and other suppliers, it is the worldwide industry standard proprietary control bus.

Each device is recognized by a unique address and can operate as either a receiver-only device (e.g. an LCD driver), or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip must initiate a data transfer, or is only addressed. I²C is a multi-master bus, i.e. it can be controlled by more than one I²C connected to it.

The basic I²C bus, with a data transfer rate up to 100 kbits/s and 7-bit addressing, was introduced nearly 20 years ago.

But, as data transfer rates and application functionality rapidly increased, the I²C – bus specification was enhanced to include fast-mode and 10-bit addressing, thus meeting the demand for higher speeds and more address space.

The DSP multi-master I²C peripheral provides an interface between a TI DSP device and I²C bus-compatible devices that connect via the I²C serial bus.

The DSP I²C peripheral supports any slave or master I²C-compatible device.

The figure on the previous page shows the example of these pins for multiple C55x I²C serial ports connected for a two-way transfer from one device to other devices.

In this slide, the ADS7828 12-bit, 8-channel, 50-kSPS device is interfaced to the C55xx DSP from Texas Instruments.

See   http://www-s.ti.com/sc/psheets/spra785/spra785.pdf
for further details

I2C Interface — Microcontroller
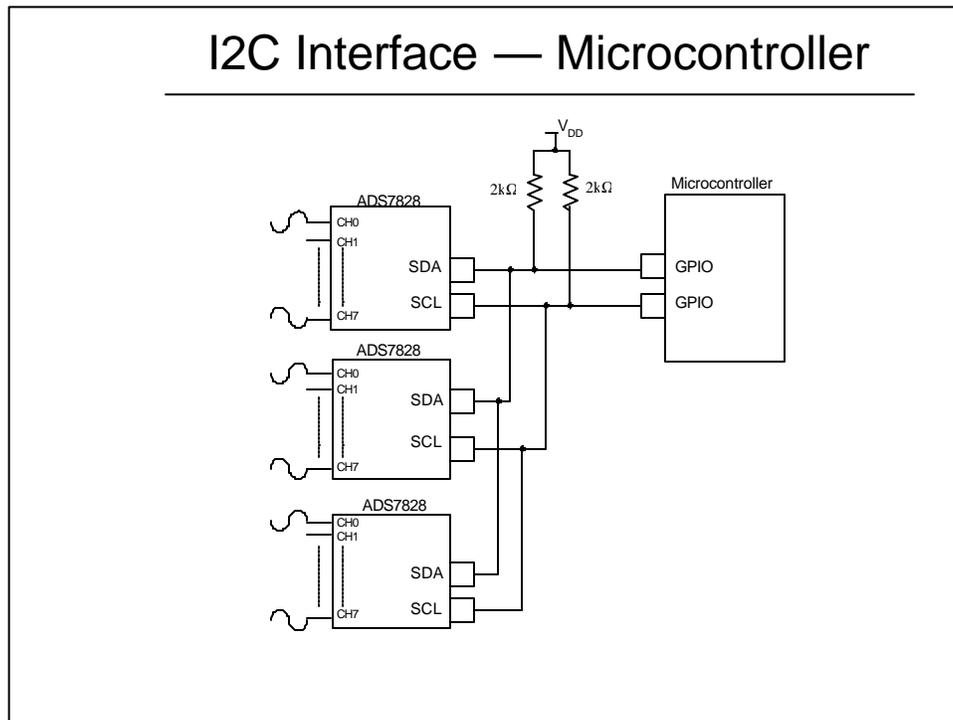
Using any two available I/O pins, microcontrollers like the MSP430 are capable of emulating the open collector operation of the SDA and SCL signals required for I2C communications.

This is accomplished by setting the output data for these two I/O pins low and using the directions setting of the pins to determine the logic level of the signal lines.

Whenever a logic high is required, the direction bit for the corresponding pin is set to configure that pin as an input.

The pull-up resistor on the signal line then pulls it to a logic high state.

If a logic low is required, the direction bit is set to switch the pin to an output.

Since the data for the pins was previously set low, the signal line will be pulled low by the pin being switched to an output.

Each device on the serial bus is addressed. The first byte sent by the master is the slave address. Only the slave addressed will return an acknowledge bit after the slave address and each received byte. The details of the I2C interface is available from Philips and in the ADS7828 data sheet.

In this slide, multiple ADS7828, 12-bit, 8-channel, 50kSPS devices are interfaced to the TI MSP430 microcontoller.
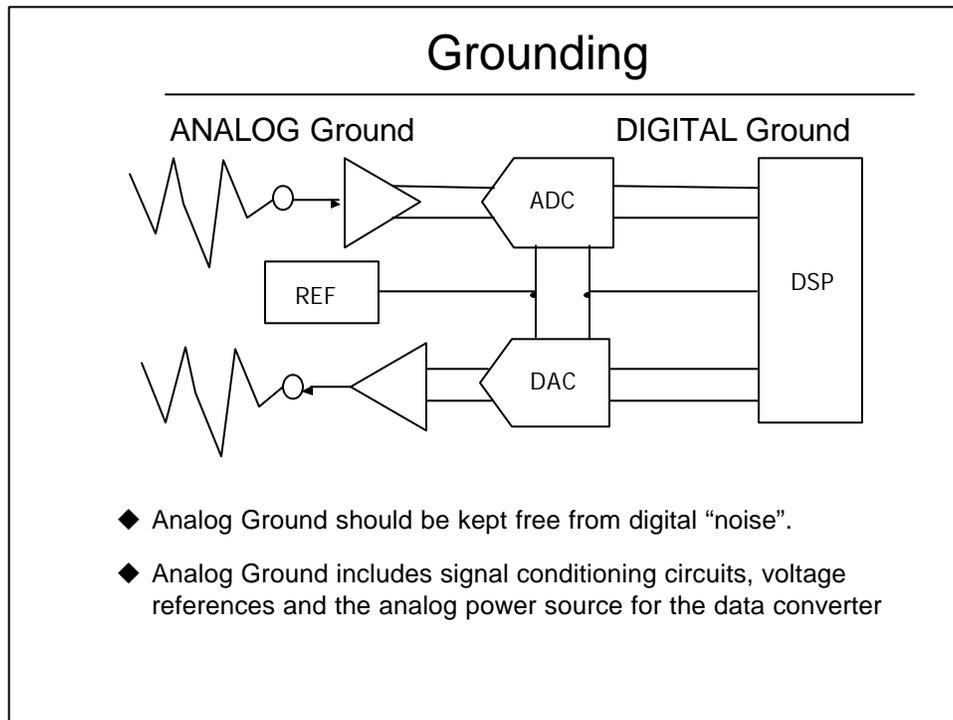
Physical Considerations

◆ Grounding

◆ Layout

◆ PWB materials

◆ Filtering

◆ Bypass capacitors

◆ Assembly

Physical Considerations

These are the areas that we will consider in providing us with a method
to manage the physical constraints of our design. We'll look at :

- Grounding

- Layout

- PWB materials

- Filtering

- Bypass Capacitors

- Assembly

Grounding

ANALOG Ground · DIGITAL Ground

◆ Analog Ground should be kept free from digital "noise".

◆ Analog Ground includes signal conditioning circuits, voltage references and the analog power source for the data converter
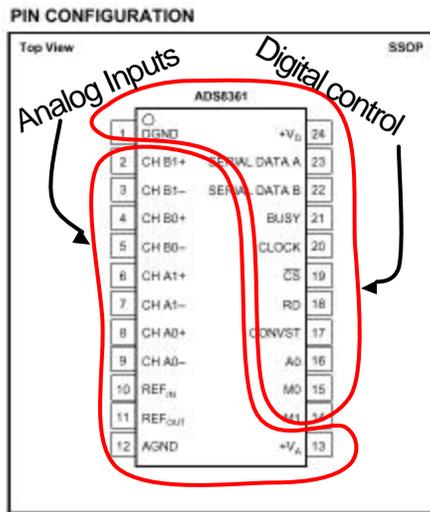
Grounding – why is it important?

As with any analog circuit, grounding considerations are critical for reliable data converter designs. For ADCs and DACs, it is essential to have a solid ground reference on the analog side of the device. This includes the analog power connections and reference connections, as well as the analog inputs. Analog ground has to be tied back to the analog inputs to reduce common-mode noise.

This does not imply, however, that the digital section can be ignored. The high currents associated with digital signals can cause ground bounce or "switching noise" which adversely affects the analog section of the data converter. A few millivolts of noise can correspond to hundreds of counts of error in a 16-bit system.

The Chip

PIN CONFIGURATION

Top View   SSOP

Analog Inputs   Digital control

ADS8361

| 1 | DGND | +V_D | 24 |
2	CH B1+	SERIAL DATA A	23
3	CH B1−	SERIAL DATA B	22
4	CH B0+	BUSY	21
5	CH B0−	CLOCK	20
6	CH A1+	CS	19
7	CH A1−	RD	18
8	CH A0+	CONVST	17
9	CH A0−	A0	16
10	REF_IN	M0	15
11	REF_OUT	M1	14
12	AGND	+V_A	13

Internally, the chip is separated into distinct analog and digital sections.

Careful planning of the layout for a high-resolution data converters actually begins long before the design engineer ever has a part in his hands.

Chip designers often spend a great deal of time and effort on the actual layout of the silicon in order to get the desired performance from the device.

The analog and digital sections are normally well defined on the actual substrate in order to minimize the effects of switching noise on the analog circuitry.
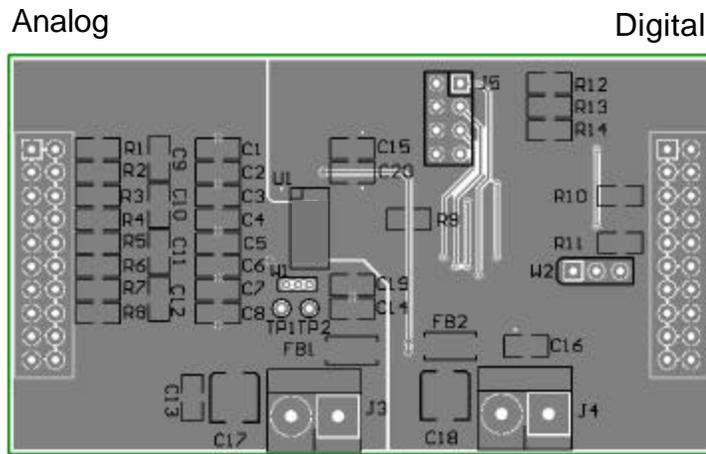
◆ Split the plane into Analog and Digital sections when
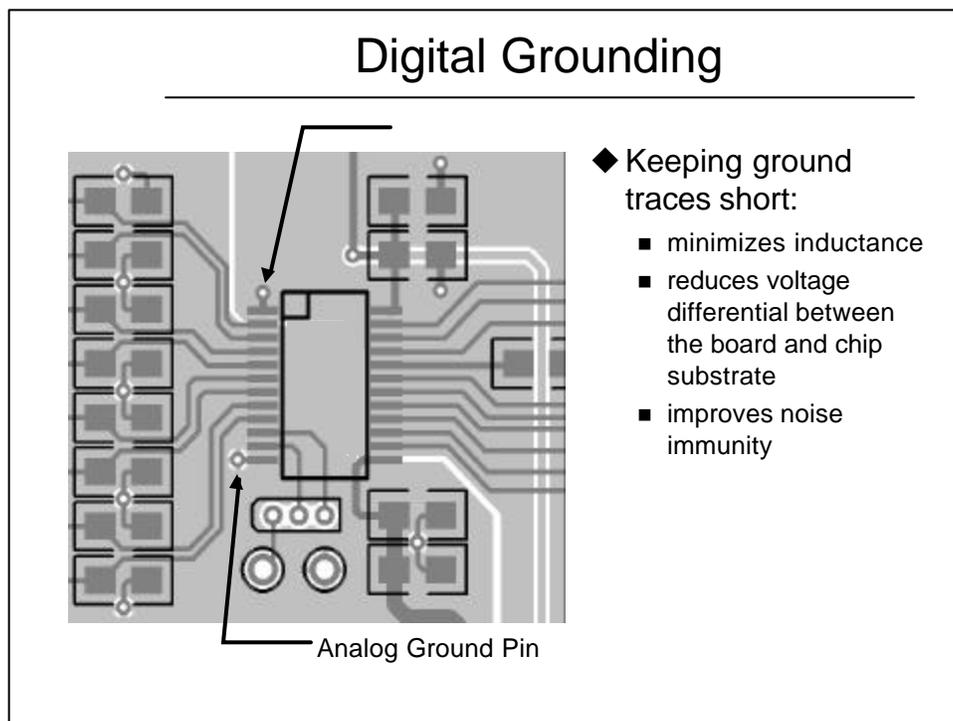the layout permits.

Split or Solid

To eliminate, or at least minimize, the effects of ground disturbances in
high-resolution systems, carefully planned ground schemes are
necessary. While people may argue as to whether a "split" ground or
"solid" ground plane provides the best performance, isolation and/or
filters between the analog and digital sections and well bypassed
connections back to the system power supply are essential.

The board depicted on this slide has a distinct analog and digital section.
This provides isolated ground structures which prevent the high-speed
digital signals from finding a return path through the analog circuitry.
However, we do provide a small ground plane underneath the actual
converter.

You don't need a solid ground plane under the ADC in all cases - very
often we put a very small (5-10mil) connection between the two under
the ADC - just so the digital return currents from the ADC can flow back
to analog side, since they are connected inside the ADC. There is no
need for a big plane here, since these currents are small.

If the split goes completely through the ADC, then you can see that those return paths have to flow all the way down the board, through the power supply, and back up through the analog plane. This is what we're trying to avoid, since now digital signals are on the analog plane, and you have a much larger loop area, increasing the inductance and raising the potential for EMI.

Digital Grounding

◆ Keeping ground traces short:
- minimizes inductance
- reduces voltage differential between the board and chip substrate
- improves noise immunity

Analog Ground Pin

The digital circuitry needs to communicate with the main system. Digital communication involves the switching of ones and zeros. All this switching generally involves large return currents through the chip to the digital ground plane.

When the digital section is active, these currents tend to cause transient voltage differences across the substrate of the chip, and between device and the printed circuit board. The digital circuitry is designed to handle these voltage differences. The analog circuitry, however, is not.

The digital ground pin needs a solid, low impedance connection to the system ground. Avoid long traces whenever possible and keep analog signals away from this pin.

Common Ground

◆ Tie Analog and Digital grounds together at their source.
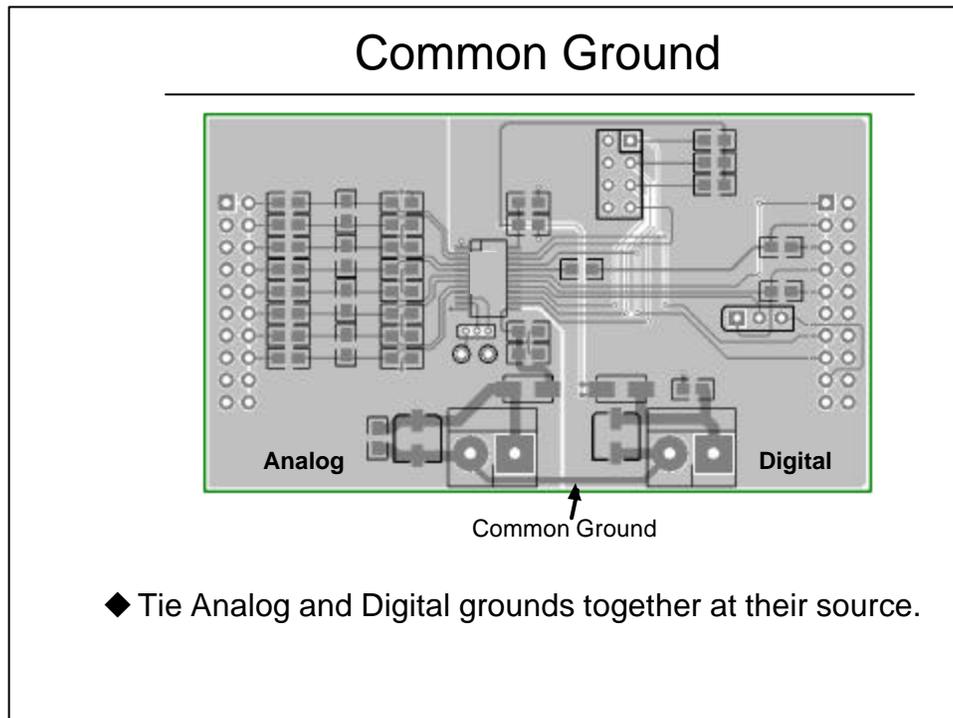
Common Ground

Since both digital and analog "islands" are part of the same system, they must be tied together somewhere. The ideal place to do this is directly on the printed circuit board close to the source of the digital and analog power.

In split plane designs, a single bridge between the digital and analog planes is recommended. Poured ground planes should be tied in a star configuration.
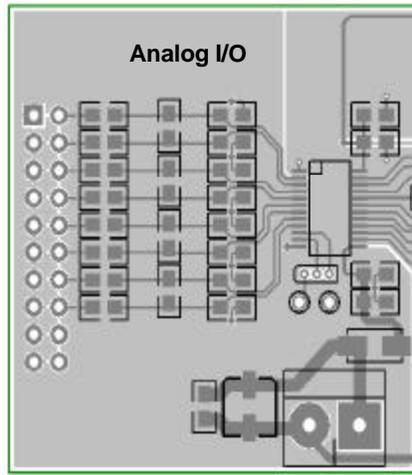
But here's the exception to the rule: we put a very small (5-10mil) connection between the two planes under the ADC - just so the digital return currents from the ADC can flow back to analog side, since they are connected inside the ADC. Note that the proper place to connect the ground planes is at the supply - but you also need to have that small connection under the ADC. Does this give you a ground loop? Yes. Is it a problem? Probably not, since the only currents that will want to flow under the ADC are its own return currents!

This points out why many times, it's just easier and makes more sense to use a single ground plane, particularly if you can partition the circuit as we have shown into distinct analog and digital portions. If you don't have that luxury, then splits in the plane can help steer currents where you want them to go, and away from sensitive analog circuitry.

As with a well-designed chip, the ideal board layout consists of well-defined analog and digital sections.

The analog inputs need to be kept short to minimize stray capacitance and inductance. This usually is not too difficult, since the analog circuitry tends to be point-to-point wiring. Symmetry in the analog I/O can improve channel-to-channel performance. By keeping the inputs symmetrical, system noise should remain nearly identical to each input. Symmetry also eases testing, troubleshooting and inspection tasks.

Keep reference circuitry and voltage regulators away from the analog I/O. This helps to reduce the effects of thermal noise and ensures that each analog channel has the same ambient environment.

If the analog and digital signals have to share a common connector, split the connector into a digital and analog section with high-speed clocks and analog inputs as far away from each other as possible.

Always route analog and digital signals away from each other. If your analog signals MUST cross digital signals, minimize the possibility of signal degradation by keeping the lines at right angles to each other. Do not allow any signal to cross between the analog and digital planes in a split plane design.

The Printed Circuit Board
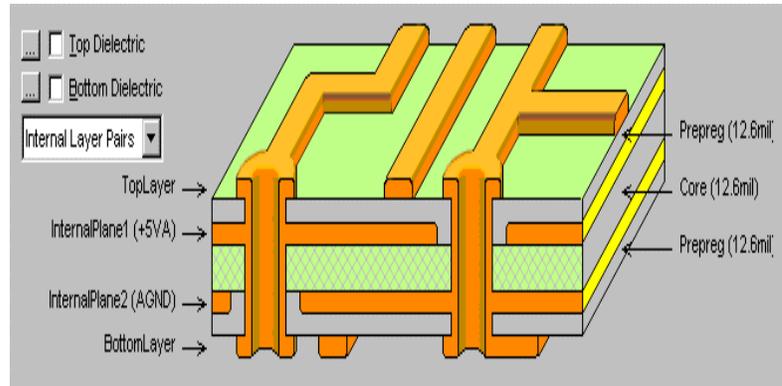
The PCB

The Printed Circuit Board (or Printed Wiring Board as it is sometimes referred to) is an essential component for the success of any design.
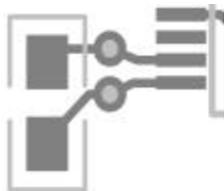
The most common type of material used in printed circuit board fabrication is the NEMA standard FR4 material. The material is actually an epoxy-glass composition with an impregnated flame resistant resin. "FR4" is a generic term which applies to the flame rating of the materials used.

FR4 typically has a dielectric constant on the order of 4.2 to 4.9 and temperature rating to 150ºC. Additional information about PCB material and design standards can be found in the "Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies"; ANSI/IPC standard IPC-D-275.

An important item to consider when selecting a board fabrication shop is to choose a house that works with your board designers. Some of the advertised "board shops" in the industry trade papers are actually shop brokers. Using a shop broker can lead to inconsistent quality of the final product.

Take time to review the design requirements with your PCB fabricator. If your design needs to adhere to specific impedance matching criteria, ask for suggestions on how to implement those needs early on. If clock signals need to be routed at a certain line width to maintain impedance, it is best to know that before the design gets underway. This helps to ensure you get the board you need without over-constraining the fabricator.

Filtering

In many cases, a single common supply can provide power for both the analog and digital portions of the data converter, provided that adequate decoupling is used. One way to do this with a single common source is to split the incoming supply into AVdd and DVdd through inductors and low ESR capacitors.

"T" filters, "PI" filters and semi-custom filter modules are available from many different suppliers. These devices usually incorporate inductors and capacitors in a single package. Size, power ratings and cost vary, so choose a solution which best fits the overall board design requirements. A single module may be more cost effective when weighed against the cost of purchasing, storing and installing two or three individual parts.

A simple rule of thumb for inductor selection is to choose one whose saturation current is 3x greater than that which your circuit requires (5x in 3.3-V systems).

Bypass Caps

◆ Reduce high-frequency noise

◆ Keep them close to the power pin

◆ Route "into" the capacitor

Bypass capacitors

Bypass capacitors are extremely important in reducing the effect of high frequency noise. Bypass capacitors should be kept close to the power pin it is decoupling. When feeding the power trace from an internal plane, put the via on the outboard side of the capacitor lead. Putting a via to the power plane between the capacitor and power pin can reduce the capacitors effectiveness. Ensure the capacitors have a short, low impedance ground return path as well.
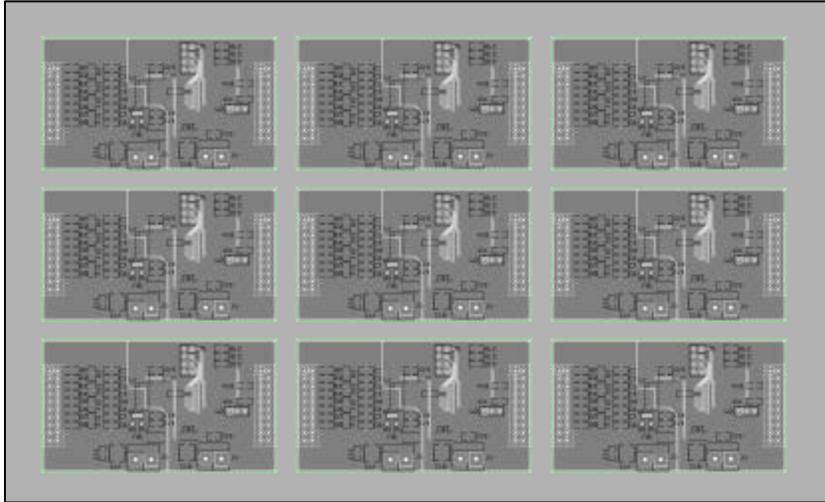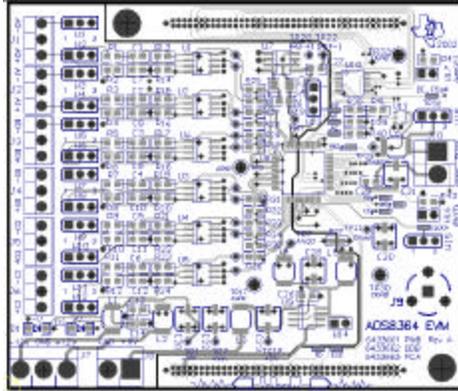
Assembly

Allow your assembly contractor/manager to review your design as well. They can point out items which may impede the ability to assemble or test the board. Ideally, the assembly contractor will also have a good rapport with your PCB fabrication house. This allows for the exchange of information between all parties regarding the expectations of the final product. The board shop can tailor panel sizes to meet the preferred conditions of the assembly shop based on the type of equipment they have.

The Final Product

◆ The end result is a well-designed board that can be reliably fabricated, easily assembled and tested with fewer problems, less rework.

The end product should represent the physical representation of the original design requirements, with inputs from Assembly, Test, Inspection and Manufacturing.

The final package represents all the assembly notes, assembly drawings, BOMs, PCB notes, test procedures, etc.
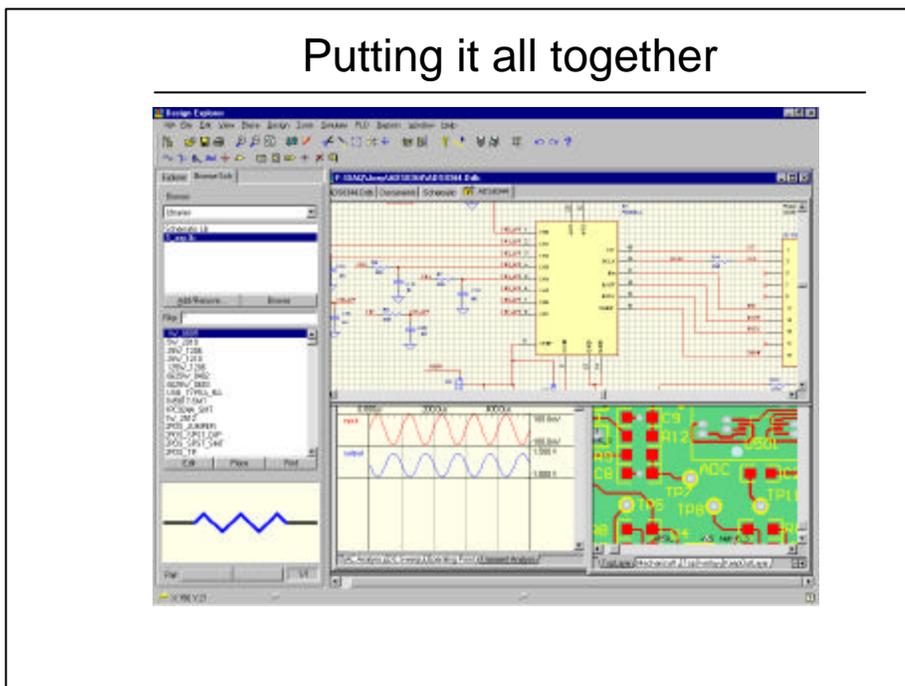
Design should be fully documented and archived so that it can be reproduced on demand.

When a design is released, there should be few, if any, questions left unanswered.

If manufacturing has to return to the design engineer to do a simple rebuild, the design is not complete.

Putting it all together

Following the circuit concept, and armed with the information you need, you can now begin your specific circuit design, layout and routing activities.

Copies of the schematic and each layer of the PWB are available for you to examine the design for yourself.

The EVM is also available for order.

Summary

- ◆ Be aware of the characteristics of the signal you want to digitize.
  - ■ Highest Frequency component, rise time,...
- ◆ Choose the data converter that meets the specifications that are most important to you.
  - ■ Static or Dynamic specs, Channel count, Speed, Power consumption, Size,...
- ◆ Buffer your analog input(s).
  - ■ This presents a stable, known output impedance to the ADC.
- ◆ Understand the role support circuits can play in achieving optimum performance.
  - ■ Voltage reference, Anti-aliasing filter, Low-jitter clock
- ◆ Plan PWB fabrication with care
  - ■ Layout, Grounding, Filtering

Additional SAR Converters

	Device Name	Number of channels	Speed (KSPS)	Power dissipation (mW)	Number of pins
Resolution					
12-bit					
	TLV2548	8 Single-ended	200	4.5	24
	TLV2541	1 Single-ended	200	2.3	8
	TLV2553	11 Single-ended	200	4.5	20
	ADS7823	1 Single-ended	50	1.6	8
	ADS7828	8 Single-ended	50	1	16
14-bit					
	TLC3578	8 Single-ended	200	29	24
	ADS8324	1 Differential	50	2.5	8
16-bit					
	TLC4541	1 Single-ended	200	17.5	8
	ADS8320	1 Differential	100	10	8
	ADS8344	8 Single-ended	100	6	20
	ADS8341	4 Single-ended	100	5	16

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