mini-LVDS Interface Specification

DSBU mini-LVDS

ABSTRACT

The trend towards higher and higher resolutions in flat panel displays, particularly LCD panels, is pushing the capabilities of conventional interfaces towards display drivers to the limit. The aggregate bandwidth requirement for state-of-the art displays (e.g. UXGA and QXGA) is already in the range of 5 Gbps and will increase. This necessitates a large number of connections between the timing controller and the display drivers, with the result being that the interconnect becomes the bottleneck in further reduction of display size. EMI generation by this wide interconnect is another problem. The conventional parallel CMOS interface, which has served well for low resolution displays in the past, is no longer a viable solution for today's displays.

The mini-LVDS is a high speed serial interface that solves these problems. This specification describes the electrical and logical features of this interface. The mini-LVDS offers a low EMI, high bandwidth interface towards display drivers, which is particularly well-suited for TFT LCD panel column drivers.

A TFT LCD panel is a two-dimensional array of pixels, arranged in n rows of m columns. Each pixel consists of three adjacent subpixels (one each for red, green and blue) in the same row. The panel is written into using an active matrix addressing scheme, whereby an entire row of pixels is updated simultaneously by column drivers. The rows are updated sequentially from the first row to the last, after which the process repeats. The timing controller has to source video data for the entire row of pixels in one line duration (~ 10 μs). This video data consists of 6 (or 8) bits of intensity information for each sub pixel.

The timing controller typically gets video data from a graphics controller. The incoming video data has format control information to delimit video frames and lines. The timing controller extracts the video data and redistributes it to the column drivers, at the same time generating control signals for the row drivers for addressing the TFT matrix.

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1 Scope

The mini-LVDS is the interface between the timing controller and the column drivers (see Figure 1). It is described in subsequent sections of this document.

Note that the standard does not cover the signals between the timing controller and the row drivers, or the signals between the column drivers (which may be used, for example, to put column drivers into power-down mode).

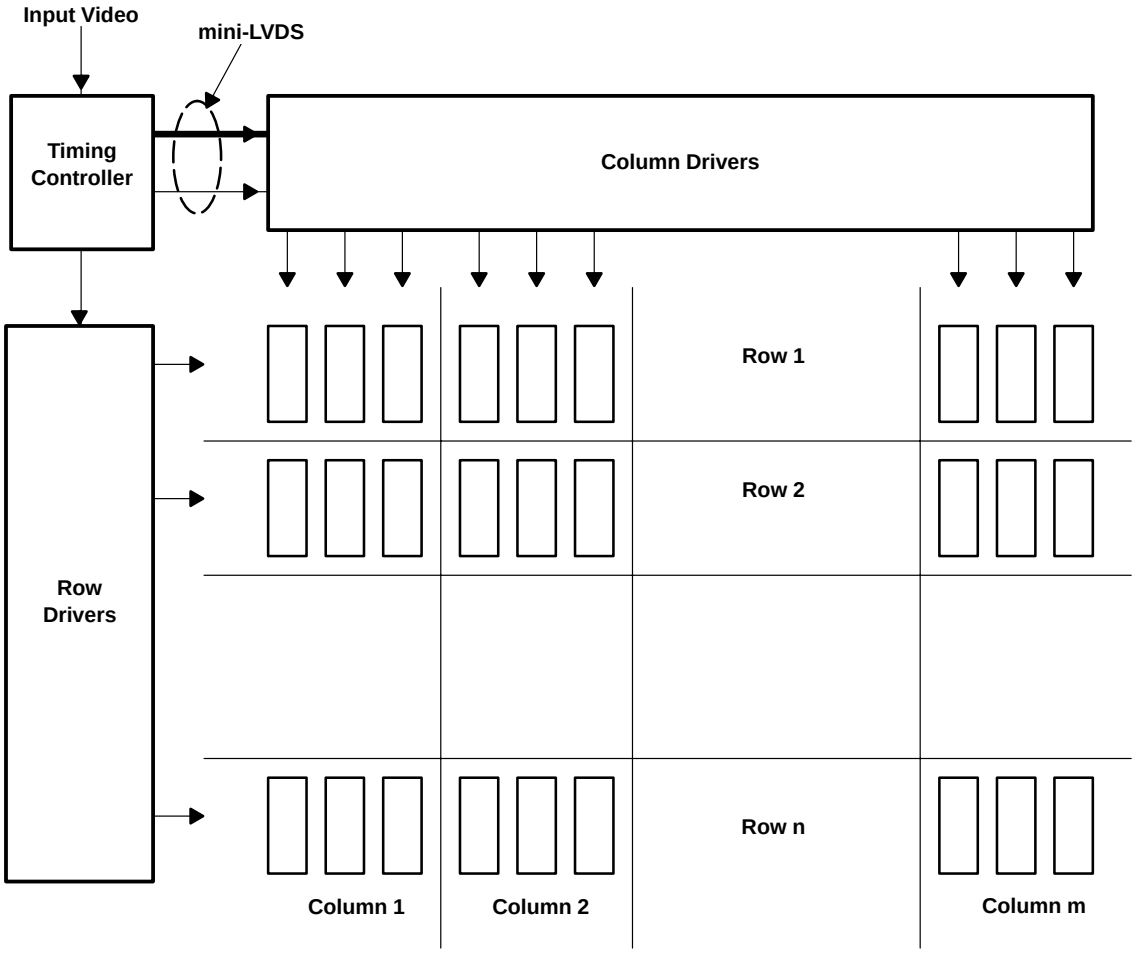


Figure 1. mini-LVDS Interface

2 Overview

The mini-LVDS is a unidirectional interface from the timing controller to the column drivers. Topologically, it is a dual bus, with each bus carrying video data for the left or the right half of the panel. These buses are subsequently referred to as RLV and LLV for the right and left halves, respectively. See Figure 2.

Physically, each bus consists of a number of pairs of transmission lines on a printed-circuit board, with each pair carrying differential serialized video and control information. The number of signal pairs is left to the particular implementation and is determined primarily by the maximum frequency that the column driver semiconductor technology can support. The individual pairs making up xLV (x is either R or L) are called xLVi, with i ranging from 0 to n for a bus consisting of n+1 data pairs. The two lines constituting the xLVi pair are xLViP and xLViM, with the P and M designating the positive and the negative lines of the pair. xLVi is deemed to be at a logic high (logic state = 1) if the voltage at xLViP is greater than the voltage at xLViM.

Each group of xLV also has an accompanying clock pair, which, like data signals, are differential pairs. To minimize EMI without increasing receiver complexity, data transfer occurs on both rising and falling edges of the clock; that is, the clock frequency is half of the maximum data transfer rate. The clock pairs are referred to as xLVCLK (x is either R or L) and the individual lines making up the pair are referred to as xLVCLKP and xLVCLKM (see Figure 3).

In addition to the differential pairs carrying video data, there are two more signals (TP1 and POL) that make up the mini-LVDS. These are CMOS level signals shared by both RLV and LLV. TP1 is essentially a line delimiter, generated by the timing controller to signal end-of-data transfer at every line. POL controls the polarity of the column driver outputs.

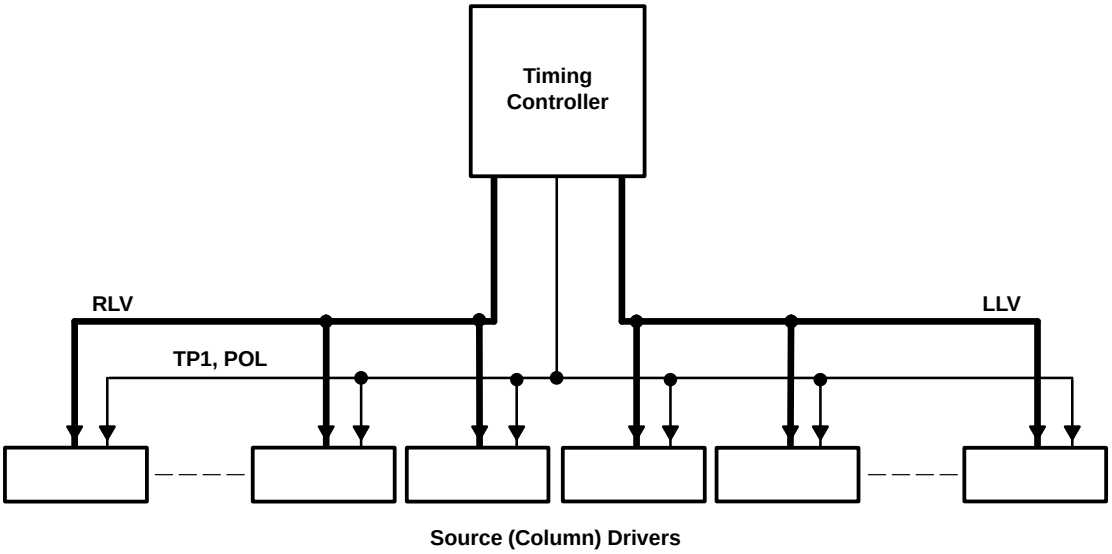


Figure 2. mini-LVDS Right and Left Buses

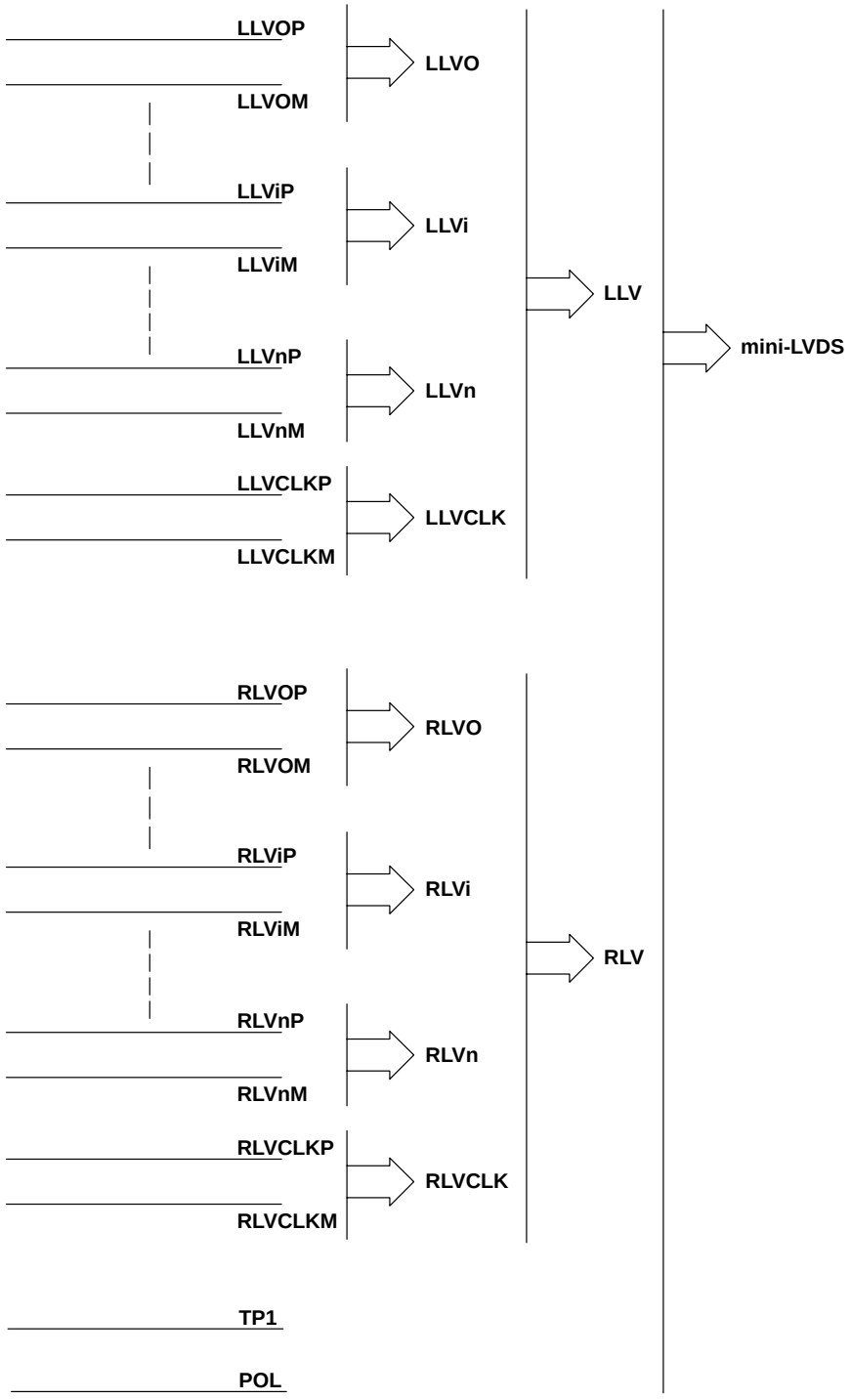


Figure 3. mini-LVDS Signals

3 DC Electrical Specifications

3.1 Transmission Line Impedance

Each mini-LVDS pair is made up of two transmission lines. In practice, these transmission lines are implemented using a strip-line or microstrip topology on a PCB. To support a variety of PCB materials of different thickness, it is recommended that the mini-LVDS transmitter in the timing controller be capable of driving transmission lines with impedances Z_O ranging from 25 Ω to 75 Ω.

To maintain signal quality, the actual impedance of the lines should not deviate from the nominal impedance Z_O by more than ±5%.

3.2 Termination

Each mini-LVDS pair should be terminated with a resistance $R_T = 2Z_O$. (see Figure 4)

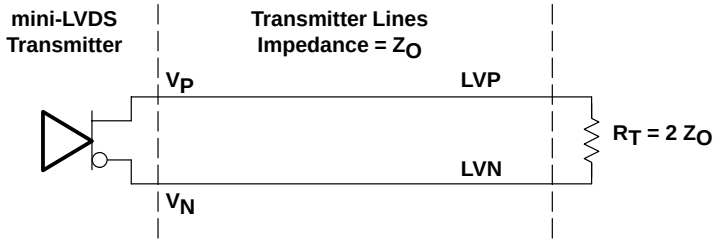


Figure 4. Signals Across a Data Pair

3.3 mini-LVDS Transmitter Output-Signal Levels

The driver output, when properly terminated, results in a small-swing differential voltage. This differential voltage is made up of two single-ended outputs. The single-ended outputs alternate between sourcing and sinking a constant current. The differential voltage is the product of this constant current and the terminating resistance R_T. To support a wide variation in the value of R_T (50 Ω to 150 Ω), it is convenient to provide some means of adjusting the output current in the transmitter.

The following specifications apply to both clock (xLVCLK) and data (xLVi) pairs over the permitted range of termination-resistance values and operating voltages (see Figure 5).

PARAMETER		MIN	NOM	MAX	UNIT
$\|V_{OD}\|$	Output differential voltage $\|V_P - V_N\|$	300		600	mV
V_{CM}	Output common mode voltage $(V_P + V_N)/2$	1	1.2	1.4	V
ΔV_{OD}	Variation in V_{OD} between 0 and 1			50	mV
ΔV_{CM}	Variation in V_{CM} between 0 and 1			50	mV

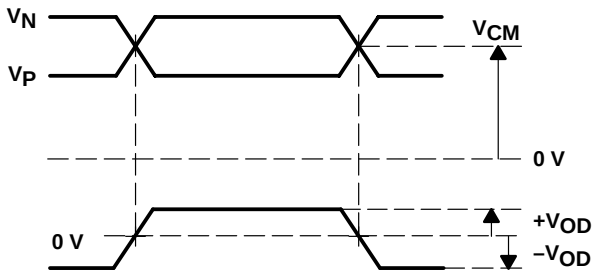


Figure 5. Signals Across a Data Pair

3.4 mini-LVDS Receiver Specifications

The mini-LVDS receivers for clock, as well as data, must comply with the following requirements over all ranges of operating conditions (see Figure 6).

PARAMETER		MIN	MAX	UNIT
$\|V_{IDTH}\|$	Input differential voltage threshold $\|V_P - V_N\|$	200	600	mV
V_{ICM}	Input common-mode voltage $(V_P + V_N)/2$	$0.3+\|V_{ID}/2\|$	$V_{DD}-1.2-\|V_{ID}/2\|$	V
I_{IL}	Input leakage current	–1	1	µA

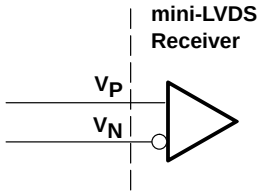


Figure 6. mini-LVDS Receiver

3.5 TP1 and POL Output Specifications

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA	0.8 V_{DD}		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		0.15 V_{DD}	V

3.6 TP1 and POL Input Specifications

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage		0.7 V_{DD}		V
V_{IL}	Low-level input voltage			0.25 V_{DD}	V

4 Differential Signal Timing Specifications

4.1 mini-LVDS Transmitter Timing Specifications

PARAMETER		MIN	MAX	UNIT
δ_{CLK}	Clock duty cycle	45%	55%	
t_f	V_{OD} fall time, 20% to 80%		500	ps
t_r	V_{OD} rise time, 20% to 80%		500	ps
t_{su}	Data setup time	$0.225 \times T_M$		
t_h	Data hold time	$0.225 \times T_M$		

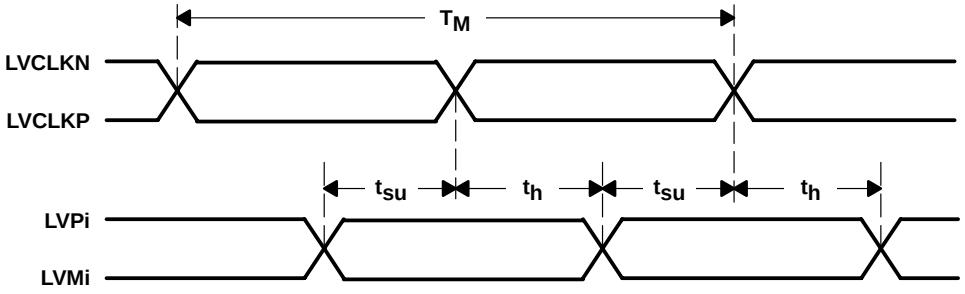


Figure 7. mini-LVDS Transmitter Timing

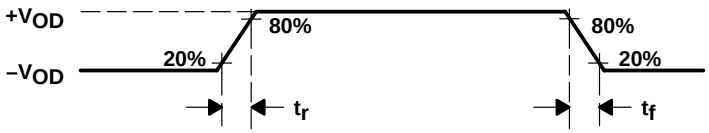


Figure 8. mini-LVDS Transmitter Pair Voltage Timing

4.2 Receiver AC Specifications

The mini-LVDS receiver functions normally with input signals meeting the following specifications over the entire range of operating conditions.

PARAMETER		MIN	MAX	UNIT
δ_{CLK}	Clock duty cycle	40%	60%	
t_{su}	Data setup time	$0.175 \times T_M$		
t_h	Data hold time	$0.175 \times T_M$		

5 Control Signal Timing

5.1 Reset Pulse

A reset pulse is embedded in the data stream to indicate start of data for every line, as shown in Figure 9. The format of the reset pulse is shown in Figure 10.

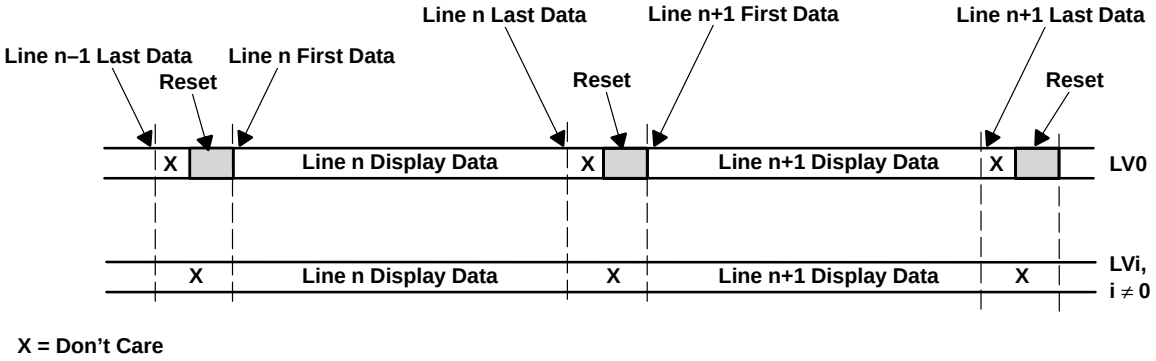


Figure 9. Reset Pulse

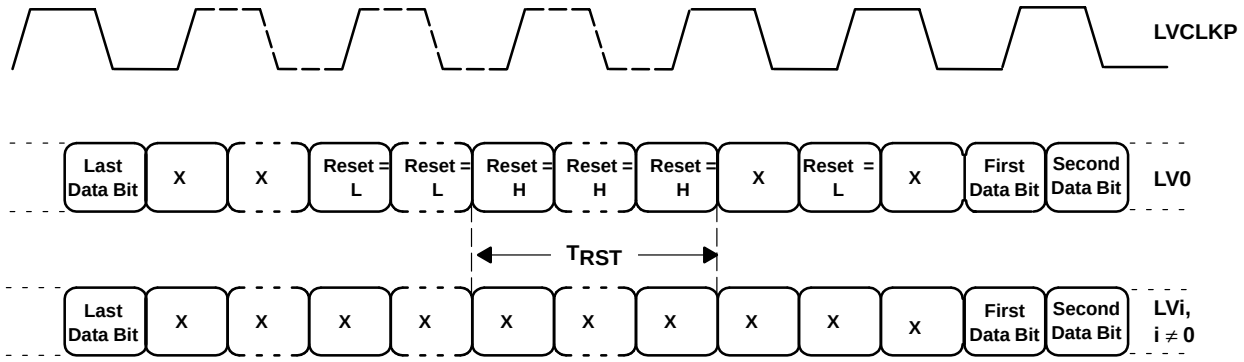


Figure 10. Reset Pulse Format

The reset pulse duration (T_{RST}) has to satisfy both of the following conditions.

PARAMETER		MIN	MAX	UNIT
T_{RST}	Reset pulse duration	50		ns
		3		T_M

5.2 Last Display Data and TP1

TP1 is generated by the timing controller to indicate that the display data for the line is over. The timing relationship is shown in Figure 11 and Figure 12.

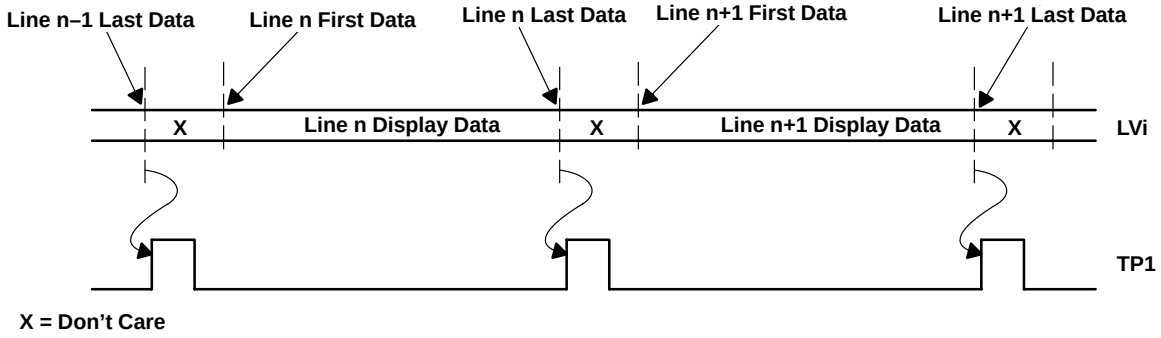


Figure 11. Timing Relationship Between TP1 and Data Lines

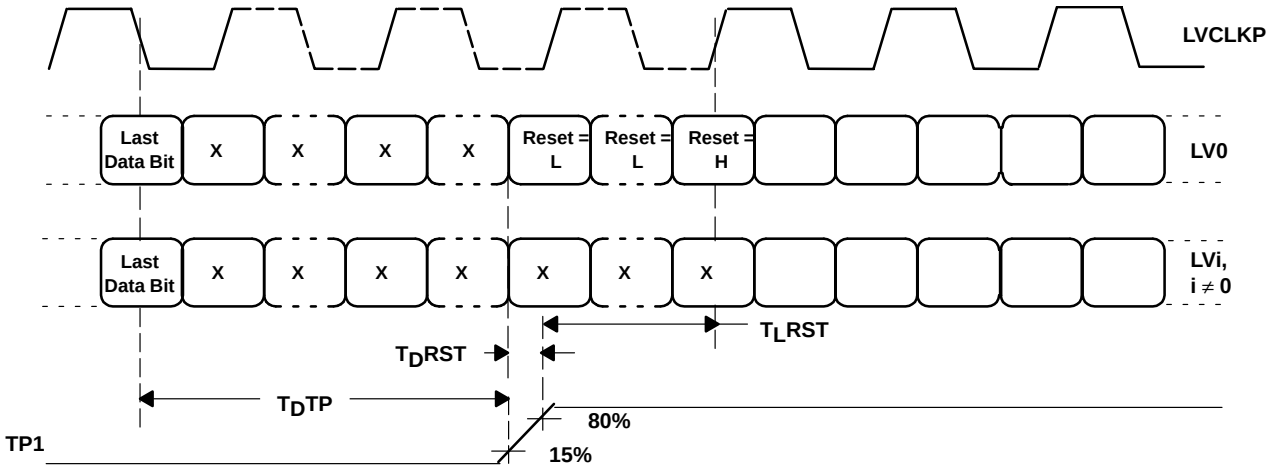


Figure 12. Display Data and TP1 Timing

PARAMETER		MIN	MAX	UNIT
T_DTP	Last data to TP1 rising edge delay	9		T_M
T_DRST	Reset low to TP1 rising edge	0		ns
T_LRST	TP1 rising edge to reset high	200		ns

Figure 13 is a consolidated picture of the events that happen at the end of a line.

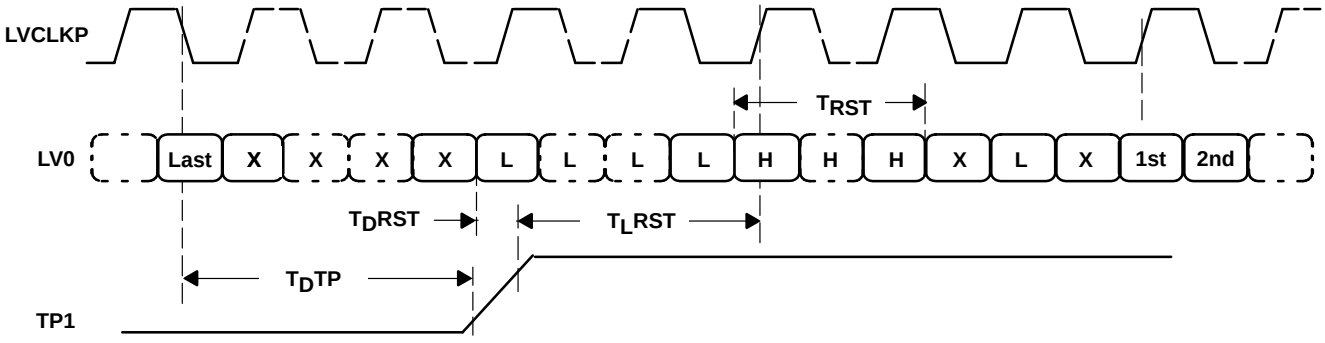


Figure 13. Display Data and TP1 Timing

5.3 Relationship Between POL and TPI

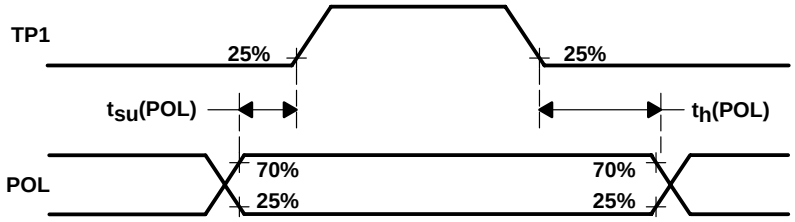


Figure 14. Relationship Between POL and TP1

The column drivers functions normally with TP1 and POL meeting the following specifications over the entire range of operating conditions.

PARAMETER		MIN	MAX	UNIT
t_{su}(POL)	Setup time for POL from TP1 rising edge	5		ns
t_h(POL)	Hold time for POL from TP1 falling edge	6		ns

The timing controller should generate POL with the following specifications.

PARAMETER		MIN	MAX	UNIT
t_{su}(POL)	Setup time for POL from TP1 rising edge	6		ns
t_h(POL)	Hold time for POL from TP1 falling edge	7		ns

6 Logical Interface

6.1 Overview and Definitions

This section defines the ordering of data on the mini-LVDS links.

Any pixel in the display panel can be uniquely identified by a pair of numbers (i, j), where i and j are the row and column numbers of the pixel location, respectively. In this document, (i, j)P stands for the pixel located at (i, j), and (i, j)R, (i, j)G, (i, j)B represents the red, green, and blue subpixels of pixel (i, j)P. The 6 (or 8)-bit word that determines the intensity of subpixel (i, j)X is written as (i, j)X5–0 or (i, j)X7–0, and (i, j)Xk represents the k^{th} bit of the word, (i, j)X0 being the LSB. (X is either R, G, or B).

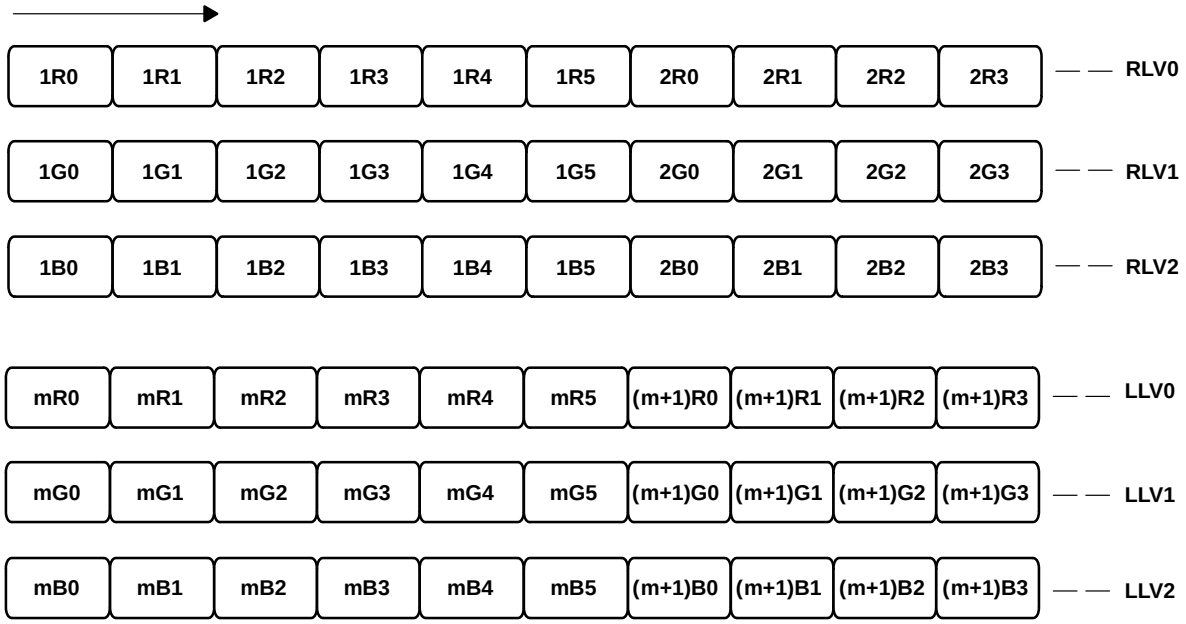
Display data is transported line by line on the mini-LVDS interface and no distinction is made between different lines. This distinction is made by the row (gate) drivers, which are controlled separately by the timing controller. So we can be simplify the above representation and let iP stand for the i^{th} pixel in a given row. In this scheme, iR, iG, and iB mean the red, green, and blue subpixels of iP. iXk is the k^{th} bit of the intensity word for subpixel iX.

6.2 Data Sequence

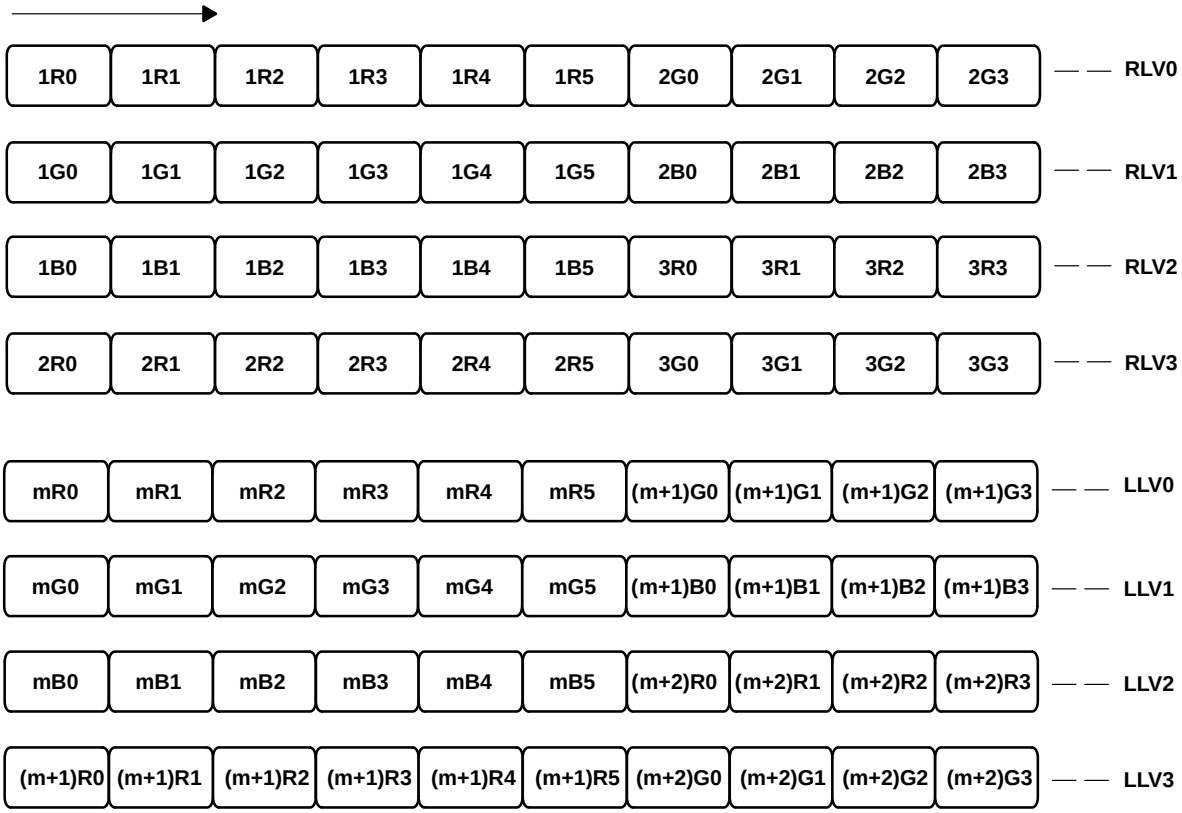
This section describes the sequence in which bits are transported from the timing controller to the column drivers on LLV and RLV for a display with 2m pixels in each row. Several cases with different numbers of links in the busses for both 6-bit and 8-bit data are covered.

These sequences can easily be extended to handle cases of fewer/more data pairs.

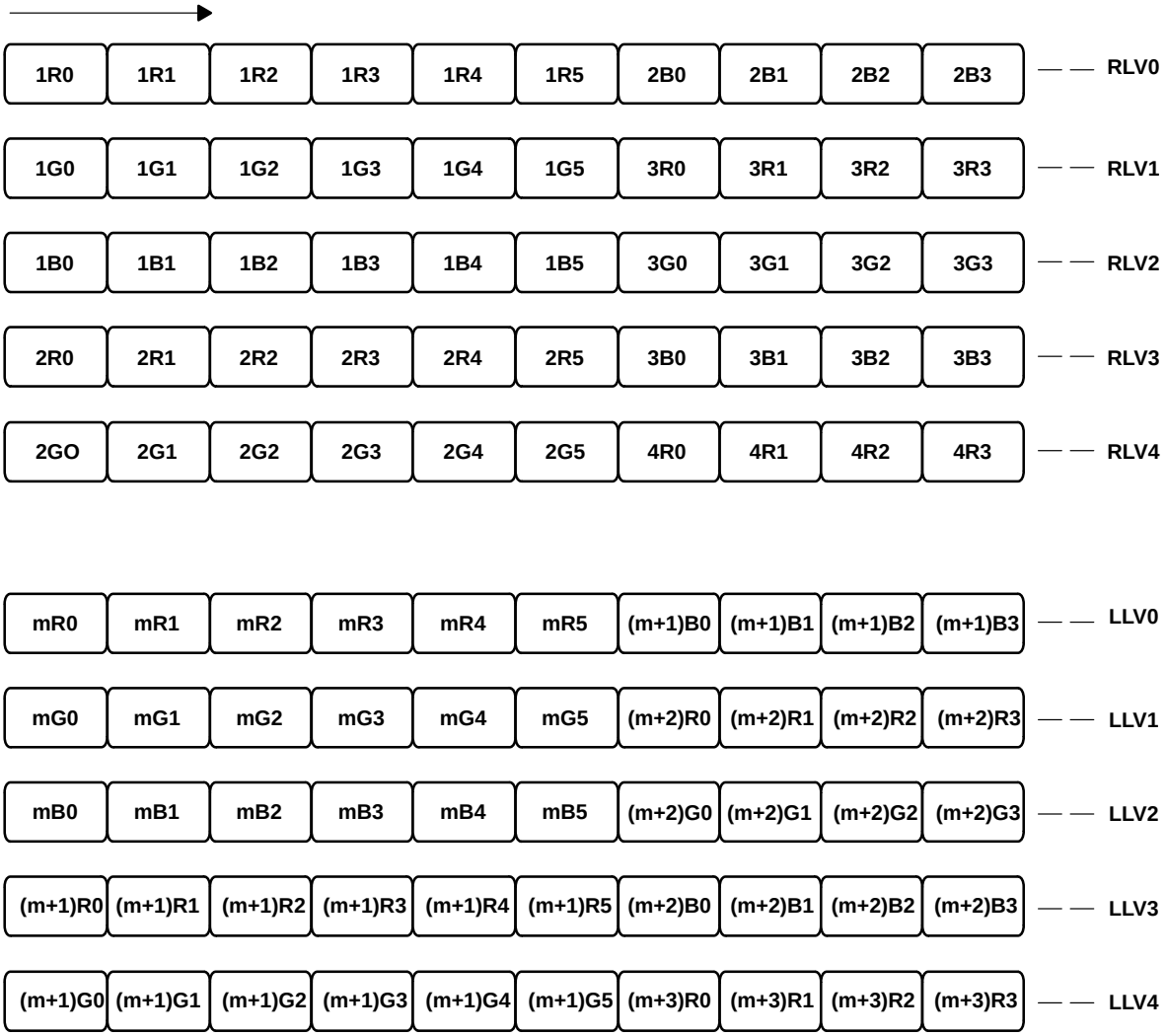
6.2.1 6-Bit Data, Three Pairs



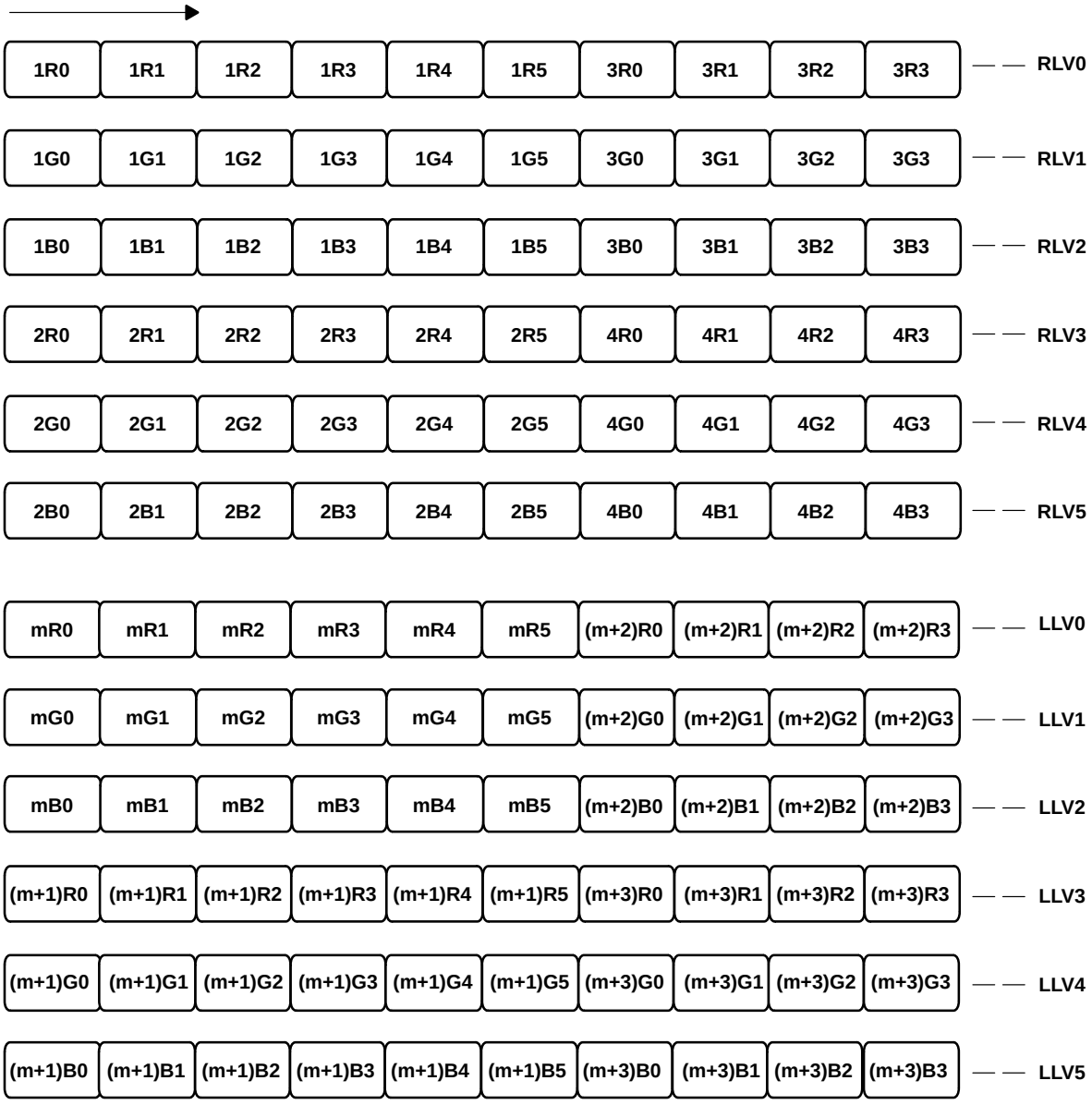
6.2.2 6-Bit Data, Four Pairs



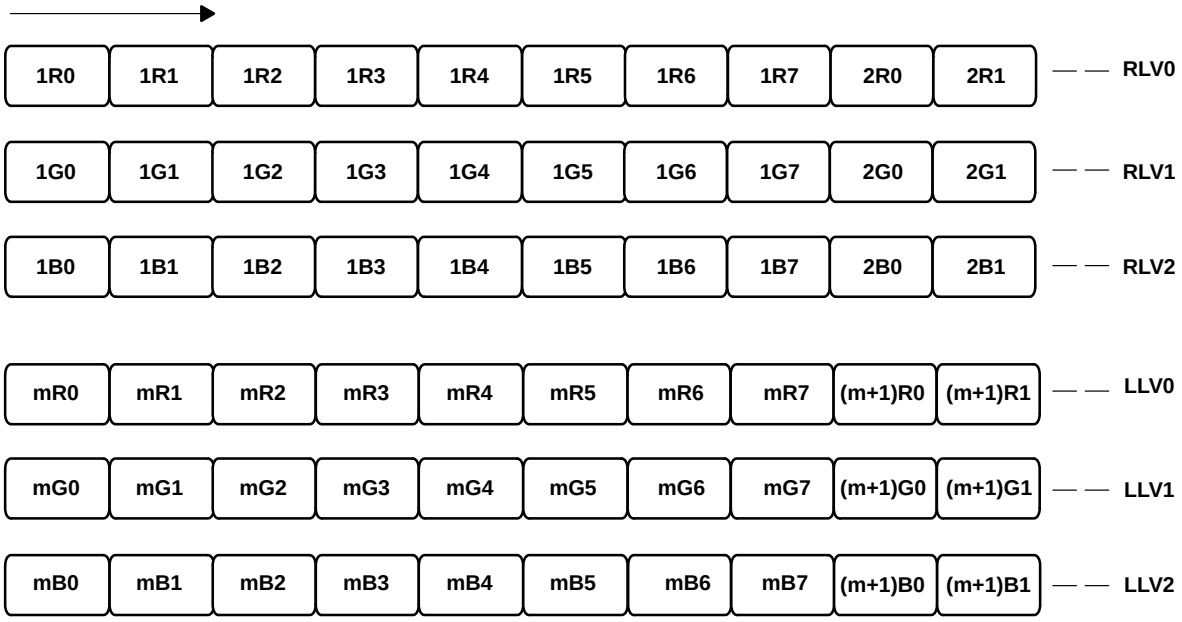
6.2.3 6-Bit Data, Five Pairs



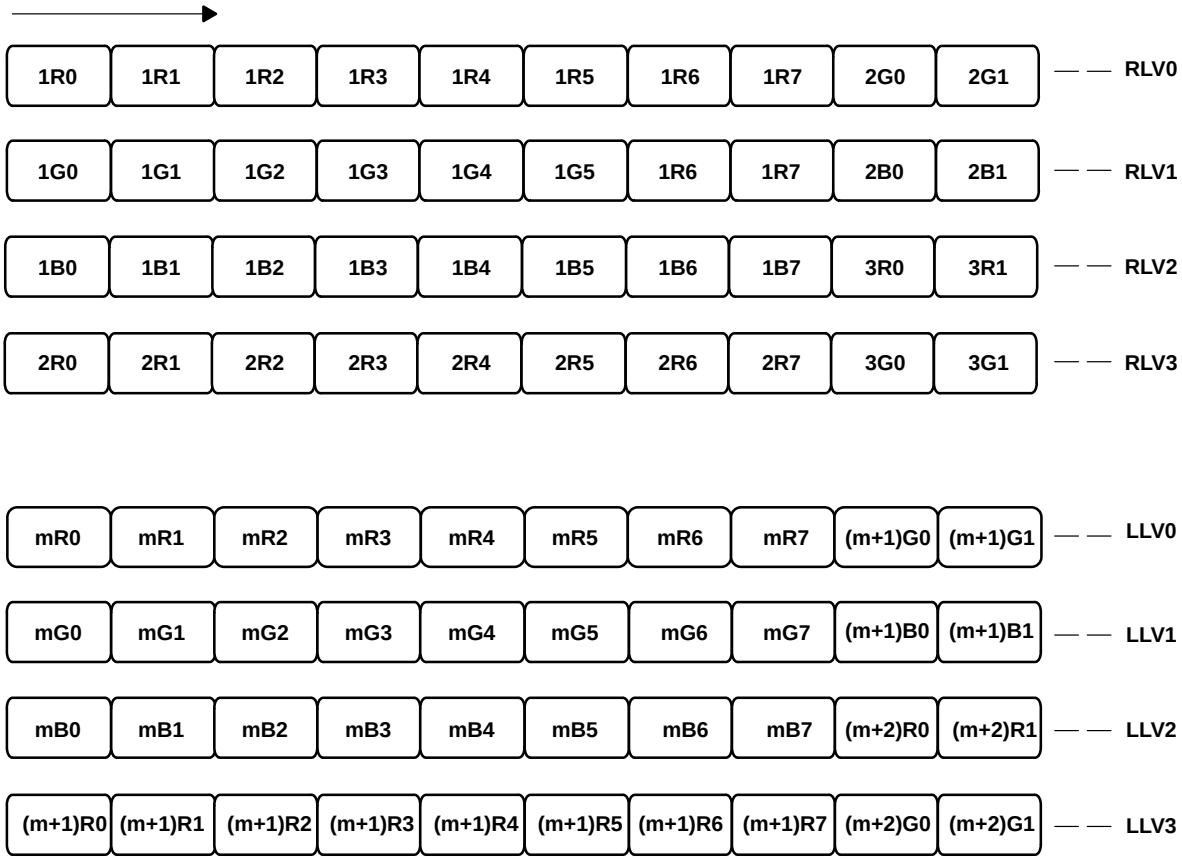
6.2.4 6-Bit Data, Six Pairs



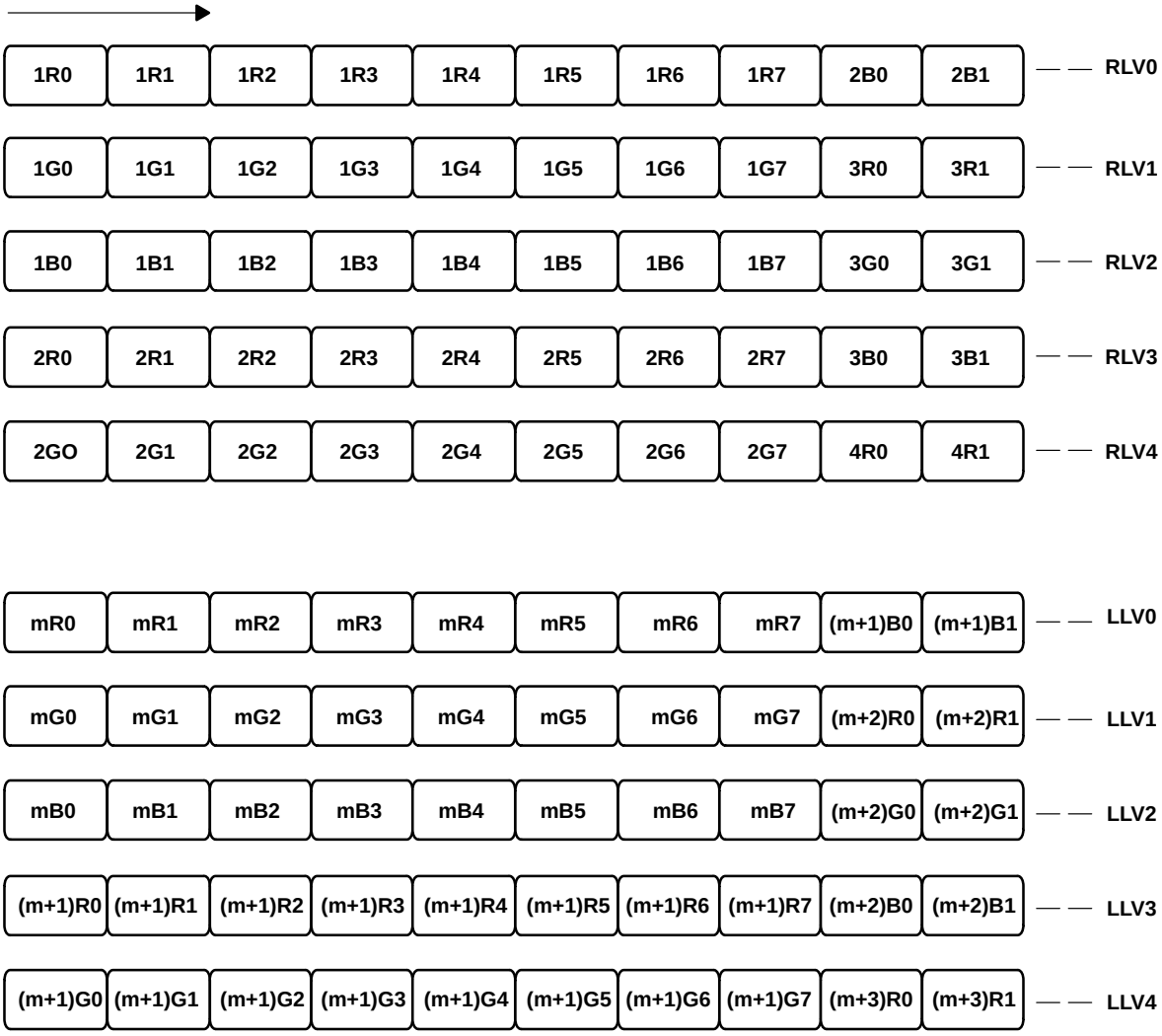
6.2.5 8-Bit Data, Three Pairs



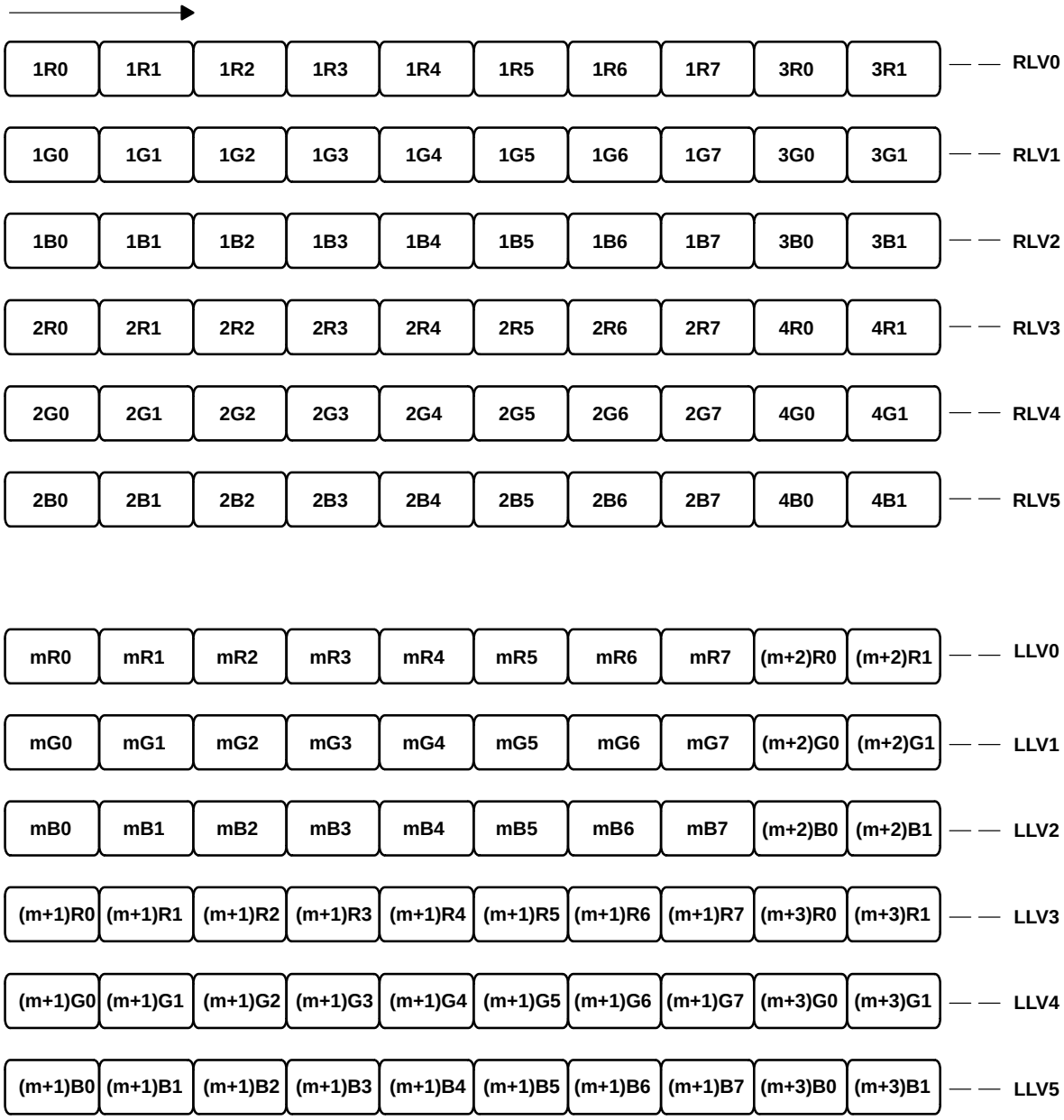
6.2.6 8-Bit Data, Four Pairs



6.2.7 8-Bit Data, Five Pairs



6.2.8 8-Bit Data, Six Pairs



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