PCM1807EVM

The DEM-DAI1807 is an evaluation board for the PCM1807, a 96-kHz, 24-bit PCM audio A/D converter, with digital audio transmitter, optical and coaxial interfaces, onboard multiple clock generator, –6-dB amplifier with LPF, switches and jumpers for mode and clock control, and a connector to interface with a PC for serial-mode control. On the evaluation board, the PCM1807 works in conjunction with a DIT4096 and a PLL1707.

The DIT4096 is a digital audio interface transmitter designed for use in both professional and consumer applications, and which converts the PCM audio interface signal to an S/PDIF signal and supports data rates up to 96 kHz. The PLL1707 is a phase-locked-loop multiclock generator which generates various audio system clock frequencies from a 27-MHz master clock. Detailed information on the devices is available from the following links:

PCM1807 Single-Ended, Analog-Input 24-Bit, 96-kHz Stereo A/D Converter data sheet, (SLES147)

DIT4096 96kHz Digital Audio Transmitter data sheet, (SBOS225)

PLL1707, PLL1708 3.3-V Dual PLL Multiclock Generator data sheet, (SLES065)

The DEM-DAI1807 operates using 5-V and ±15-V analog power supplies with a 1-Vrms or 2-Vrms unbalanced analog signal input.

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1.1 Block Diagram

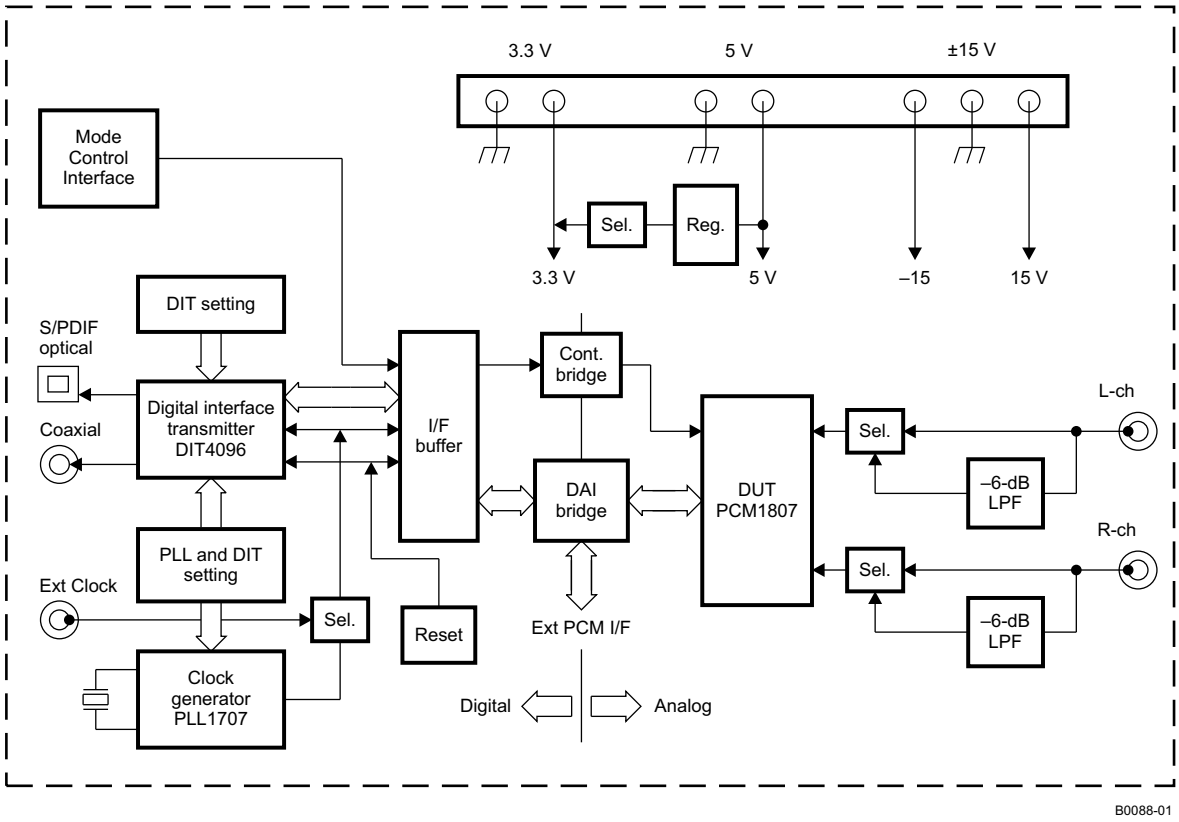


Figure 1. DEM-DAI1807 Block Diagram

1.2 Basic Connection and Operation

1.2.1 Basic Connections and Configurations

1. Install the REGTEST software accompanying the EVM into an appropriate folder of the PC which is to be used to control this EVM.
2. Connect the 5-V and ±15-V power supplies to V_{CC}, $\pm AV_{CC}$, and GND on CN051–CN055. The ±15-V power supplies are required only for 2-Vrms input.
3. Connect the S/PDIF output to CN003 (coaxial) or U001 (optical).
4. Using JP001, select the system clock source from the 256/512 f_S or 384 f_S generated by the onboard clock generator (PLL1707), or from the external clock input connector (CN001), and ensure the presence of system clock on JP001.
5. Set the interface mode (master or slave) using the M/$\overline{S}$ switch of SW002.
6. Set the interface (master or slave) through the serial-mode control to PCM1807 from the PC using the REGTEST software, if required.
7. Set the interface format (LJ-24 or I^2S-24) using the FMT0 switch of SW002.
8. Set the interface format (LJ-24 or I^2S-24) through the serial-mode control to PCM1807 from the PC using the REGTEST software, if required.
9. Select the combination of sampling frequency (16 kHz to 96 kHz) and system clock rate (256, 384, 512 f_S) using CLK1, CLK0, SR, FS2, and FS1 of SW002.
10. Set the channel status for DIT4096, if required. (It is not required for PCM1807 evaluation.)

1.2.2 Configuration Controls

1.2.2.1 System Clock Source Selection

The system clock (master clock) source for EVM including PCM1807, which is associated with sampling frequency, can be selected by the JP001 settings shown in Table 1.

Table 1. System Clock Source Selection

JP001	Description
256	Internal, 256/512 times the sampling frequency
384	Internal, 384 times the sampling frequency
EXT	External, TTL interface level, up to 25 MHz

1.2.2.2 Master/Slave Interface Mode Selection

The audio interface mode of PCM1807 on the EVM can be selected as shown in Table 2. In slave mode, the audio interface clock, BCK, and LRCK are generated in the DIT4096 and supplied to the PCM1807 through a buffer. In master mode, they are generated in the PCM1807 and supplied to the DIT4096.

Mode control of the PCM1807 must be performed in serial mode through the mode-control interface by running the REGTEST software on a PC attached to EVM.

For slave-mode operation just after power on, mode control of the PCM1807 is not required, because slave mode is the default mode of the PCM1807.

Table 2. Master/Slave Interface Mode Selection

SW002, M/S (1)	PCM1807, I/F Mode (1)		Description
	MDI	MDO	
OFF (High)	0	0	Slave mode (default)
ON (Low)	0	1	Master mode
	1	0	
	1	1	

(1) Other inconsistent combinations between SW002 M/S selection and PCM1807 setting are reserved.

1.2.2.3 Interface Format Selection

The audio interface format of the PCM1807 on the EVM is selected as shown in Table 3.

Table 3. Interface Format Selection

SW002, FMT0 (1)	PCM1807, FMT (1)	Description
OFF (High)	0	I^2S 24-bit (default)
ON (Low)	1	Left-justified 24-bit

(1) Other inconsistent combinations between SW002 FMT0 selection and PCM1807 setting are reserved.

1.2.2.4 Sampling Frequency and System Clock Frequency Selection

The sampling frequency and the system clock frequency for the PCM1807 and EVM can be selected as shown in Table 4 and Table 5 by setting JP001, SW002, and PCM1807. Sampling frequencies of 16 kHz to 96 kHz and system clock frequencies of 256 f_S, 384 f_S, and 512 f_S are available for the EVM. The settings of JP001, CLK1, and CLK0 of SW002, and PCM1807 register bits MD1, MD0 as shown in Table 4 determine the system clock rate. The settings of SR, FS2, and FS1 of SW002 as shown in Table 5 determine the sampling clock and system clock frequencies. The possible combinations of sampling clock and system clock frequencies appear in the rightmost column of Table 5.

Table 4. System Clock Rate Selection

JP001	SW002[1]		PCM1807, I/F Mode[2]		System Clock Rate
	CLK1	CLK0	MD1	MD0	
–	ON/Low	ON/Low	–	–	Reserved
256	ON/Low	OFF/High	1	1	256 f_S
384	OFF/High	ON/Low	1	0	384 f_S
256	OFF/High	OFF/High	0	1	512 f_S

(1) Select the DIT4096 master clock rate.
(2) Select the system clock rate if master-mode operation of the PCM1807 is required. If slave-mode operation of the PCM1807 is required, the combination of MD1 = 0 and MD0 = 0 is available for all three rates, 256 f_S, 384 f_S, and 512 f_S, and it does not require setting of the PCM1807 as it is a default state of PCM1807.

Table 5. Sampling Frequency and System Clock Frequency Selection

SW002[1]			FREQUENCIES
SR	FS2	FS1	Sampling Clock (kHz)/System Clock (MHz)
256 f_S Operation			
OFF/Low	ON/High	OFF/Low	32/8.192
OFF/Low	OFF/Low	ON/High	44.1/11.2896
OFF/Low	OFF/Low	OFF/Low	48/12.288
ON/High	ON/High	OFF/Low	64/16.384
ON/High	OFF/Low	ON/High	88.2/22.5792
ON/High	OFF/Low	OFF/Low	96/24.576
384 f_S Operation			
OFF/Low	ON/High	OFF/Low	32/12.288
OFF/Low	OFF/Low	ON/High	44.1/16.9344
OFF/Low	OFF/Low	OFF/Low	48/18.432
ON/High	ON/High	OFF/Low	64/24.576
ON/High	OFF/Low	ON/High	88.2/33.8688[2]
ON/High	OFF/Low	OFF/Low	96/36.864[2]
512 f_S Operation			
OFF/Low	ON/High	OFF/Low	16/8.192[2]
OFF/Low	OFF/Low	ON/High	22.05/11.2896
OFF/Low	OFF/Low	OFF/Low	24/12.288
ON/High	ON/High	OFF/Low	32/16.384
ON/High	OFF/Low	ON/High	44.1/22.5792
ON/High	OFF/Low	OFF/Low	48/24.576

(1) Select the clock output frequency of PLL1707 SCKOx; the combination of FS2 = ON/High and FS1 = ON/High is reserved.
(2) Not applicable through the S/PDIF interface due to a limitation of the DIT4096. They are applicable for PCM direct interface between PCM1807 and externals.

1.2.2.5 Analog Input Level/Path Selection

The DEM-DAI1807 supports 1-V rms or 2-V rms as the full-scale analog input signal. The input range is selected by setting JP101 and JP102. For 2-V rms input selection, the input signal is applied through an onboard 100-kHz LPF and –6-dB attenuator. The default setting is 2-V rms input. The input level settings are listed in Table 6.

Table 6. Analog Input Level/Path Selection

JP101, 102	Description
1Vrms	1-V rms full-scale, analog input is fed to ADC directly.
2Vrms	2-V rms full-scale, analog input is fed to ADC through 100-kHz LPF and –6-dB attenuator (default).

1.2.2.6 Reset Control

Pushbutton switch SW003 is the DEM-DAI1807 reset control for the DIT4096.

1.2.2.7 S/PDIF Transmitter Format (Channel Status) Setting for DIT4096

The extended configurations of the digital audio interface transmitter, DIT4096, and the channel status of S/PDIF can be set using the DIP switches, SW001. The individual switch settings and their functions are described in Table 7. For general evaluation or test of the functionality and performance of the PCM1807, changes from default settings of SW001 are not needed. This is provided for evaluation of DIT4096 function, mainly related with channel status information.

Table 7. S/PDIF Transmitter Format (Channel Status) Settings for DIT4096

SW001	On/Off	Description
CSS	Off (High)	Channel status data bits are set in serial fashion at the COPY/C input with clock input at the SYNC input.
	On (Low)	COPY/C, L, $\overline{\text{AUDIO}}$, and $\overline{\text{EMPH}}$ inputs are used to set associated channel status data bits.
COPY/C(1)	Off (High)	Copy and generation status information with L input for CSS = Low, channel status data bit = 1 for CSS = High
	On (Low)	Copy and generation status information with L input for CSS = Low, channel status data bit = 0 for CSS = High
U	Off (High)	User data input = 1
	On (Low)	User data input = 0
V	Off (High)	Validity data input = 1
	On (Low)	Validity data input = 0
L(1)	Off (High)	Copy and generation status with COPY/C for CSS = Low
	On (Low)	Copy and generation status with COPY/C for CSS = Low
$\overline{\text{AUDIO}}$	Off (High)	Audio data valid control input, nonlinear PCM
	On (Low)	Audio data valid control input, linear PCM
$\overline{\text{EMPH}}$	Off (High)	Pre-emphasis status input, pre-emphasis not applied
	On (Low)	Pre-emphasis status input, pre-emphasis applied
BLSM	Off (High)	BLS mode control input, BLS is an output
	On (Low)	BLS mode control input, BLS is an input
BLS	Off (High)	Block start is input for BLSM = Low, output for BLSM = High
	On (Low)	Not block start

(1) Copy and generation status information for CSS = Low; details are described as follows.

COPY/C	L	Copy and Generation Status
On (Low)	On (Low)	Consumer mode, PRO = 0, COPY = 0, L = 0
On (Low)	Off (High)	Consumer mode, PRO = 0, COPY = 0, L = 1
Off (High)	On (Low)	Consumer mode, PRO = 0, COPY = 1, L = 0
Off (High)	Off (High)	Professional mode, PRO = 1, no copy protection

1.2.2.8 Mode and Function Control for PCM1807

The mode/function controls for the PCM1807 can be performed through the serial-mode control port which is written by the REGTEST control software on a PC. In REGTEST, the control word consists of a register address and the control data. The register address of the control register is 31h and the control data is shown in Table 8.

Table 8. Mode and Function Controls for the PCM1807

RegAdr	B7	B6	B5	B4	B3	B2	B1	B0
31h	MRST	SRST	MD1	MD0	FMT	PDWN	PREV	MUTE

The individual settings and definitions are described in the following tables.

MRST	Description
0	Mode control register reset
1	Normal operation (default)

SRST	Description
0	System reset (clock and timing reset)
1	Normal operation (default)

MD1	MD0	Description
0	0	Slave mode (default)
0	1	Master mode, 512 f_S
1	0	Master mode, 384 f_S
1	1	Master mode, 256 f_S

FMT	Description
0	I^2S, 24-bit (default)
1	Left-justified, 24-bit

PDWN	Description
0	Normal operation (default)
1	Power-down mode

PREV	Description
0	Normal operation (default)
1	DOUT DATA polarity reverse

MUTE	Description
0	Normal operation (default)
1	DOUT data mute on

1.2.2.9 DAI Bridge and Control Bridge Selection

The DEM-DAI1807 has a flexible PCM audio interface through the DAI bridge, so that the PCM1807 can interface with external devices or equipment instead of the internal buffer and DIT4096. Interfacing with externals can be done by changing the JP052 and JP053 connections for SCLK, BCK, LRCK, DATA, and GND as described in Figure 2.

The DEM-DAI1807 also supports flexible serial mode control of the PCM1807 by allowing connection with other control devices or equipment through settings of the control bridge, JP054. The default setting is for interface with the internal DIT4096 and mode control enabled.

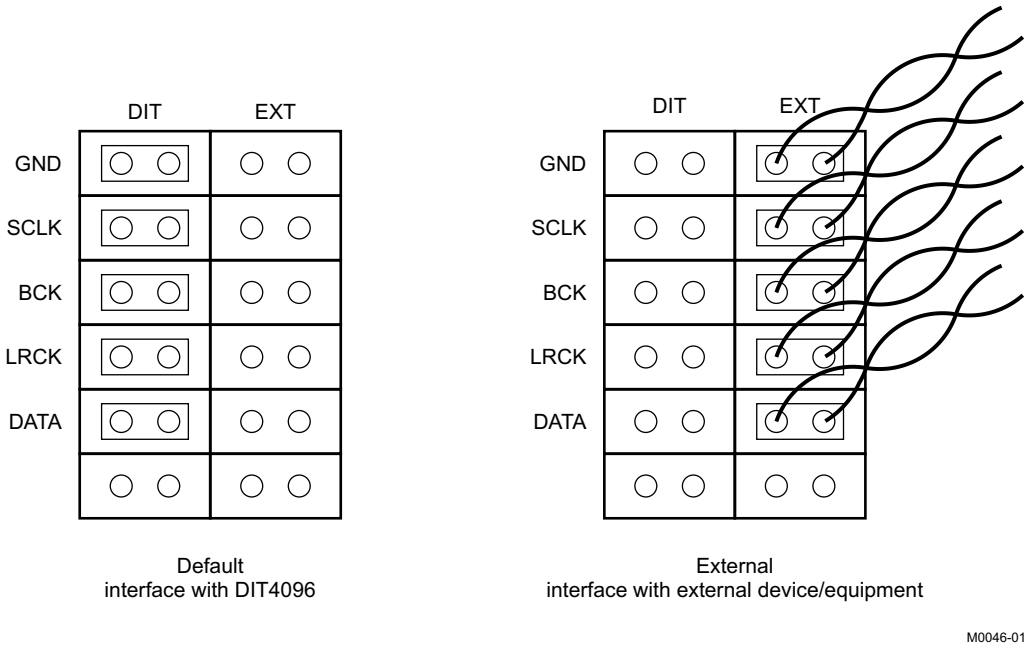


Figure 2. DAI Bridge Connection

1.3 Typical Performance and Measurement Example

Typical performance of DEM-DAI1807 for default condition is as follows, and FFT results for full scale input and –60 dB input are shown in Figure 3 and Figure 4, respectively.

THD+N at 48 kHz/512 f_S	– 93.5 dB
Dynamic range at 48 kHz/512 f_S	99.2 dB
SNR at 48 kHz/512 f_S	99.2 dB

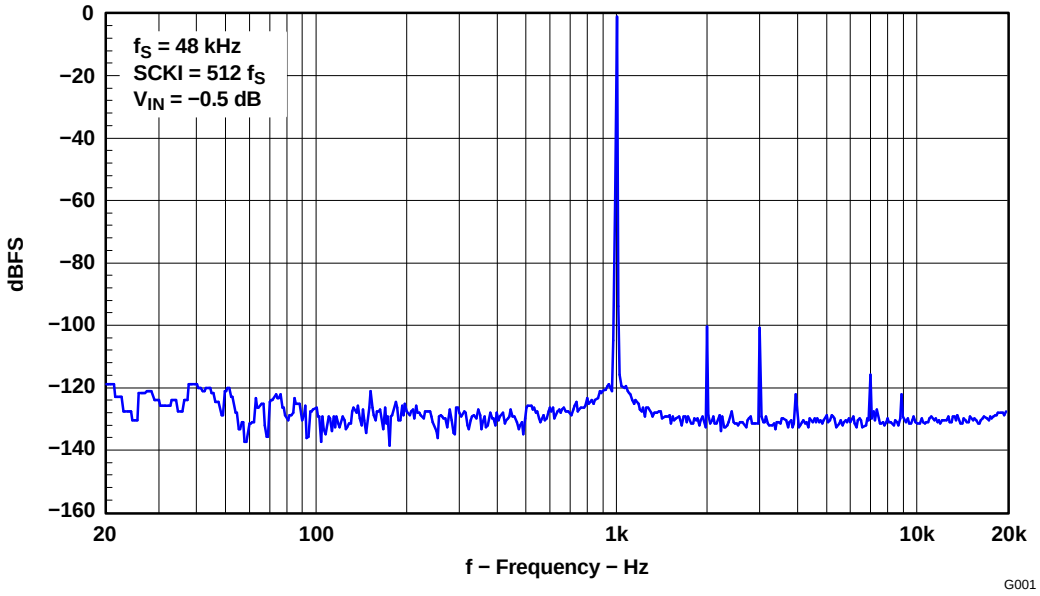


Figure 3. FFT Spectrum for –0.5-dB, 1-kHz Signal

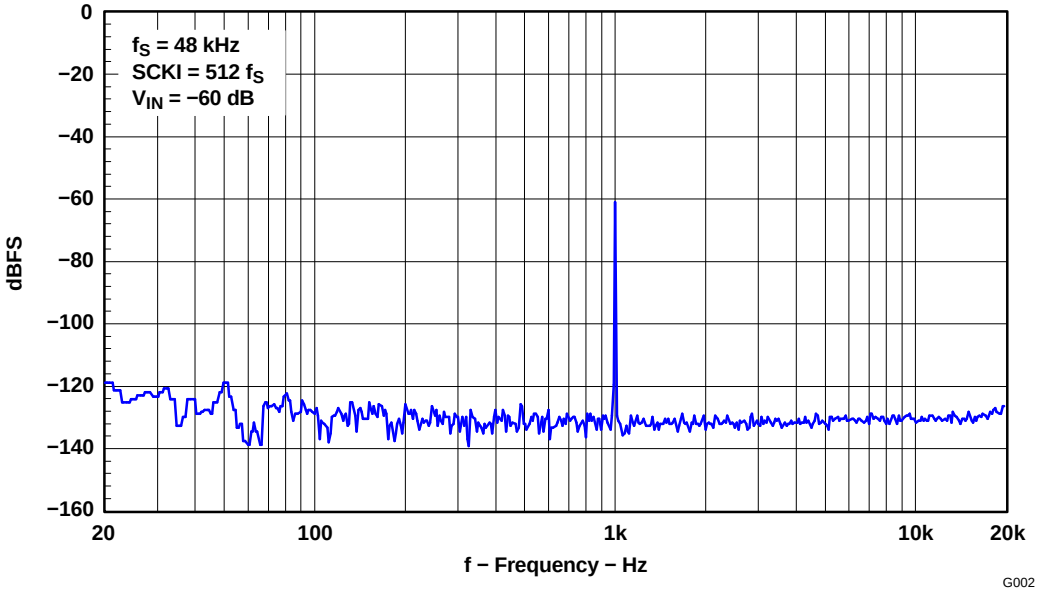


Figure 4. FFT Spectrum for –60-dB, 1-kHz Signal

2 Schematic and Printed-Circuit Board

This section presents the DEM-DAI1807 schematics, BOM, and printed-circuit boards.

2.1 DEM-DAI1807 Schematic

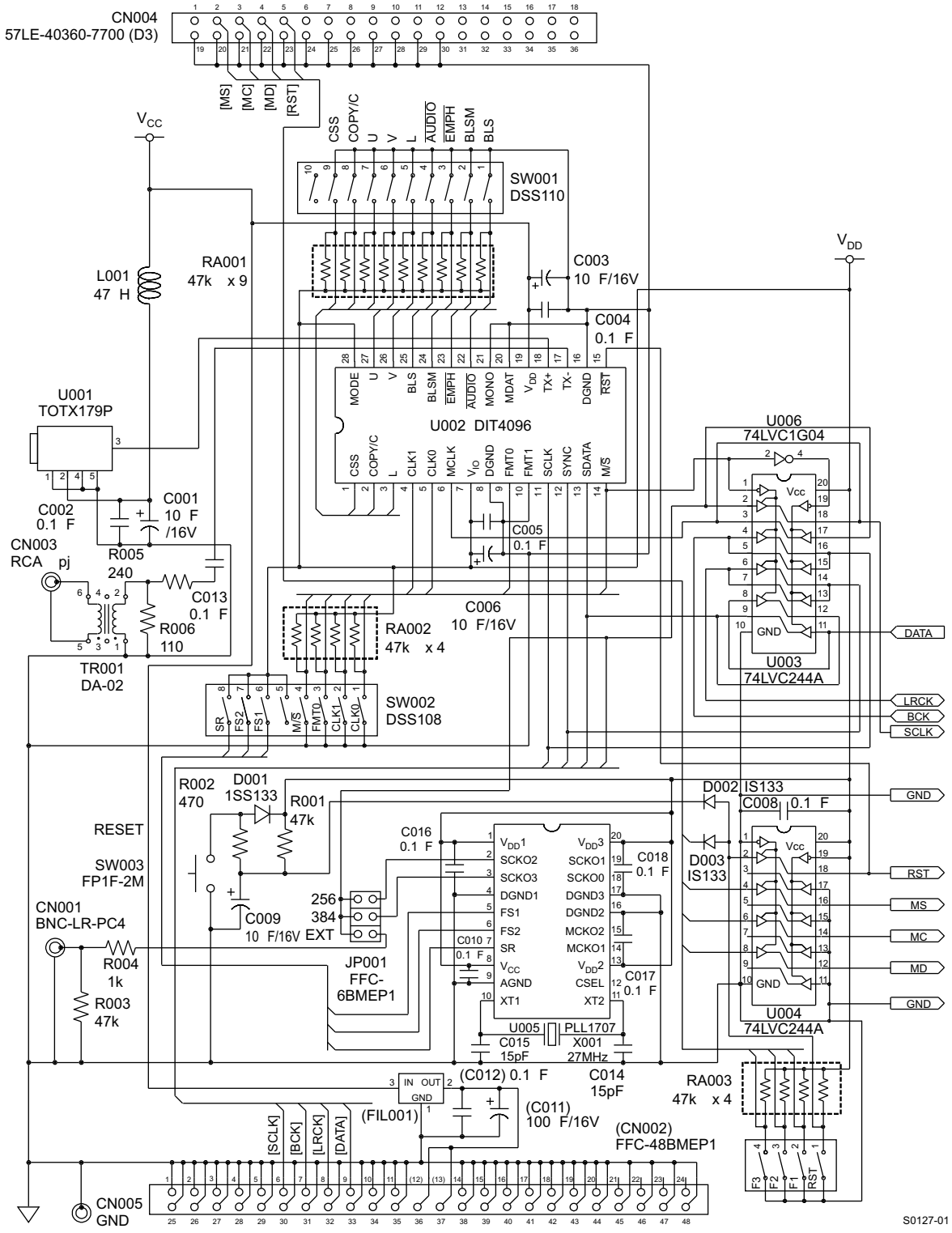


Figure 5. DEM-DAI1807 Digital Section (Digital Audio Interface) Schematic Diagram

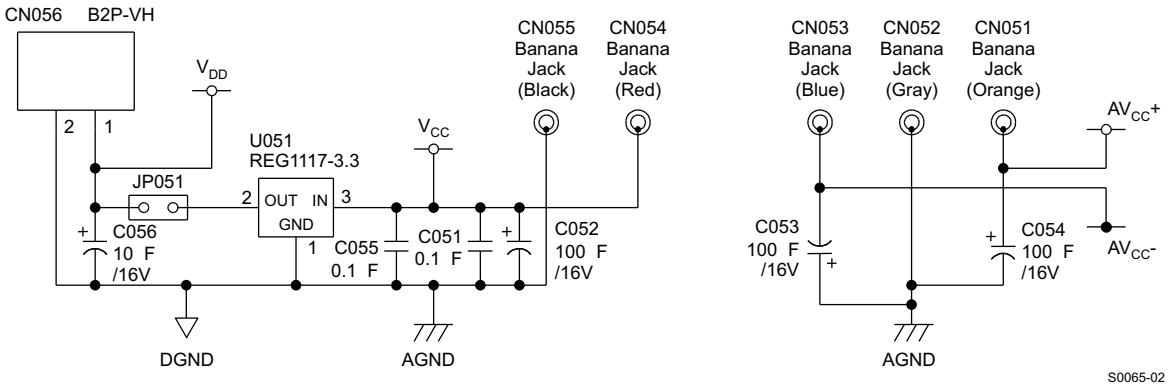


Figure 6. DEM-DAI1807 Regulator and Connector Schematic Diagram

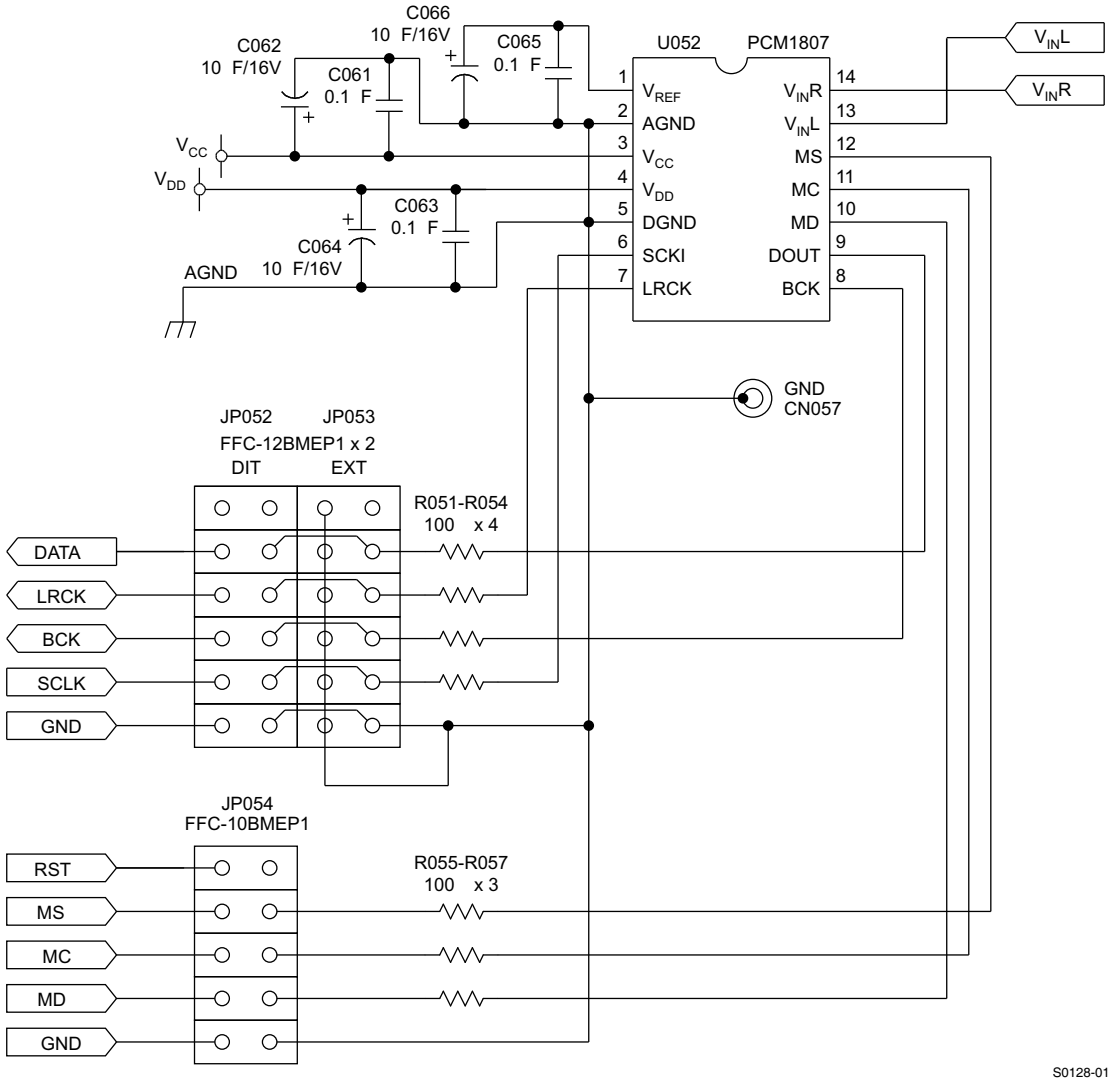


Figure 7. DEM-DAI1807 A/D Converter Section Schematic Diagram

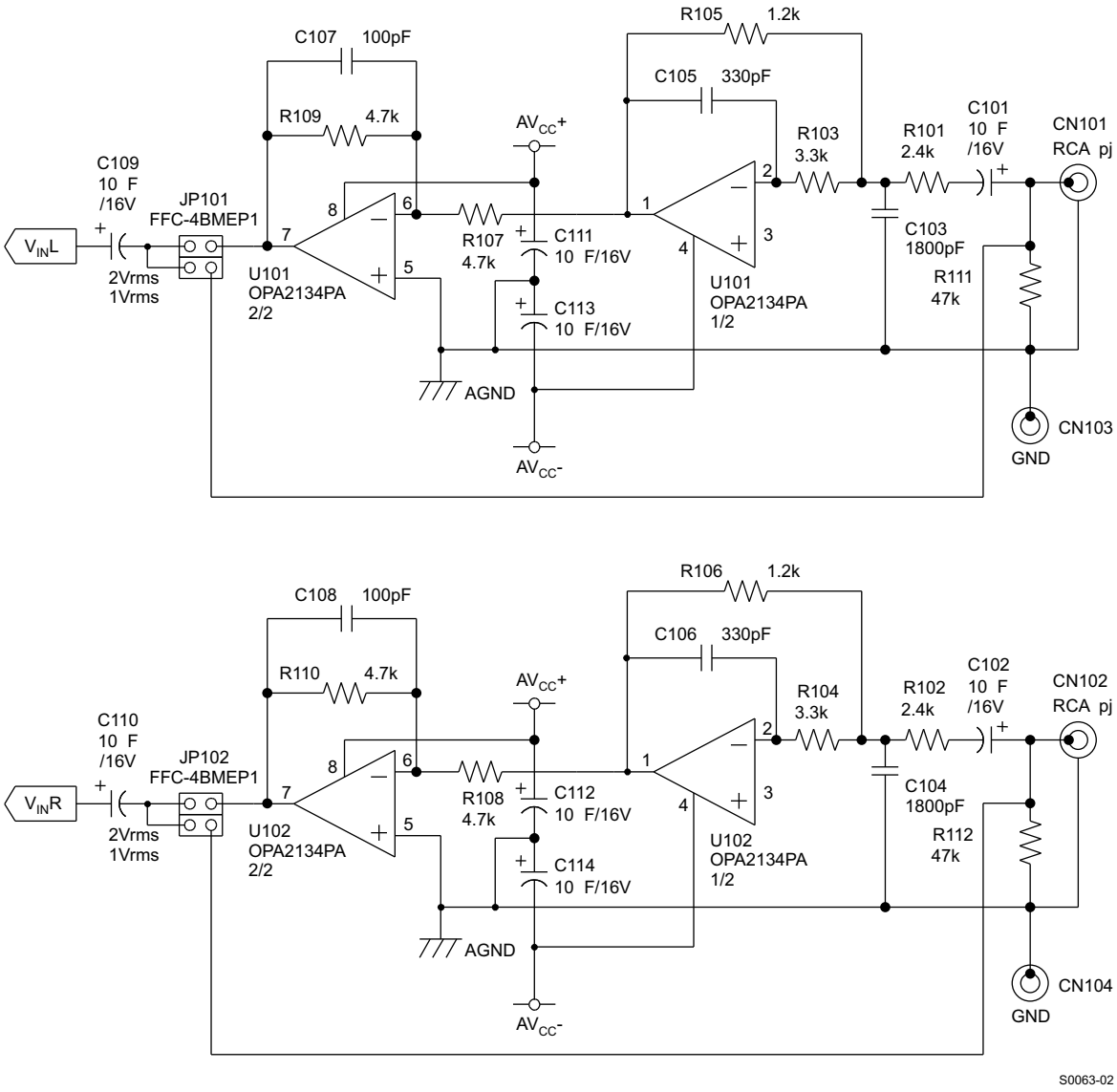


Figure 8. DEM-DAI1807 Analog Section Schematic Diagram

2.2 DEM-DAI1807 Bill of Materials

Table 9 is the bill of materials.

Table 9. Bill of Materials

Ref No.	Part Name	Spec-1	Spec-2	Part No.	Supplier	Remarks
Parts List 1/4 (Digital Section)						
C001	Electrolytic capacitor	10 µF/16 V		R3A-16V100M	ELNA	
C002	Ceramic capacitor	0.1 µF/25 V		PRE132F104Z50	Murata	
C003	Electrolytic capacitor	10 µF/16 V		R3A-16V100M	ELNA	
C004	Ceramic capacitor	0.1 µF/25 V		PRE132F104Z50	Murata	
C005	Electrolytic capacitor	10 µF/16 V		R3A-16V100M	ELNA	
C006	Ceramic capacitor	0.1 µF/25 V		PRE132F104Z50	Murata	
C007	Ceramic capacitor	0.1 µF/25 V		PRE132F104Z50	Murata	
C008	Ceramic capacitor	0.1 µF/25 V		PRE132F104Z50	Murata	
C009	Electrolytic capacitor	10 µF/16 V		R3A-16V100M	ELNA	
C010	Ceramic capacitor	0.1 µF/25 V		PRE132F104Z50	Murata	
C011	Electrolytic capacitor	100 µF/16 V		ROA-16V101M	ELNA	Unmounted
C012	Ceramic capacitor	0.1 µF/25 V		PRE132F104Z50	Murata	Unmounted
C013	Ceramic capacitor	0.1 µF/25 V		PRE132F104Z50	Murata	
C014	Ceramic capacitor	15 pF/50 V		PRE131CH150J50	Murata	
C015	Ceramic capacitor	15 pF/50 V		PRE131CH150J50	Murata	
C016	Ceramic capacitor	0.1 µF/25 V		PRE132F104Z50	Murata	
C017	Ceramic capacitor	0.1 µF/25 V		PRE132F104Z50	Murata	
C018	Ceramic capacitor	0.1 µF/25 V		PRE132F104Z50	Murata	
CN001	BNC connector			BNC-LR-PC4		Right angle
CN002	48-pin connector			FFC-48BMEP1	Honda	Unmounted
CN003	RCA connector	Yellow		LPR6520-0804	SMK	
CN004	Connector			57LE-40360-7700	Daiichi-Denshi-Kogyou	
CN005	Test terminal			LC-2-G	Mac8	GND
D001	Diode			1S133	ROHM	
D002	Diode			1S133	ROHM	
D003	Diode			1S133	ROHM	
FIL001	Filter					Unmounted
JP001	6-pin connector			FFC-6BMEP1	Honda	256/384/Ext
L001	Micro inductor	47 µH	J	EL0606SKI-470J	TDK	
R001	Metal film resistor	1/8 W, 47 kΩ	J			
R002	Metal film resistor	1/8 W, 470 Ω	J			
R003	Metal film resistor	1/8 W, 47 kΩ	J			
R004	Metal film resistor	1/8 W, 1 kΩ	J			
R005	Metal film resistor	1/8 W, 240 Ω	J			
R006	Metal film resistor	1/8 W, 110 Ω	J			
RA001	Resistor array	47 kΩ× 9	J			
RA002	Resistor array	47 kΩ× 4	J			
RA003	Resistor array	47 kΩ× 4	J			
SW001	DIP switch			DSS110	Fujisoku	DIT
SW002	DIP switch			DSS108	Fujisoku	DIT and PLL
SW003	Pushbutton switch			FP1F-2M	Fujisoku	Reset DIT
SW004	DIP switch			DSS104	Fujisoku	Unmounted
TR001	Pulse transformer			DA-02	JPC	

Table 9. Bill of Materials (continued)

Ref No.	Part Name	Spec-1	Spec-2	Part No.	Supplier	Remarks
U001	Optical transmitter			TOTX-179P	Toshiba	
U002	S/PDIF transmitter			DIT4096	TI	
U003	Buffer			SN74LVC244A	TI	
U004	Buffer			SN74LVC244A	TI	
U005	PLL clock generator			PLL1707DB	TI	
U006	One-gate inverter			SN74LVC1G04	TI	
X001	Crystal resonator	27 MHz	±50 ppm	HC-49/U-S, 27MHz	Kinseki	
	Shorting plug	x1		DIC-130	Honda	JP001
Parts List 2/4 (Power Section)						
C051	Ceramic capacitor	0.1 μF/25 V		PRE132F104Z50	Murata	
C052	Electrolytic capacitor	100 μF/16 V		ROA-16V101M	ELNA	
C053	Electrolytic capacitor	100 μF/16 V		ROA-16V101M	ELNA	
C054	Electrolytic capacitor	100 μF/16 V		ROA-16V101M	ELNA	
C055	Ceramic capacitor	0.1 μF/25 V		PRE132F104Z50	Murata	
C056	Electrolytic capacitor	10 μF/16 V		R3A-16V100M	ELNA	
CN051	Banana jack	Orange				
CN052	Banana jack	Gray				
CN053	Banana jack	Blue				
CN054	Banana jack	Red				
CN055	Banana jack	Black				
CN056	VH connector			B2P-VH	Nihon-Accyaku-Tanshi	
JP051	2-pin connector			FFC-2AMEP1	Honda	
U051	3.3-V regulator			REG1117-3.3	TI	
	Shorting plug	×1		DIC-130	Honda	JP051
Parts List 3/4 (DUT Section)						
C061	Ceramic capacitor	0.1 μF/25 V	1608 type	GRM39F104Z25PT	Murata	Chip type
C062	Electrolytic capacitor	10 μF/16 V		R3A-16V100M	ELNA	
C063	Ceramic capacitor	0.1 μF/25 V	1608 type	GRM39F104Z25PT	Murata	Chip type
C064	Electrolytic capacitor	10 μF/16 V		R3A-16V100M	ELNA	
C065	Ceramic capacitor	0.1 μF/25 V	1608 type	GRM39F104Z25PT	Murata	Chip type
C066	Electrolytic capacitor	10 μF/16 V		R3A-16V100M	ELNA	
CN057	Test terminal			LC-2-G	Mac8	GND
JP052	12 pin connector			FFC-12BMEP1	Honda	
JP053	12 pin connector			FFC-12BMEP1	Honda	
JP054	10 pin connector			FFC-10BMEP1	Honda	
R051	Metal film resistor	1/8W, 100 Ω	J			Chip type
R052	Metal film resistor	1/8W, 100 Ω	J			Chip type
R053	Metal film resistor	1/8W, 100 Ω	J			Chip type
R054	Metal film resistor	1/8W, 100 Ω	J			Chip type
R055	Metal film resistor	1/8W, 100 Ω	J			Chip type
R056	Metal film resistor	1/8W, 100 Ω	J			Chip type
R057	Metal film resistor	1/8W, 100 Ω	J			Chip type
U052	A/D converter (DUT)			PCM1807DB	TI	
	Shorting plug	×10		DIC-130	Honda	JP052, JP053, JP054

Table 9. Bill of Materials (continued)

Ref No.	Part Name	Spec-1	Spec-2	Part No.	Supplier	Remarks
Parts List 4/4 (Analog Section)						
C101	Electrolytic capacitor	10 μF/16 V		ROA-16V100M	ELNA	
C102	Electrolytic capacitor	10 μF/16 V		ROA-16V100M	ELNA	
C103	Film capacitor	1800 pF	J	APSF0100J182	Nissei	
C104	Film capacitor	1800 pF	J	APSF0100J182	Nissei	
C105	Film capacitor	330 pF	J	APSF0100J331	Nissei	
C106	Film capacitor	330 pF	J	APSF0100J331	Nissei	
C107	Film capacitor	100 pF	J	APSF0100J101	Nissei	
C108	Film capacitor	100 pF	J	APSF0100J101	Nissei	
C109	Electrolytic capacitor	10 μF/16 V		ROA-16V100M	ELNA	
C110	Electrolytic capacitor	10 μF/16 V		ROA-16V100M	ELNA	
C111	Electrolytic capacitor	10 μF/16 V		R3A-16V100M	ELNA	
C112	Electrolytic capacitor	10 μF/16 V		R3A-16V100M	ELNA	
C113	Electrolytic capacitor	10 μF/16 V		R3A-16V100M	ELNA	
C114	Electrolytic capacitor	10 μF/16 V		R3A-16V100M	ELNA	
CN101	RCA connector	White		LPR6520-0803	SMK	
CN102	RCA connector	Red		LPR6520-0802	SMK	
CN103	Test terminal			LC-2-G	Mac8	GND
CN104	Test terminal			LC-2-G	Mac8	GND
JP101	4-pin connector			FFC-4BMEP1	Honda	
JP102	4-pin connector			FFC-4BMEP1	Honda	
R101	Metal film resistor	1/8 W, 2.4 kΩ	F			
R102	Metal film resistor	1/8 W, 2.4 kΩ	F			
R103	Metal film resistor	1/8 W, 3.3 kΩ	F			
R104	Metal film resistor	1/8 W, 3.3 kΩ	F			
R105	Metal film resistor	1/8 W, 1.2 kΩ	F			
R106	Metal film resistor	1/8 W, 1.2 kΩ	F			
R107	Metal film resistor	1/8 W, 4.7 kΩ	F			
R108	Metal film resistor	1/8 W, 4.7 kΩ	F			
R109	Metal film resistor	1/8 W, 4.7 kΩ	F			
R110	Metal film resistor	1/8 W, 4.7 kΩ	F			
R111	Metal film resistor	1/8 W, 4.7 kΩ	F			
R112	Metal film resistor	1/8 W, 4.7 kΩ	F			
U101	Dual operational amplifier	DIP		OPA2134PA	TI	
U102	Dual operational amplifier	DIP		OPA2134PA	TI	
	IC socket	DIP 8-pin				U101
	IC socket	DIP 8-pin				U102
	Shorting plug	×2		DIC-130	Honda	JP101, JP102

2.3 DEM-DAI1807 Printed-Circuit Board

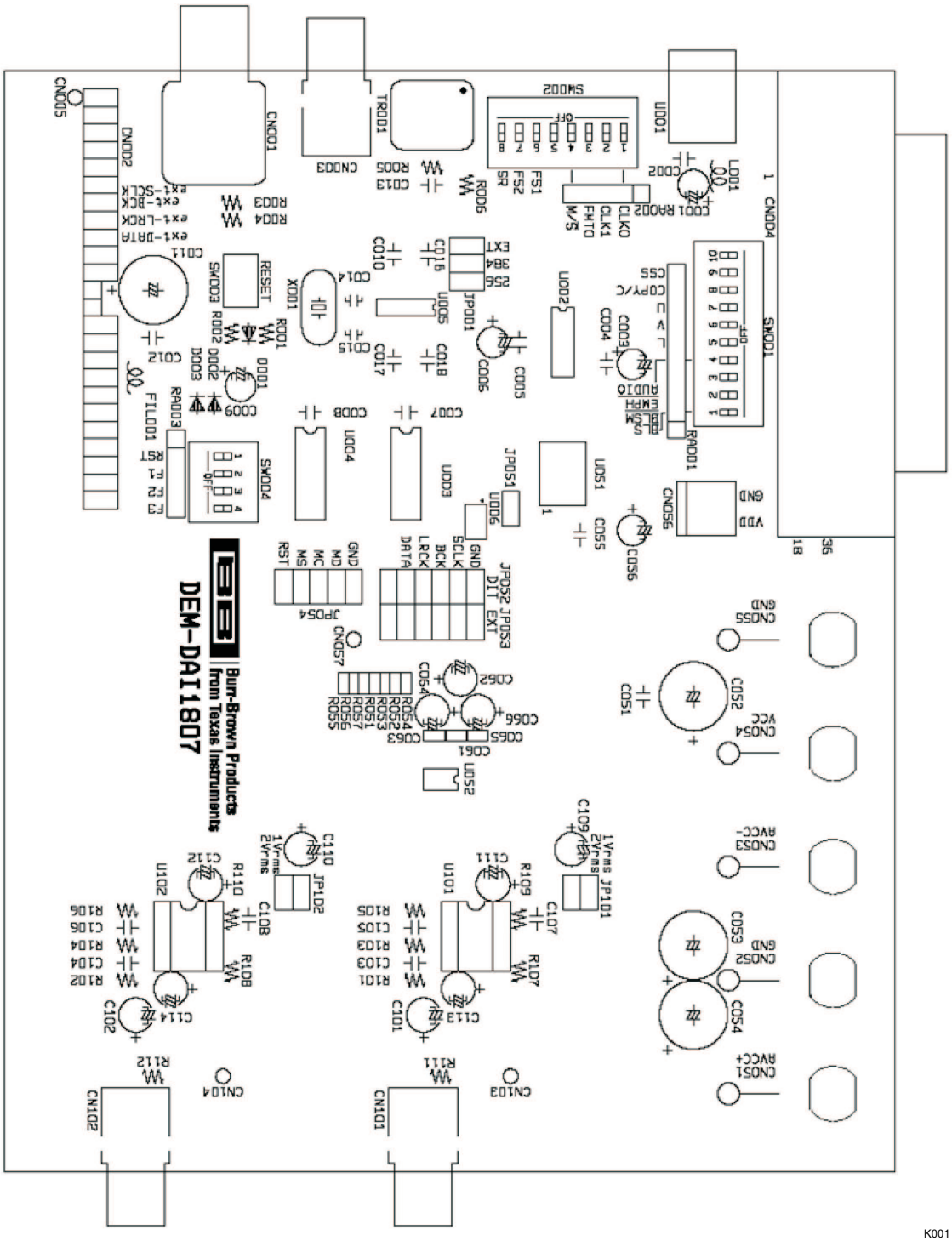
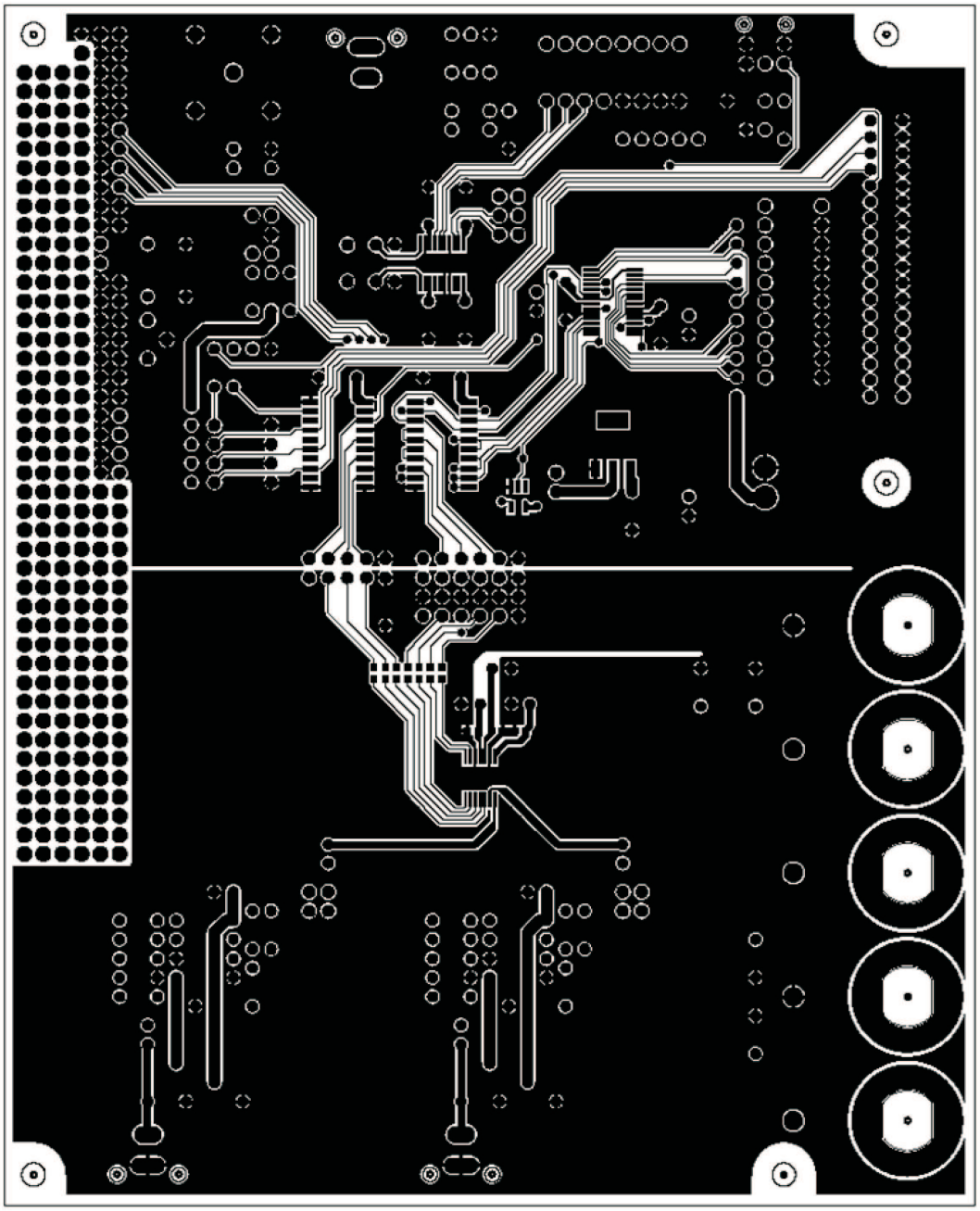
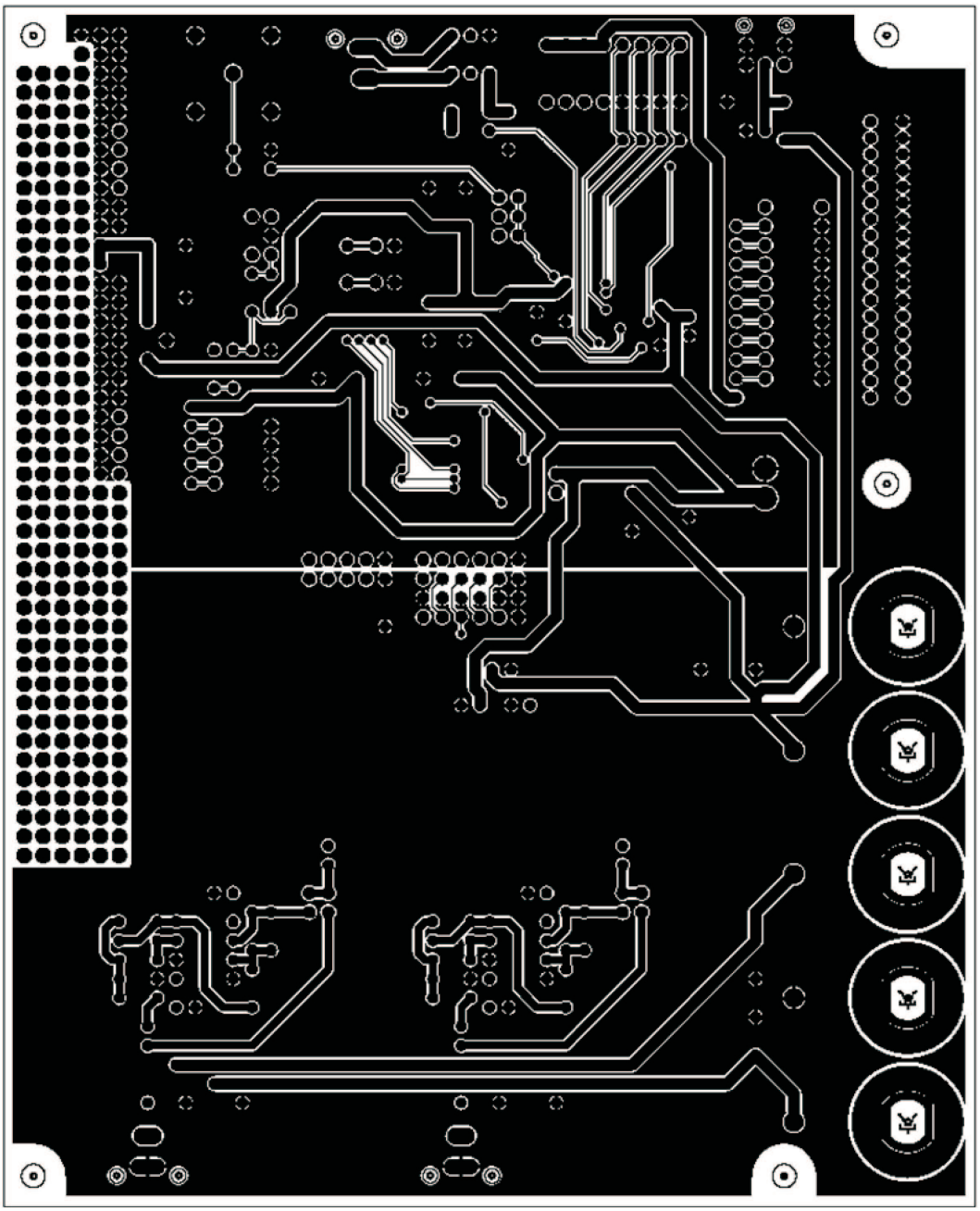


Figure 9. DEM-DAI1807 Silkscreen



K002

Figure 10. DEM-DAI1807 — Top View



K003

Figure 11. DEM-DAI1807 — Bottom View

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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