A Comparison of LinBiCMOS and CMOS Process Technology in LVDS Integrated Circuits

Rick Jordanger *Interface IC Design Engineering*

ABSTRACT

This application report compares LinBiCMOS and pure CMOS technologies for the design of high-speed low voltage differential signaling (LVDS) interface integrated circuits. LinBiCMOS is shown to be a superior technology choice in all areas. This includes electrostatic discharge (ESD) performance, maximum data rate, propagation delay, and common mode output voltage control because of the availability of bipolar transistors in the manufacturing process. LinBiCMOS-based circuitry is also shown to easily lend itself to glitch-free power-up enable circuits because of the bipolar's characteristics. Pure CMOS technology advantages are summarized to form the foundation upon which the advantages of LinBiCMOS processes are built. However, the advantages of the bipolar transistor are emphasized since a LinBiCMOS process includes the advantages of CMOS, with bipolar technology being the differentiating factor between CMOS and LinBiCMOS.

Contents

Introduction . . . 3
Summary of CMOS and Bipolar Technology Advantages for the Performance of LVDS Circuits . . . 3
Electrostatic Discharge Performance Comparison . . . 5
Maximum Data Rate and Minimum Propagation Delay . . . 8
Common Mode Output Control . . . 10
Examination of First Term of Equation (7) . . . 12
Examination of Second Term of Equation (7) . . . 13
Temperature Compensation of Equation (7) . . . 14
Glitch-Free Power-Up Enable . . . 18
Summary . . . 21
References . . . 22

List of Figures

1 NPN Saturation Phenomena . . . 4
2 NPN Based ESD Protection Scheme . . . 5
3 NMOS Based ESD Protection Scheme . . . 6
4 NPN Based ESD Protection Scheme With NPN Trigger Devices as Implemented on TI's LVDS Bus Pins . . . 7
5 NMOS Based ESD Protection Scheme Implemented on Alternate Vendor's LVDS Bus Pins . . . 7
6 Common-Mode Output Control Circuit for a LVDS Driver . . . 11

7 Brokaw Bandgap Circuit as Implemented on Many of TI's LVDS Integrated Circuits, V_{bg} Is Output Reference Voltage 12
8 CMOS Voltage Reference Circuit With Good Power Supply Rejection But Poor Process Variation 15
9 CMOS Based Brokaw Bandgap That Suffers From Major Design Problems 16
10 Bipolar Based Power-Up Enable on TI's SN65LVDS050 18
11 Start-Up Characteristic of LVDS Driver Outputs Enabled by Bipolar Based PUE on TI's SN65LVDS050 19
12 CMOS Based Power-Up Enable Implemented on Alternate Vendor's Integrated Circuit 19
13 Start-Up Characteristic of a LVDS Receiver Enabled by CMOS Based PUE on Alternate Vendor's Integrated Circuit 20

Introduction

Technology choice for all interface circuits including LVDS is governed largely by technology performance as it relates to important design specifications of high-speed data transmission and reception. Among these design specifications are ESD performance, maximum data rate, propagation delay, common-mode output voltage control, and glitch-free power up enable circuitry. This application report discusses the relative performance advantages of LinBiCMOS technology vs CMOS technology based on theoretical discussions and laboratory experiments performed on integrated circuits designed to the TIA/EIA-644 Standard: Electrical Characteristics Of Low Voltage Differential Signaling (LVDS) Interface Circuits,[1]. This application report stresses the advantages of using bipolar devices for LVDS integrated circuits, since all the advantages of CMOS circuitry are included in a LinBiCMOS technology process. However, the advantages of CMOS circuitry for LVDS integrated circuits is summarized to form the foundation for the advantages of the LinBiCMOS technology process. Most of Texas Instruments' LVDS integrated circuits are produced using LinBiCMOS technology processes.

For clarity, a typical CMOS technology manufacturing process includes, at minimum, N and P-type MOSFETs, resistors and capacitors. A typical LinBiCMOS technology manufacturing process includes, at minimum, all of the CMOS process components in addition to bipolar transistors.

The term BiCMOS is used interchangeably with LinBiCMOS in this application report. This is a matter of nomenclature which has a subtle meaning in that the prefix Lin implies a linear process for analog design. Also, the terms process, process technology, technology process, manufacturing process, and technology manufacturing process are used interchangeably. These terms refer to the steps by which semiconductor integrated circuits are produced. The term technology does not refer to the steps by which an integrated circuit is produced, but rather to a differentiation between the types of integrated circuits produced.

Summary of CMOS and Bipolar Technology Advantages for the Performance of LVDS Circuits

CMOS technology is widely used for interface integrated circuit design and has advantages over bipolar technology for certain LVDS circuits. The three main advantages that CMOS has over bipolar for use in LVDS circuits are lower power consumption, nonsaturating driver transistors, and rail-to-rail complementary logic.

The first advantage that CMOS has over bipolar is lower power consumption. Bipolars are essentially current-mode devices requiring both ac and dc input base current to function as a gain stage or logic switch. Therefore, CMOS transistors are lower power for dc static analysis and for at-speed ac analysis at the moderate frequencies of LVDS data transfer. Specifically, CMOS has lower power consumption than bipolars for typical LVDS speeds of 650 Mbps [1] and slower. However, CMOS eventually looses its power-consumption advantage, because, at higher speeds, CMOS circuits have high capacitive charging and discharging currents compared to bipolar circuits. As of this writing, these speeds are higher than necessary for LVDS drivers and receivers, so this point is not considered, since the advantage of CMOS is clear for moderate frequencies. An exact cut-off frequency where bipolar becomes lower power is difficult to derive because power consumption is very circuit-dependent. However, CMOS technology is the lower power choice for top speed LVDS drivers compared to bipolar technology.

The second advantage of CMOS over bipolar is that CMOS transistors can be run at higher speeds than bipolars when used as drivers or logic switches. This is because bipolars used as drivers or logic switches can suffer from slow-downs due to saturation. Saturation occurs when the collector voltage of a bipolar falls a sufficient amount below its base voltage, and a lot of base charge is caught in the base of the transistor. This can happen on bipolars used as rail-to-rail output drivers and can severely limit the circuits' upper speed if proper design is not enforced to prevent saturation.

For example, an NPN connected as a logic switch, as shown in Figure 1, can suffer from saturation when high output collector current drive is necessary at moderately high frequencies, such as those used in LVDS drivers and receivers. When the base voltage is pulled to a high voltage by the input driver, the collector is pulled to a logic low. This forward biases the base-collector (b-c) diode as shown in Figure 1. For the bipolar to allow the collector voltage to go back high upon a logic transition on the input, the bipolar must be brought back out of saturation. This process takes time because a lot of base charge must be removed from the base of the bipolar. Saturation, therefore, can effectively limit the upper speed at which a bipolar can operate in such an application. CMOS does not have problems with saturation since it is an isolated-gate, voltage-mode technology. Therefore, CMOS transistors are safer to use in drivers and logic switches, such as those found in LVDS driver predrives and LVDS receiver output stages.

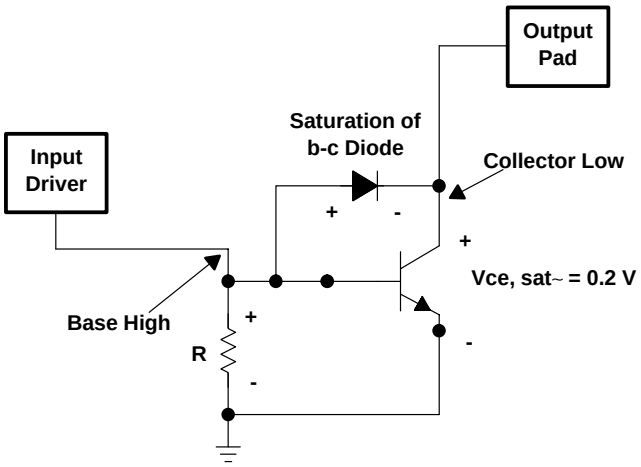

Figure 1. NPN Saturation Phenomena

Finally, ease of design in rail-to-rail complementary-logic gates is considered a CMOS advantage. Many LinBiCMOS processes do not include a PNP transistor, the logical complement of the NPN transistor, because PNPs are difficult and expensive to produce with the same gain factors as the NPN in the same manufacturing process. This makes design of rail-to-rail complementary circuits difficult or impossible with NPNs. LVDS drivers, for example, are difficult to design strictly with NPNs without the benefit of complementary MOS (CMOS) transistors. This comes from the basic fact that the inputs to LVDS drivers are usually at TTL or CMOS type voltage levels. These inputs are typically supplied with 3.3 V or 5 V, thus demanding a complementary technology process to easily implement them.

To summarize, CMOS transistors are better than bipolars in some LVDS integrated circuit applications. CMOS has lower power consumption, does not suffer from saturation when used as drivers or logic switches, and has a complementary nature for the design of rail-to-rail logic gates.

LinBiCMOS technology includes all the advantages of CMOS technology since LinBiCMOS manufacturing processes in no way subtract from the performance of CMOS transistors. Therefore, the remainder of this application report focuses on the advantages that bipolars have over CMOS for specific LVDS integrated circuit applications. LinBiCMOS technology has advantages over CMOS in any compared area, including electrostatic discharge (ESD) performance, maximum data rate, propagation delay, common mode output voltage control, and glitch-free power-up enable. This is true due to the addition of the bipolar transistor in LinBiCMOS technology as compared to CMOS technology.

Electrostatic Discharge Performance Comparison

High ESD protection is a prevalent design requirement for the bus pins of LVDS drivers and receivers. Bus lines can travel off board for many meters and encounter many sources of high ESD voltages in a harsh environment. Therefore, in such systems it is beneficial and convenient to provide integrated circuit level ESD protection that reaches into the 12-kV to 15-kV protection range for human body model (HBM) type strikes. This high level of protection is only available in integrated circuits (ICs) fabricated using modern LinBiCMOS type technology processes.

An efficient bipolar-based ESD protection scheme is almost universally available in today's sub-micron LinBiCMOS type processes. For a given area, a well designed bipolar-based ESD protection circuit out performs CMOS by a factor of about 2 to 3 times the maximum level of protection (in units of V/μm feature width). For example, a lateral NMOS device in a CMOS process is specified with a protection level of 7-10 V/μm while an NPN is specified with a 20-35 V/μm level of protection.[2] To understand why this is so, the principles by which the protection schemes operate must be understood.

A bipolar based scheme like the one shown in Figure 2 relies on the high efficiency NPN device to be able to shunt large amounts of current away from the protected circuitry. It performs this function during the short duration that an ESD strike lasts while holding the pad voltage to a safe level. This scheme needs a trigger device that senses when the pad voltage is high enough to necessitate the turn-on of the NPN device. Otherwise, the NPN base is pulled low to ground by a passive resistor so the NPN does not interfere with normal operation of the data bus pins. The trigger device can rely on various mechanisms including breakdown voltage and capacitive coupling.

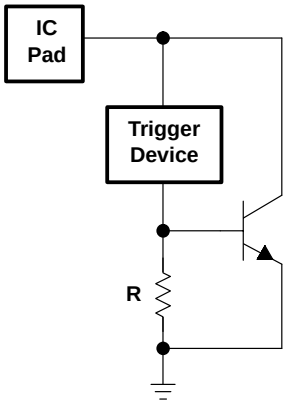

Figure 2. NPN Based ESD Protection Scheme

It is important to understand that NPNs in a LinBiCMOS process are deliberately designed to be efficient in terms of current-carrying capacity. Specifically, a good NPN is designed to have a low base resistance, high gain factor (beta or h_{fe}) and low collector on-resistance.

A CMOS-based ESD protection scheme comparable to a bipolar-based scheme relies heavily on the parasitic NPN formed by the drain (collector) - back-gate (base) - source (emitter) junctions of a large NMOS device like the one shown in Figure 3. This parasitic NPN is an inefficient device because it was not designed to be a high gain, low resistance path for ESD strikes to follow. It is merely used as an NPN because an NPN is not available in the process.

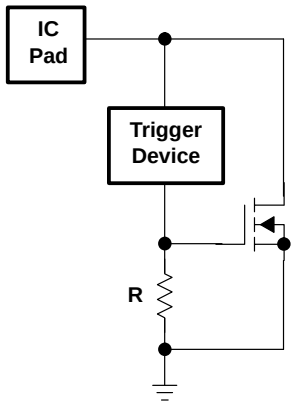

Figure 3. NMOS Based ESD Protection Scheme

If this type of CMOS ESD protection circuit is made large enough, it can perform almost as well as bipolar-based protection schemes. However, this scheme may not be practical for use on an IC because of the large amount of capacitance associated with such a large CMOS structure and because of space limitations. Specifically, slew rates can be limited on input and output pins because of the large values of capacitance added by a CMOS protection scheme with moderate-to-large values of ESD protection. In fact, input speeds can be limited to less than 1 MHz if large CMOS structures with moderate ESD protection levels are used on input pads.

Furthermore, if ESD protection devices become too large, they can limit the maximum number of pads—and thus the pins available on an IC—because the ESD protection circuits must be placed next to the pad that they protect. This is known as pad limiting and can, at the very least, raise the cost of ICs or, at the worst, make them completely impractical or impossible to produce with the desired function.

To show how much more compact a bipolar ESD scheme can be, a figure of merit must be established to compare the different implementations. A figure of merit is merely a defined mathematical quantity by which something can be compared. The figure of merit chosen in this case is maximum ESD protection per unit area of active ESD device. A particular bipolar-based ESD protection scheme in a BiCMOS process like the one shown in Figure 2 has a figure of merit of ~4 (5.5 kV /1360 μm^2) for HBM-type strikes while a CMOS protection scheme like the one in Figure 3 in the same manufacturing process has a figure of merit of ~1.2 (6 kV/ 5000 μm^2) for HBM-type strikes. This comparison shows the compactness of bipolar protection schemes which lead to smaller, less expensive IC designs and can, in some cases, make manufacturing of large-pad limited ICs possible.

A basic NPN-based ESD protection scheme implemented on the bus pins of the Texas Instruments SN65LVDS31 and SN65LVDS32 (among others) is shown in Figure 4 which uses NPN breakdown as the trigger mechanism. From laboratory testing on a LinBiCMOS-technology-based LVDS integrated circuit, the bus pins that use this very basic protection scheme have been shown to withstand greater than 15 kV HBM testing in a relatively compact size. The bus pins that use this scheme are specified with a minimum of 15 kV HBM protection. A comparable CMOS protection scheme used on an alternate vendor's CMOS-technology-based LVDS integrated circuit was also measured. Under the same test conditions, on the same type of LVDS bus pins, this scheme, shown in Figure 5, showed protection levels around 8 kV HBM on a limited sample size. These pins are specified with a minimum of 6 kV HBM protection offering less than half the guaranteed protection as the LinBiCMOS scheme. This scheme uses capacitive coupling as the trigger mechanism. The capacitor shown is not an actual additional device, it is the drain-to-gate capacitance C_{dg} of the NMOS device.

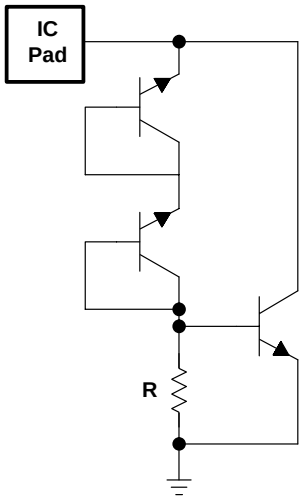

Figure 4. NPN Based ESD Protection Scheme With NPN Trigger Devices as Implemented on TI's LVDS Bus Pins

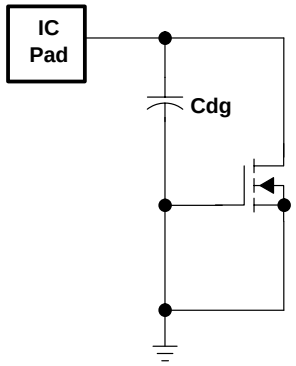

Figure 5. NMOS Based ESD Protection Scheme Implemented on Alternate Vendor's LVDS Bus Pins (trigger device is drain-to-gate capacitance, C_{dg})

As CMOS feature sizes tend to become smaller and smaller, ESD experts believe that the parasitic NPN device of the NMOS noted above will become more efficient. This is due to base width reduction of the parasitic NPN that accompanies smaller gate lengths that will raise the gain of the parasitic device and thus it should have higher current carrying capability. At the current technology nodes used for LVDS however in most cases LinBiCMOS is the only practical choice for the high ESD protection necessary on LVDS bus pins that travel off the board.

Maximum Data Rate and Minimum Propagation Delay

It is widely accepted in integrated circuit design that bipolar technology out performs CMOS technologies for maximum speed in almost any application where state of the art process technologies are used. However, this design preconception is not always true at supply voltages lower than 2–3 V where at low fanouts, CMOS can actually out-perform pure bipolar or BiCMOS circuits [3][4] in digital logic gates. Therefore, for the scope of this application report, BiCMOS and CMOS technology nodes will be compared at 3.3 V nominal supply or higher where the advantage of bipolar technology can clearly be established.

The classic reasons for the speed advantage are that bipolar devices tend to have a higher f_T or transition frequency when run at the proper current densities [5] and higher transconductance than MOSFETs. A basic definition of f_T is when the input frequency of a transistor is reached such that the transistor becomes useless because it simply has lost all gain. At the current maximum LVDS speed of 650 Mbps [2] current technology for bipolar or CMOS can easily achieve the necessary f_T levels, so focus here will be on device transconductance. Higher transconductance of devices in LVDS circuits leads to faster data rates and lower signal propagation delays.

Bipolars have a higher g_m or transconductance for a given device size vs a comparable MOSFET device size. Note g_m is a measure of output current drive for a given input voltage. This means that a bipolar transistor can be made to have as much equivalent gain as that of a much larger MOSFET. This comes from the fact that bipolar g_m is almost exclusively proportional to the collector current of the transistor as given by equation (1). Furthermore, note that the collector current grows exponentially with V_{be} as shown by equation (3) derived from equation (2).[6] For completeness, collector current is also proportional to the area of the emitter of the device.

$$g_m = \frac{I_C}{V_T} \tag{1}$$

$$V_{be} = V_T \times \ln\left[\frac{I_C}{A \times J_S}\right] \tag{2}$$

$$I_C = A \times J_S \times e^{\frac{V_{be}}{V_T}} \tag{3}$$

Where:

g_m = Transconductance in mA/V
I_c = Collector current of bipolar transistor in mA
V_T = Thermal voltage, in volts = $k \times T/q$, k is Boltzmann's constant, q is the charge on an electron, T is temperature in degrees Kelvin
J_S = Saturation current density of the transistor in mA/μm^2

A = Emitter area of bipolar in μm^2
V_{be} = Base-emitter voltage of transistor in V

Whereas for the MOSFET, the g_m is proportional to the size of the device, the current gain, and the drain current as given by equation (4).[6]. However, it is important to note that the g_m decreases with increasing gate-to-source voltage as given by equation (5) since the threshold voltage V_t is a constant. Equation (5) can be derived from equation (6) and equation (4). [6]

$$g_m = \sqrt{2 \times I_D \times K_p \times \frac{W}{L}} \tag{4}$$

or

$$g_m = \frac{2 \times I_D}{V_{gs} - V_t} \tag{5}$$

$$I_D = \frac{K_p}{2} \times \frac{W}{L} \times \left(V_{gs} - V_t\right)^2 \tag{6}$$

Where:

g_m = Transconductance in mA/V
I_D = Drain current of MOSFET transistor in mA
K_p = Current gain of MOSFET in mA/V^2
W = Width of transistor gate in μm
L = Length of transistor gate in μm
V_{gs} = Gate to source voltage of MOSFET in V
V_t = Threshold voltage of MOSFET in V

Using a numerical example for clarification illustrates this point. The bipolar thermal voltage V_T is ~26 mV at room temperature. This means that for the g_m of the MOSFET to be the same as the g_m of the bipolar, with equal drain and collector current, the MOSFET must be biased with only 52 mV of overdrive, V_{gs} - V_t, at room temperature. That is, if V_t = 0.8 V then V_{gs} must equal 0.852 V to achieve 52 mV of overdrive. This means that the MOSFET will have to be very large in terms of device width, W, to drive the required drain current as given by equation (6) because it has such a small overdrive. Notice also that the drain current only goes up with the square of the overdrive for a MOSFET vs the advantage of the exponential relationship with V_{be} for the bipolar collector current.

Therefore, to achieve the same gain factor $A_v = g_m \times r_o$, in a typical amplifier stage, MOSFETs must typically be made larger than a bipolar to achieve the same transconductance while holding r_o constant. Note, r_o is the ac output resistance of the transistor used for a gain device. This includes the ac load on the device and the ac output resistance of the device itself, properly combined. The larger MOSFET device size for a given gain A_v leads to greater capacitance in MOSFET stages. It follows that all the stages being driven in a multistage circuit will have more input capacitance when MOSFET transistors are used vs bipolars to achieve equivalent overall gain values. This in turn slows down the slew rate and therefore the data rate of a given circuit built from MOSFET's vs the same circuit built from bipolars. This is true because maximum slew rate, given in units of V/s, is proportional to current drive and inversely proportional to load capacitance.

Stated another way, for two devices with the same input capacitance in comparable process technologies, a bipolar transistor will have higher g_m than a CMOS transistor. Simulation data from a BiCMOS process reveals that the g_m for a MOSFET and a bipolar with equal input capacitance, measured with MOSFET drain current equal to the bipolar collector current, has a ratio of ~3.3. This means that the bipolar can output ~3.3 times the gain A_V as the MOSFET for a given r_O.

The higher transconductance of bipolar transistors compared to CMOS transistors makes the bipolar of greater use when gaining up small signals such as those found on the data bus lines of an LVDS system. Specifically, it takes less gain stages to gain up a typical 350 mV differential signal when using bipolar transistors rather than CMOS in the receiver stage of an LVDS circuit. It follows that a faster propagation delay will result in a circuit with fewer gain stages and faster slew rate. For completeness, it should be noted that if a small signal is gained up too far, too fast, in any technology, this can actually lead to a longer propagation delay compared to gaining up the same small signal in a few more well-designed stages. So, if well-designed gain stages incorporate bipolar transistors, the signal can typically be gained up to the same output level in 1 or 2 less stages than using CMOS, thus leading to a faster overall propagation delay. A typical LVDS receiver requires at least two, and as many as five, gain stages to gain the signal up from ~350 mV differential to 3.3 V single-ended.

Thus the conclusion is that properly designed LVDS receivers that make use of bipolar transistors for gain stages will have better maximum data rate and propagation delay because of the higher transconductance and higher slew rate of bipolar technology. It is important to reiterate that maximum data rate is directly dependent on the maximum slew rate of a circuit. This is true because once the maximum slew rate of an LVDS circuit is exceeded, the output voltage of an LVDS circuit will begin to lose its maximum peak-to-peak value and noise margin considerations will eventually be violated.

Common Mode Output Control

Common-mode voltage of bus lines in LVDS data transfer systems is an important parameter to control. This is especially important when transferring data over long distances where ground offsets can cause data to be difficult or impossible to properly receive. Therefore, the driver on an LVDS bus must control the common mode voltage as close to nominal as possible. In an LVDS data transfer system, a typical nominal common-mode bus voltage is 1.2 V. The closer this voltage is controlled to the nominal voltage the potentially greater distance data can be transferred.

See Figure 6 for an example of a common-mode output control circuit.

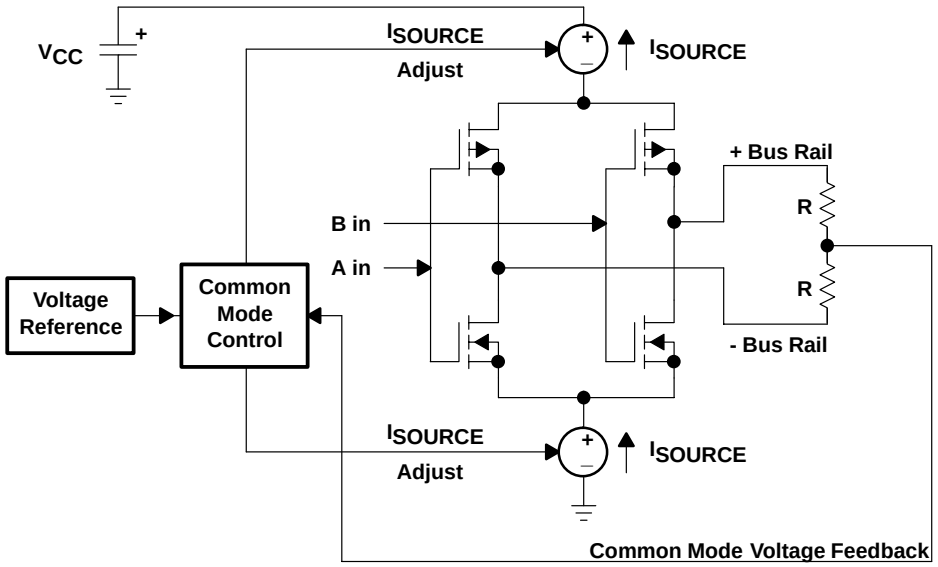

Figure 6. Common-Mode Output Control Circuit for a LVDS Driver

Bipolar circuits have an advantage over CMOS circuits for use as the reference of an output common-mode voltage control circuit. Specifically, a ground referenced bandgap voltage produced by bipolar circuits has much less variation than a voltage produced by comparable CMOS circuits. A bandgap voltage is the output voltage of a bandgap circuit that is used as a very precise voltage reference. The primary reason for this lie in the fact that a properly designed bandgap voltage has very little variation over an integrated circuit junction temperature, manufacturing process variation, and the voltage supply applied to the circuit. CMOS counterparts have especially high variation over the same parameters, especially process variation, compared to a bipolar-based bandgap circuit.

Figure 7 shows the core of a typical circuit used to produce a bandgap reference voltage on many of TI's LVDS integrated circuits such as the SN65LVDS31 and SN65LVDS32.

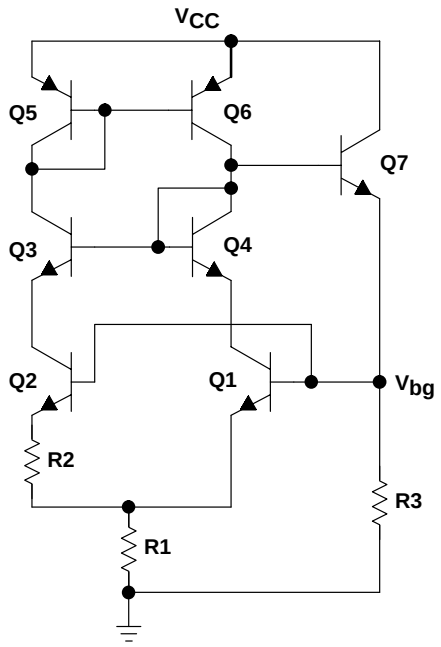

Figure 7. Brokaw Bandgap Circuit as Implemented on Many of TI's LVDS Integrated Circuits, V_{bg} Is Output Reference Voltage

The governing equation for the bipolar based bandgap, in this case a Brokaw bandgap, is given by equation 7:

$$V_{bg} = V_{be1} + 2 \times \frac{R1}{R2} \times V_T \times \ln[N] \quad (7)$$

Where:

V_{bg} = Bandgap output voltage in volts
V_{be1}= Base-emitter voltage of transistor Q1 in volts
R1 = Value of resistor R1 in ohms
R2 = Value of resistor R2 in ohms
V_T = Thermal voltage, in volts = k × T/q, k is Boltzmann's constant, q is the charge on an electron, T is temperature in degrees Kelvin
N = Ratio of the emitter sizes of Q2/Q1, unit-less

Examination of First Term of Equation (7)

Let us now examine the terms in this equation to understand why the bandgap reference voltage is so accurate. First, let us examine the V_{be} term of equation (7). A V_{be} is typically around 0.7 V and has a temperature coefficient of -2 mV/°C. The V_{be} value will depend on the current I_C as given by equation (8):

$$V_{be} = V_T \times \ln\left[\frac{I_C}{A \times J_S}\right] \quad (8)$$

Where:

J_S = Saturation current density of the transistor in mA/μm^2
A = Emitter area of bipolar in μm^2
I_C = Collector current of the transistor in mA
V_{be} and V_T have been previously defined

Using Kirchof's Voltage Law (KVL) with reference to Figure 7 it can easily be shown the following equation is true for the Brokaw bandgap:

$$V_{be1} = V_{be2} + I_{C2} \times R2 \quad (9)$$

Rewrite this equation in the form of a ΔV_{be} as given by the following equation:

$$\Delta V_{be} = V_{be1} - V_{be2} = I_{C2} \times R2 \quad (10)$$

Now, use equation (8) to substitute for the V_{be}'s equation (10), subtract natural log terms, and equation (11) can be derived since the collector currents and saturation current densities cancel (note that $I_{C1} \cong I_{C2}$ because of the PNP mirrors):

$$\Delta V_{be} = V_T \times \ln\left[\frac{A2}{A1}\right] \quad (11)$$

Where:

A1 = Emitter area of Q1
A2 = Emitter area of Q2

Equating the right-hand side of (11) with the right-hand side of (10) and replacing A2/A1 with N you get equation (12):

$$V_T \times \ln[N] = I_{C2} \times R2 = \Delta V_{be} \quad (12)$$

Where:

N = A2/A1

Equation (12) shows that I_{C2} depends on the ΔV_{be} and R2. Note that the ΔV_{be} is independent of any term except the ratio between the emitter areas N. Therefore, I_{C2} is set by the value of R2 and the ΔV_{be} as shown by rearranging equation (12):

$$I_{C2} = V_T \times \frac{\ln[N]}{R2} \quad (13)$$

Equation (13) would seem to imply that the absolute value of I_{C2} will cause V_{bg} to vary a great deal, since V_{be1} is proportional to I_{C1} (which is $\cong I_{C2}$) and V_{be1} is an additive term in the bandgap voltage [see equation (7)]. Remember that $I_{C2} \cong I_{C1}$ because of the current mirror in the bandgap circuit. However, V_{be1} is dependent on the natural log of I_{C1} as equation (8) shows and therefore V_{be1} will not change much due to I_{C1} and I_{C2} varying ±20 to 25%. This is the typical variation of the current due to the absolute value of R2 in a typical integrated circuit technology. This fact is one reason why the bandgap voltage reference is so accurate. In other words, the bipolar transistor's collector current can change a lot with just a little change in Vbe. Therefore, a ±25% change in I_C only requires a small change in V_{be}.

The entire preceding discussion accounts for the accuracy of the first term in equation (7).

Examination of Second Term of Equation (7)

Now, examining resistors R1 and R2 of the second term of equation (7), remember that the absolute value of the resistors can only be controlled within about ±20 to 25% in a typical integrated circuit technology. However, with proper sizing, the resistor matching can be controlled to within 1% across a 6-sigma statistical distribution. This tightly controlled matching partially accounts for the absolute accuracy of the second term in equation (7) because the ratio R1/R2 can be tightly controlled.

V_{bg} in equation (7) also depends on V_T and ln[N] from the second term in equation (7). Let us also examine these in turn. V_T is the thermal voltage and is a physical constant of bipolar transistors where k is Boltzmann's constant, q is the charge of an electron and T is the absolute temperature of the base-emitter junction of the bipolar transistor. Since k and q are constants, V_T is only affected by T. Therefore, the variation of V_T is linearly dependent on T and therefore easy to predict. At 27°C $V_T \cong 26$ mV and will vary directly with T.

Finally, N is the ratio of the emitter areas of Q1 and Q2 and can be tightly controlled in modern bipolar technologies to within <1% typically. Therefore, the ln[N] term also has very high accuracy.

Summarizing: The first term in equation (7) is accurate due to accuracy of the V_{be} voltage even with varying I_C. The second term in equation (7) is accurate due to tight matching of bipolar emitter areas and resistor ratios. But what about the temperature coefficients of the first and second terms caused by the V_{be} and T of the V_T term? This leads to an important aspect of equation (7).

Temperature Compensation of Equation (7)

The main feature of equation (7) lies in the fact that the ratio R1/R2 can be chosen such that the negative temperature coefficient of V_{be1}, –2 mV/°C, can be balanced by the positive temperature coefficient of the second term of equation (7). This leads to a V_{bg} voltage that is approximately constant across temperature. Note that the resistor temperature coefficients do not come into play, because as long as R1 and R2 are the same resistor type, they will have equal temperature coefficients. Therefore, the ratio R1/R2 will stay constant across temperature. The term ln[N] will also vary little with temperature because it is mostly dependent on physical sizing of the transistors.

The entire preceding discussion explains why the bandgap voltage is so accurate. In fact, if a Brokaw bandgap is properly temperature compensated by the proper choice of R1 and R2, bandgap voltage accuracy can easily be achieved within 2–5% of the nominal voltage.

This circuit can then be used as a reference voltage for a common-mode output control circuit. Intuition alone says that the better the reference for a circuit, the better a circuits' output will be controlled. In this case it can be easily seen that if a bandgap voltage can be controlled within 2–5%, the output voltage of a common–mode output control circuit can easily achieve accuracy within 4 to 7%, accounting for any offsets or inaccuracies in the common mode control circuit.

Now contrast the bipolar bandgap circuit to a typical CMOS counterpart as shown in Figure 8 which has good rejection to power supply variance but is highly dependent on process parameters.

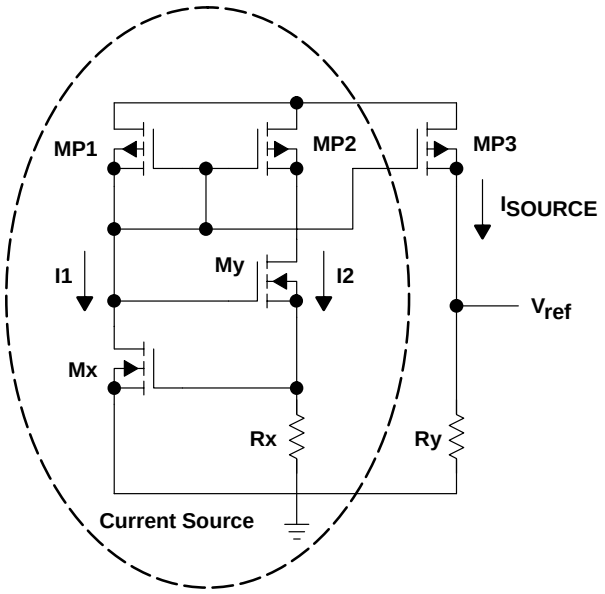

Figure 8. CMOS Voltage Reference Circuit With Good Power Supply Rejection But Poor Process Variation

This circuit is made up of current source which forces a current across the resistor RY in order to form a voltage reference. The current source is formed by forcing the current in RX to be the same as the current in MX with the PMOS mirrors. This forces the operating point of the circuit to balance where $I_1 = I_2$. In equation form this relationship can be expressed by equating the current in a MOSFET, equation (15)—assuming saturation region operation—and the current in a resistor equation (14):

$$V_r = I_2 \times R_x \tag{14}$$

$$I_1 = \frac{K_p}{2} \times \frac{W_x}{L_x} \times \left(V_{gsx} - V_t\right)^2 \tag{15}$$

Where:

K_p = Current Gain of MOSFET in mA/V^2
W_x = Width of MOSFET Mx gate in μm
L_x = Length of MOSFET Mx gate in μm
V_{gsx} = Gate to source voltage of MOSFET Mx in V
V_t = Threshold voltage of MOSFET in V
I_1 = Drain current of MOSFET Mx in mA

But $V_r = V_{gsx}$ for this particular circuit so (14) can be rewritten:

$$V_{gsx} = I_2 \times R_x \tag{16}$$

Rearranging (15) to get V_{gsx} as the dependent variable gives:

$$V_{gsx} = \left[\frac{2 \times I_1 \times L_x}{W_x \times K_p}\right]^{\frac{1}{2}} + V_t \tag{17}$$

This circuit is typically biased so that V_{gsx} is just a little larger than V_t, so (17) can be simplified to equation (18):

$$V_{gsx} \cong V_t \tag{18}$$

Now (16) and (18) can be equated to result in the final characteristic equation for the current source:

$$I_1 = I_2 \cong \frac{V_t}{R_x} \tag{19}$$

Let us examine the accuracy of the current source expressed by this simple equation. First, V_t is a quantity that can vary around ±25% in a typical CMOS process. The resistor, as previously mentioned, also varies 20 to 25% in a typical process. One might assume that variance of the current formed by this circuit could be ±50%. This, however, is not correct because of the approximations used to arrive at equation (19). Even taking into account the additional factor that the absolute value of the output voltage varies directly with the absolute value of the resistor RY, the actual variance is much less than predicted by the simplified equations. The actual voltage variance, taking into account all of the process terms, actually is more like ±15 to 20% if the circuit is properly temperature compensated. Compare this to the accuracy of the bandgap circuit, ±2 to 5%, and the advantage of a LinBiCMOS process for the accurate production of a voltage reference becomes obvious. As stated previously, this voltage can be used for the production of accurate voltage reference for a common-mode output control circuit. Note, that the TIA/EIA-644 standard specifies that this voltage, referred to as V_{OS} [7] in this specification, is controlled within 1.125 V to 1.375 V. This is a variance of ±10% off the nominal of 1.25 V. This means that the CMOS V_t voltage regulator has no chance of reliably meeting this important specification while the bandgap can easily meet it.

One might believe the circuit shown in Figure 9, produced in a CMOS process, could potentially regulate an output voltage almost as well as a bipolar circuit. The details of the equations for this circuit will not be derived here, only quickly discussed.

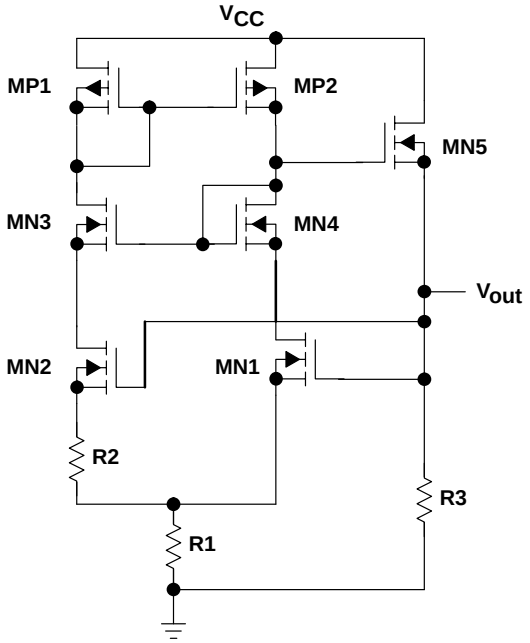

Figure 9. CMOS Based Brokaw Bandgap That Suffers From Major Design Problems

This circuit works on the principle that when MOS devices are biased in the weak inversion region they also have a natural log relationship like bipolars as given by the following equation (20) [8]:

$$I_D = K_X \times \frac{W}{L} \times e^{\left(\frac{V_{gs}}{n \times V_T}\right)} \quad (20)$$

Where:

K_X = Current Gain of MOSFET in mA/V^2
W = Width of MOSFET Mx gate in μm
L = Length of MOSFET Mx gate in μm
V_{gs} = Gate to source voltage of MOSFET Mx in V
V_T = Thermal voltage of NPN in MOSFET in V
η = V_T adjustment factor for NPN in MOSFET, unit-less
I_D = Drain current of MOSFET in mA

Following the same reasoning to derive equation (7) equation (21) for the circuit in Figure 9 can be written:

$$V_{out} = V_{t1} + 2 \times \frac{R1}{R2} \times V_T \times \ln[N] \quad (21)$$

Where:

V_{t1} = Threshold voltage of MN1 in V
N = Ratio of W1/L1 and W2/L2, unit-less
V_T = Thermal voltage in V
R1 = Value of R1 in ohm
R2 = Value of R2 in ohm

Notice that equation (21) is very similar to the Brokaw bandgap equation. This is because the MOS device is essentially being used as a bipolar device. Using a MOS as a bipolar is possible because the MOS device is biased in the weak inversion region. The circuit shown in Figure 9 seems to contradict the conclusion above that stated bipolar devices are much better building blocks for voltage references than CMOS. However, this statement is still true because this CMOS based bandgap shown in Figure 9 suffers from severe drawbacks. This circuit's accuracy is still on the order of ±14% over temperature and process variations even when properly temperature compensated. This is because the V_t of a MOSFET varies a great deal due to the manufacturing process and V_t is an additive term in equation (21). Contrast this to the steady value of a Vbe across process in equation (7). Second, since the CMOS devices must be biased in the weak inversion region, they can only be biased with a very small amount of current, typically <1 μA. At moderately high temperatures, leakage current of a MOSFET becomes 1 to 10 times the weak inversion current and thus the devices no longer function properly since the leakage term dominates the MOSFET's drain current. Furthermore, these small bias currents of <1 μA are susceptible to on-chip current noise which can also severely affect this circuits accuracy. Therefore, because of the inaccuracy and difficulties in producing a bandgap voltage from MOSFETs biased in the weak inversion region, it is still far more reliable and practical to produce voltage references from bipolar circuits.

Glitch-Free Power-Up Enable

When powering up an LVDS integrated circuit, noise or glitches produced on the output pins of the chip are undesirable. Noise or glitches on output pins can lead to false data transfers in a system or disturbances to other system circuitry. This is why it is important to hold an LVDS output pin in a known state until on-chip power is at a safe level and input signals are propagated to the output drivers. This is the purpose of an IC level power-up enable circuit or PUE. A PUE senses the voltage on the power pin of an integrated circuit and will hold the integrated circuit outputs in a known state until Vcc is high enough for the integrated circuit level logic to function. At that time the logic can drive the outputs to a known state with a maximum of only 1 logic transition. Bipolar circuits naturally lend themselves to be building blocks of PUE circuits because of their clean start-up characteristics due to the fact they are ground referenced.

Figure 10 shows the core of a bipolar PUE circuit implemented on the TI SN65LVDS050:

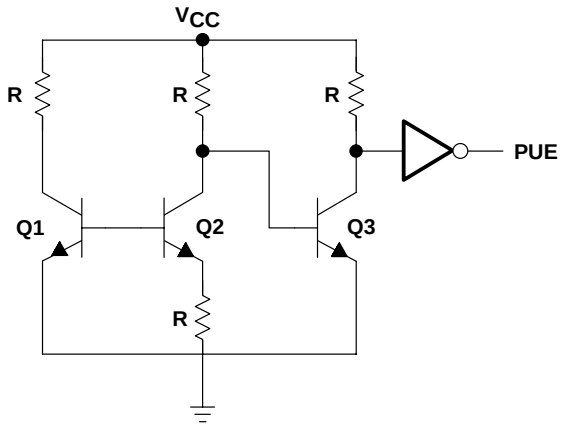

Figure 10. Bipolar Based Power-Up Enable on TI's SN65LVDS050

The circuit shown in Figure 10 is actually a bandgap which is, as described previously, a ground referenced circuit. This means it will trigger its output based on the absolute value of V_{CC} as compared to ground level potential. Because the bandgap is so accurate, it can be designed so that it will trip its output at a given absolute value of V_{CC} very reliably. In addition, the bipolar-based PUE does not require a lot of power supply current which tends to pull the on-chip supply down and cause false trips. Therefore, this circuit does not have an output signal that tends to bounce on and off and cause noise or glitches. Contrast the bipolar-based PUE circuits' performance to the CMOS PUE discussed below and the reasons that the bandgap makes a great PUE will become more obvious.

As an additional benefit, the bipolar-based PUE does not require any extra start-up circuitry to make sure that it does not converge to a zero-current operating point. Certain bandgap circuits require a momentary current injection to make them start up correctly, an example of which is the Brokaw bandgap discussed above. The fact that no start-up circuitry is required for the PUE in Figure 10 leads to simplified circuitry that naturally turns on at an accurate threshold, based on the value of power supply voltage. See Figure 11 below and notice the clean start-up characteristic of the LVDS driver outputs on the TI SN65LVDS050 measured with single-ended probes and the differential voltage derived mathematically with the oscilloscope:

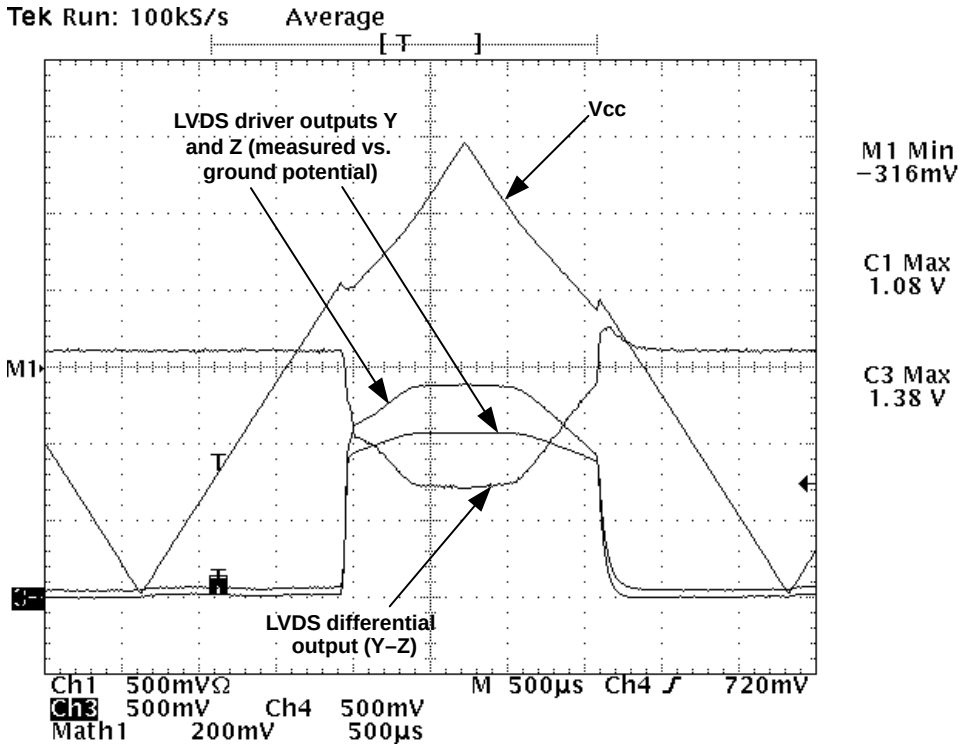

Figure 11. Start-Up Characteristic of LVDS Driver Outputs Enabled by Bipolar Based PUE on TI's SN65LVDS050

Now contrast the bipolar PUE above to a CMOS PUE implemented on an alternate vendor's integrated circuit as shown in Figure 12:

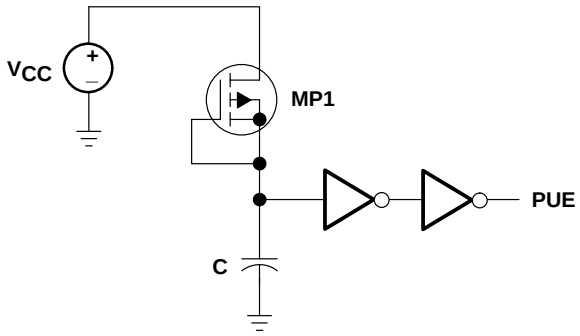

Figure 12. CMOS Based Power-Up Enable Implemented on Alternate Vendor's Integrated Circuit

This circuit has severe problems with start-up which causes the output signal of the PUE to bounce on and off. This leads to glitches and noise on the output of circuitry like those in Figure 13 whose enable is qualified by the output of this PUE. These glitches happen because the nature of this circuit has a basic design flaw.

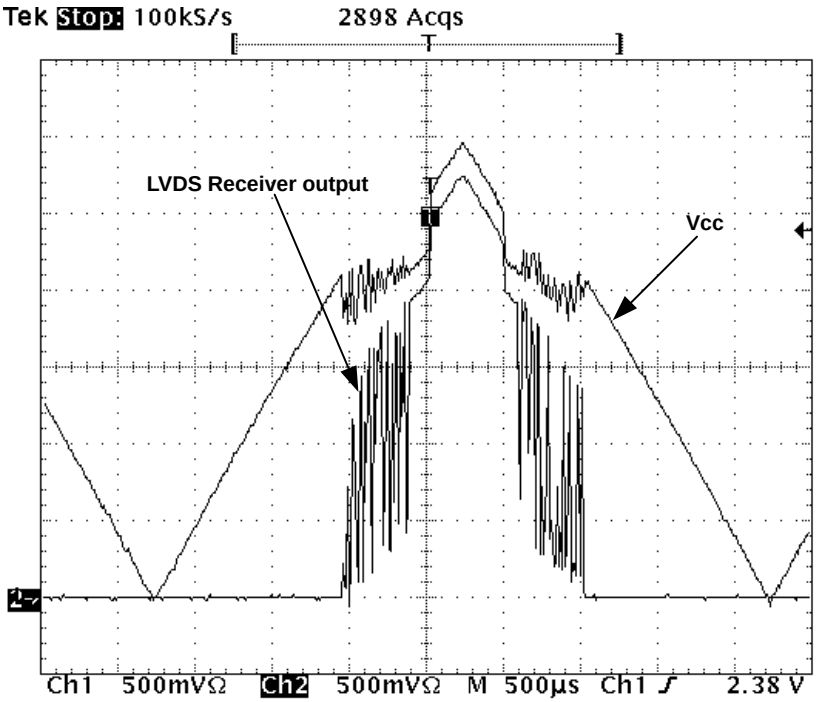

Figure 13. Start-Up Characteristic of a LVDS Receiver Enabled by CMOS Based PUE on Alternate Vendor's Integrated Circuit

The circuit works on the principal that as the power supply voltage Vcc comes up, the MOSFET-connected diode will begin to conduct current when Vcc reaches about 1 MOSFET V_t above ground. At this point the drain current of the MOSFET will charge the capacitor, which will eventually charge to a value that trips the inverter connected to the capacitor and indicate that the power supply has reached a safe operating level for on-chip logic. Unfortunately, this circuit suffers two major problems.

First, the inverter's trip point and the V_t of the diode-connected MOSFET determine at what value of Vcc the output of the circuit will indicate that power is up by the assertion of the output voltage to a high value. Since the circuits' trip point partially depends on the inverter's trip point, this is a Vcc referenced circuit. This means that the circuit is trying to reference itself to a voltage that is changing. Contrast this to the bandgap PUE which is ground referenced and it becomes obvious that the CMOS PUE will have difficulties in turning on at the designed trip point. That is, since ground is not moving for the bandgap PUE it is a stable reference for the circuit, while the CMOS PUEs are unstable due to a moving reference.

Futhermore, as mentioned previously, the V_t of a MOSFET can vary ±25%. In addition, inverters are also subject to trip point values that vary around ±10 to 15% in a typical CMOS process. The combination of these two errors leads to a great deal of absolute error in the trip voltage of this CMOS PUE circuit.

Second, the circuit has a basic design flaw which causes the glitches that are observed in Figure 13. When V_{CC} is coming up during startup the capacitor will receive charge through the MOSFET-connected diode. As the capacitor becomes charged, it will eventually trip the inverter to indicate that on-chip power has reached a voltage threshold. However, at this point the inverter pulls a great deal of supply current off of the local Vcc on-chip which causes a local dip in the Vcc voltage. This is possible because of voltage drops across the inductive IC bondwires and metal bus lines caused by the large current spikes that the inverter pulls from Vcc. These local voltage drops in turn trip the inverter to the opposite state indicating a loss of PUE signal. This cycle repeats itself until there is enough charge on the capacitor to keep the voltage on the capacitor high enough so that the inverter no longer has false trips and the output signal stabilizes. However, in the time before stabilization, the output of the LVDS receiver reacts to the glitches on the PUE signal and causes the waveform observed in Figure 13. For these reasons it is easy to see that ground referenced bandgap PUE circuits are far more reliable than V_{CC} referenced CMOS PUE circuits in terms of glitch-free reliable start-up.

Summary

LinBiCMOS technology, like that found in all of TI's LVDS integrated circuits, offers several important advantages over the use of CMOS technology for the design of LVDS integrated circuits. This is because of the added performance advantages of the bipolar device in the LinBiCMOS process. This application report has discussed the advantages of LinBiCMOS technology due to the bipolar device in the areas of electrostatic discharge (ESD) performance, maximum data rate, propagation delay, common-mode output voltage control, and clean power-up enable circuits. The advantages of CMOS technology, which are included in LinBiCMOS technology, were also discussed and summarized.

It is difficult, if not impossible, for CMOS technology to match the performance of LinBiCMOS technology in any area of LVDS system performance. CMOS technology does have advantages over bipolar technology in the areas of power consumption, nonsaturating drivers and rail-to-rail complementary logic design. However, these advantages are included in LinBiCMOS processes. Therefore, LinBiCMOS is the process of choice for the highest performance available in a LVDS data transfer system.

References

1. TIA/EIA–644 Standard: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, Telecommunications Industry Association, 1996.
2. Electrostatic Discharge in Integrated Circuits Conference. UC Berkley Extension, Ajith Amerasekera. Nov 3–5, 1997, BiCMOS/Bipolar protection section of class notes.
3. Trade-offs between CMOS and BiCMOS. Nagano, T., Solid-State and Integrated Circuit Technology, 1995 4th International Conference on, 1995 , Page(s): 763 –767.
4. A review on low-voltage BiCMOS circuits and a BiCMOS vs CMOS speed comparison. Sakurai, T. Circuits and Systems, 1992., Proceedings of the 35th Midwest Symposium on, 1992, Page(s): 564 –567 vol.1.
5. The high-frequency analogue performance of MOSFETs Vanoppen, R.R.J.; Geelen, J.A.M.; Klassen, D.B.M. Electron Devices Meeting, 1994. Technical Digest., International, 1994 , Page(s): 173 –176.
6. Analysis and Design of Analog Integrated Circuits, 3rd Edition. Paul R. Gray and Rober G. Meyer. Wiley, 1993. Page(s): 81–83.
7. TIA/EIA–644 Standard: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits. Telecommunications Industry Association, 1996, Pages (s) 8.
8. Analysis and Design of Analog Integrated Circuits, 3rd Edition. Paul R. Gray and Rober G. Meyer.1993. Page(s): 76.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265