

Difference Between the Intel™ 21150ac/bc and the PCI2050/2050B

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ABSTRACT

This application report describes the functional difference between the Intel 21150ac/bc and the PCI2050/2050B. The PCI2050 is a 32-bit, 33-MHz PCI-to-PCI bridge that was designed to be pin-to-pin compatible with the Intel 21150ac. The PCI2050B is a 32-bit, 66-MHz PCI-to-PCI bridge that was designed to be pin-to-pin compatible with the Intel 21150bc.

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1 PCI Local Bus Specification Differences

Intel 21150 is PCI Local Bus Specification Rev 2.1 compliant. The PCI2050/2050B are PCI Local Bus Specification Rev 2.2 compliant.

2 PCI Bus Power Management Interface Specification Differences

Intel 21150 is PCI Bus Power Management Interface Specification Rev 1.0 compliant. PCI2050/2050B are architecture configurable for the PCI Bus Power Management Interface Specification via the MS0 and MS1 signals. Table 1 shows the mode selection via MS0 and MS1. When MS0 is pulled high, PCI2050/2050B are in Intel mode and are PCI Bus Power Management Interface Specification Rev 1.0 compliant. When MS0 is pulled low, PCI2050/2050B are in TI mode and are PCI Bus Power Management Interface Specification Rev 1.1 compliant.

Table 1. Mode Selection Via MS0 and MS1

MS0	MS1	MODE
0	0	CompactPCI™ hot swap friendly. PCI Bus Power Management Interface Specification Rev 1.1
0	1	CompactPCI™ hot swap disabled. PCI Bus Power Management Interface Specification Rev 1.1
1	X	Intel compatible. CompactPCI™ hot swap disabled. PCI Bus Power Management Interface Specification Rev 1.0

3 Power-Up Difference

While the Intel 21150ac/bc does not have a specific power-up sequence, TI recommends that P_VCCP and S_VCCP be powered-up first before applying power to VCC.

4 Fast Back-to-Back Transaction

Intel 21150ac/bc supports fast back-to-back transaction as a master and as a target. The PCI2050 supports fast back-to-back transaction only as a target. The PCI2050B supports fast back-to-back transaction as a master and as a target.

5 Register Differences

The PCI2050/2050B have a Device ID of AC28h and a Vendor ID of 104Ch. The Revision ID for the PCI2050 is 00h, and the Revision ID for the PCI2050B is 02h.

For PCI2050/2050B, the Hot-Swap Control and Status Register has been added for CompactPCI hot swap support. While in CompactPCI hot swap mode, the Hot-Swap Control and Status Register can be used to control the hot-swap functionality of the PCI2050/2050B. The PCI2050/2050B can be set up to signal ENUM#.

The default state of the Posted Write Combining is enabled in PCI2050B, and is disabled in Intel PCI21150.

6 FIFO Size Differences

For the PCI2050B, the FIFO size is 32 DW for delayed responses (3 each direction) or 64 DW posted write and delayed request FIFO (1 each direction).

7 References

1. *Advanced Configuration and Power Interface (ACPI) Revision 1.0*
2. *PCI Local Bus Specification Revision 2.2*
3. *PCI Mobile Design Guide, Revision 1.0*
4. *PCI-to-PCI Bridge Architecture Specification Revision 1.1*
5. *PCI Bus Power Management Interface Specification Revision 1.1*
6. *PICMG Compact-PCI Hot Swap Specification Revision 1.0*

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